Whitepaper

XS NexPack: Optimising thermal performance and parasitic inductance in surface-mount SiC power modules

Design trade-offs and validation of a compact isolated power module architecture

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The increasing adoption of silicon carbide (SiC) power semiconductors is enabling significant improvements in power conversion efficiency, switching performance, and power density across applications such as EV charging infrastructure, battery energy storage systems (BESS), renewable energy converters, industrial drives, and AI data center power supplies. However, achieving the full performance potential of wide-bandgap devices requires packaging technologies that address thermal management, electromagnetic performance, electrical isolation, and system integration challenges. Existing surface-mount power modules were largely developed for traditional silicon devices and often introduce compromises in footprint, thermal resistance, and parasitic inductance.

This whitepaper examines the design considerations and engineering trade-offs associated with compact isolated surface-mount power modules for SiC power semiconductors. Using the XS NexPack platform as a case study, the impact of package architecture on thermal performance, electrical isolation, parasitic inductance and system integration is evaluated through thermal and electromagnetic simulation. By combining integrated electrical isolation, top-side cooling, flexible internal layouts, Kelvin source connections, and optional integrated temperature sensing within a compact package footprint, XS NexPack has been developed specifically to address the requirements of modern SiC power conversion systems. Thermal and electromagnetic simulation results demonstrate measurable improvements in both thermal impedance and stray inductance when compared with alternative package approaches, enabling designers to achieve higher system efficiency, increased power density, and simplified assembly.

1. Introduction & Background

The global transition toward electrification and energy efficiency is driving rapid adoption of wide-bandgap semiconductor technologies. Silicon carbide MOSFETs are increasingly being selected for high-voltage applications due to their ability to operate at higher switching frequencies, lower switching losses, and higher operating temperatures than conventional silicon devices. Moreover, a very low RDSon value are achievable in the high voltage domain by this WBG technology.

While significant advances have been made at the semiconductor level, packaging technology has increasingly become a limiting factor in overall system performance. Traditional packages originally developed for silicon power devices are often physically larger than necessary for modern SiC dies and can introduce thermal and electrical constraints that limit the benefits of wide-bandgap technology.

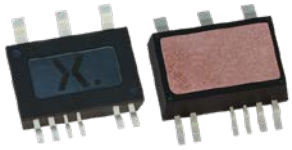

Figure 1. Nexperia XS NexPack isolated surface-mount power module.

At the system level, engineers must simultaneously balance several competing requirements:

- Maximising power density
- Minimising thermal resistance
- Reducing parasitic inductance
- Maintaining robust electrical isolation
- Simplifying PCB assembly
- Supporting automated manufacturing processes

These competing requirements have led to increased interest in surface-mount power modules that combine the integration advantages of traditional modules with the manufacturing flexibility of discrete package solutions. However, many existing module platforms remain optimised for silicon-era device dimensions and architectures, presenting opportunities for further innovation in package design.

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2. Engineering challenges in high-density SiC power systems

As switching frequencies increase and power converter designs become more compact, packaging has a growing influence on system performance.

Thermal management challenges

Wide-bandgap devices can process greater power within a smaller silicon area, increasing heat flux density. Effective heat removal becomes essential to maximise power output while maintaining safe operating temperatures.

Many conventional package solutions require additional insulating materials between the package and cooling system. These materials typically exhibit relatively poor thermal conductivity and contribute significantly to junction-to-ambient thermal resistance.

Parasitic inductance challenges

Fast switching transitions produce high di/dt values, making circuit parasitic increasingly important. Stray inductance within power loops contributes directly to voltage overshoot according to:

$$V_{overshoot} = L_{\sigma} \times \frac{dI}{dt}$$

Where:
- $L\sigma$ = stray inductance
- dI/dt = switching current slew rate

Reducing power loop inductance is therefore critical for improving switching behaviour and reducing EMI concerns.

As side effect, but very important consequence, higher switching application using compact design can show higher efficiency that a similar discrete solution as reported in the following comparison:

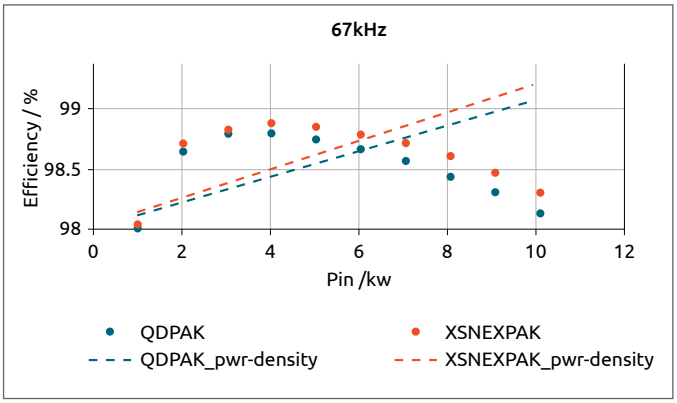

Fig. X efficiency comparison of simila devices in a discrete package half bridge configuration vs. NS XPAK compact device.

As effect of minimization of turn on switching losses, due to the stary inductances of the commutation loop, this 30mOhm SIC MOSFET half bridge housed in NS NEXPAK show higher efficiency than the equivalent discrete solution, even in a TOP side cooling package.

Isolation and assembly challenges

High-voltage systems require robust electrical isolation. Conventional approaches often rely on external insulation materials, increasing component count, assembly complexity, and thermal resistance.

Together, these challenges highlight the need for a compact module platform specifically designed around the requirements of modern SiC devices rather than adapted from existing silicon-based solutions.

3. Key design trade-offs in compact isolated modules

Designing an isolated surface-mount module for wide-bandgap devices requires balancing competing electrical, thermal and mechanical requirements.

Thermal conductivity versus isolation

Increasing dielectric thickness improves insulation capability but increases thermal resistance.

Footprint versus parasitic inductance

Reducing package size generally improves loop inductance but can constrain heat spreading area.

Integration versus flexibility

Integrating sensing and switching functions reduces component count but increases package complexity.

Top-side cooling considerations

Top-side cooling can improve system integration but imposes constraints on package mechanical structure and creepage design.

4. Nexperia XS NexPack case study: A compact isolated surface-mount module architecture

XS NexPack was developed as a compact isolated surface-mount power module platform optimised for SiC power semiconductors.

The platform integrates:
- Metal-ceramic substrate technology
- Top-side cooling
- Half-bridge circuit capability
- Kelvin source connections
- Integrated temperature monitoring
- Flexible internal circuit configurations

Unlike many conventional power modules, the platform was developed with scalability in mind, allowing multiple future product variants to be built around a common design and manufacturing architecture.

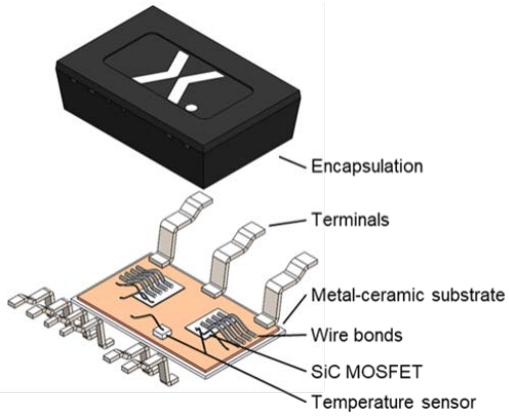

Figure 2. Exploded view showing XS NexPack package architecture.

Metal-ceramic substrate architecture

The foundation of the XS NexPack platform is a metal-ceramic substrate that combines high thermal conductivity with inherent electrical isolation.

Copper layers are selectively patterned to create isolated circuit regions while supporting direct mounting of semiconductor chips, temperature sensors, and package leads. This architecture enables significant flexibility in internal circuit design while maintaining efficient thermal performance.

Compared to non-isolated package concepts, the integrated isolation layer eliminates the need for additional external insulation materials, reducing overall assembly complexity.

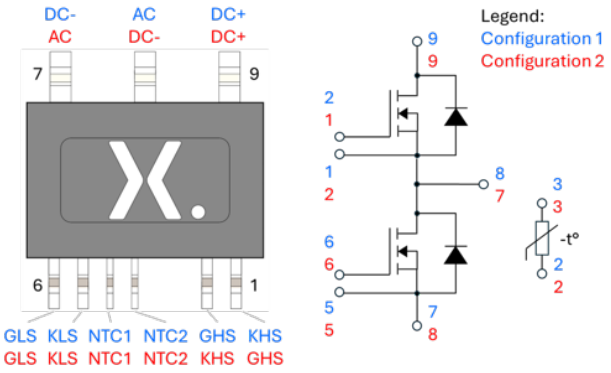

Figure 3. Examples of alternative internal pin configurations.

High-voltage isolation design

Electrical isolation is a critical requirement in modern high-voltage power converters.

The XS NexPack package incorporates carefully engineered creepage distances between leads and thermal interfaces, supporting operation up to 960 V DC under typical automotive operating conditions. The package achieves this without the need for complex external moulding features, providing greater flexibility for thermal management and mounting strategies.

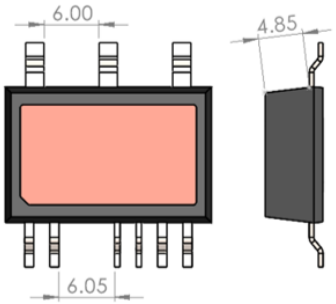

Figure 4. Package creepage distances and isolation design features.

Mechanical design for simplified integration

The package adopts a zero-standoff mechanical concept in which the mounting surfaces of the package body and leads are nominally coplanar.

This approach provides tighter control of package height variation and simplifies attachment to common cooling structures, particularly when multiple modules are mounted in parallel.

An optional integrated NTC temperature sensor also enables accurate real-time temperature monitoring without requiring additional board-level sensing components.

Figure 5. Cross-section illustrating the zero-standoff package concept.

5. Testing, simulation & validation

Package footprint comparison

As power electronics systems become increasingly compact, PCB area represents a valuable resource.

XS NexPack delivers meaningful reductions in PCB footprint compared with both equivalent discrete package solutions and existing surface-mount module approaches. The compact architecture contributes directly to higher power density and simplified system integration.

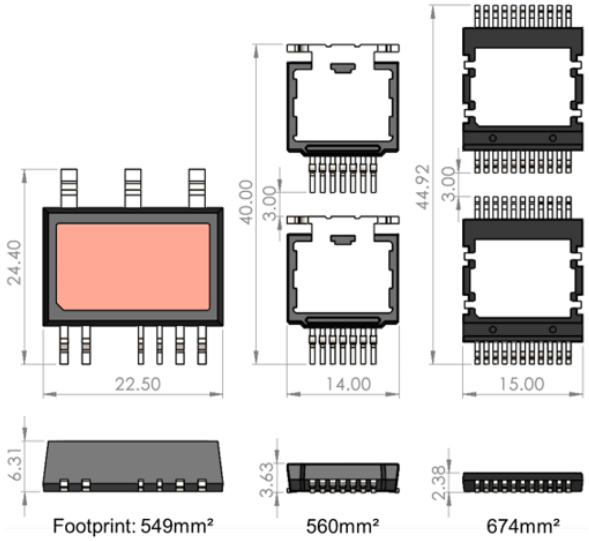

Figure 6. Footprint comparison versus X.PAK and QDPAK solutions.

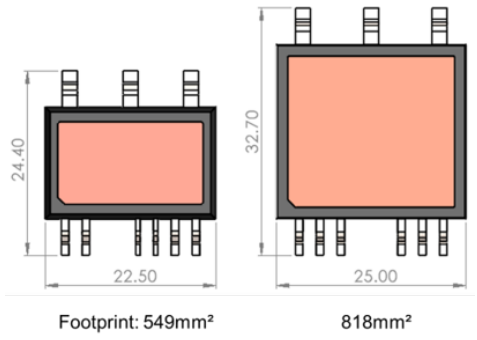

Figure 7. Comparison versus market-standard surface-mount power module.

Thermal performance validationn

To evaluate thermal behaviour, finite element simulations were performed using realistic cooling conditions and thermal interface materials.

The primary thermal resistance metrics were calculated as:

$$Pd= (Tj-Ta)/Rthj-a$$

THE AMOUNT OF POWER MANAGEABLE IS LINKED TO THE STACK OF LAYERS FROM THE SIC DIE TO THE AMBIENT INCLUDING THE TIM (THERMAL MATERIAL INTERFACE), THE HEAT-SINK CONNCETED TROUGHT THE TIM TO THE DBC AND FINALLY THE FLUID OF THE COOLING SYSTEM DEFINING THE AMBIENT TEMPERATURE AT WHICH THE DEVICE IS FORCED TO MANAGE THE POWER.

$$Rthj-c=(Tj-Tc)/Pd$$

where:

- T_J is junction temperature
- T_C is case temperature
- T_S is heat sink temperature
- Ambient temperatute
- P is dissipated power

Simulation results showed thermal resistance values of:

- RTH(J-C): 0.616 °C/W junction to case Rth
- RTH(J-S): 1.451 °C/W junction to Heat-sink Rth
- RTH(J-F): 1.746 °C/W junction to fluid Rth

where

$$R_{\text{th j – case(typ)}} = \frac{T_{\text{j(ave)}} - T_{\text{case(max)}}}{P_{\text{switch}}}$$

$$R_{\text{th j – sink(typ)}} = \frac{T_{\text{j(ave)}} - T_{\text{sink(max)}}}{P_{\text{switch}}}$$

$$R_{\text{thj – fluid(typ)}} = \frac{T_{\text{j(ave)}} - T_{\text{fluid(max)}}}{P_{\text{switch}}}$$

$$R_{\text{th j – case(max)}} = \frac{T_{\text{j(ave)}} - T_{\text{case(max)}}}{P_{\text{switch}}}$$

$$R_{\text{th j – sink(max)}} = \frac{T_{\text{j(ave)}} - T_{\text{sink(max)}}}{P_{\text{switch}}}$$

$$R_{\text{thj – fluid(max)}} = \frac{T_{\text{j(ave)}} - T_{\text{fluid(max)}}}{P_{\text{switch}}}$$

Considering all Rthj-a contribution we need to remark that:

- **Rth-jc typ**
  - Junction to case estimated with average junction temperature (Tj avg)
  - and maximum case temperature (Tc)

- **Rth-jc max**
  - Junction to case estimated with maximum junction temperature
  - (Tj max) and maximum case temperature (Tc)

- **Rth-js typ**
  - Junction to heatsink estimated with average junction temperature
  - (Tj avg) and maximum heatsink temperature (Ts)

- **Rth-js max**
  - Junction to heatsink estimated with maximum junction temperature
  - (Tj max) and maximum heatsink temperature (Ts)

- **Rth-jf typ**
  - Junction to heatsink estimated with average junction temperature
  - (Tj avg) and maximum fluid temperature (Tf)

- **Rth-jf max**
  - Junction to fluid estimated with maximum junction temperature
  - (Tj max) and maximum fluid temperature (Tf)

Compared with an equivalent X.PAK implementation, XS NexPack demonstrated a 12% reduction in junction-to-sink thermal resistance and a 4% reduction in junction-to-fluid thermal resistance. Additional improvements are achievable when higher-performance ceramic materials such as silicon nitride are employed.

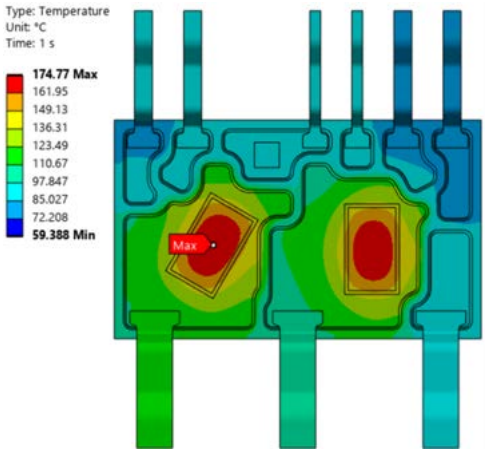

Figure 8. Thermal simulation results and temperature distribution.

Integrated temperature sensing validation

The integrated NTC sensor provides significantly improved thermal coupling compared with external temperature monitoring solutions.

Transient simulation results demonstrate close correlation between device temperature and sensor response, enabling more accurate thermal protection and control strategies.

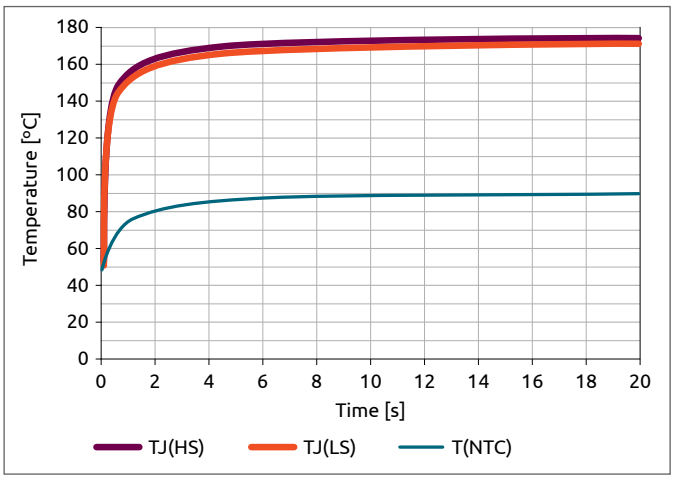

Figure 9. Dynamic temperature response of MOSFETs and integrated NTC.

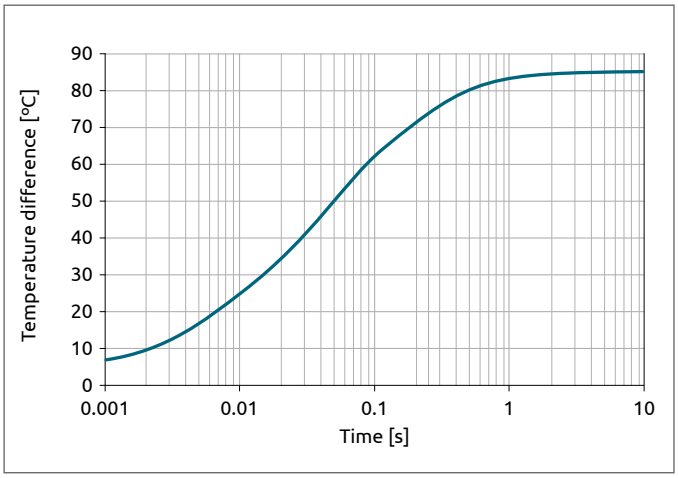

Figure 10. Temperature offset between MOSFET junction and NTC sensor.

Parasitic inductance analysis

Electromagnetic simulations were conducted using ANSYS Q3D to quantify power loop inductance.

The XS NexPack configuration achieved a loop inductance of 14.7 nH.

An equivalent half-bridge implementation using discrete X.PAK devices exhibited a loop inductance of 18.9 nH, representing a 28% increase.

The reduced inductance of the module architecture contributes directly to lower switching stress, reduced voltage overshoot, and improved electromagnetic performance and higher efficiency at higher switching frequency.

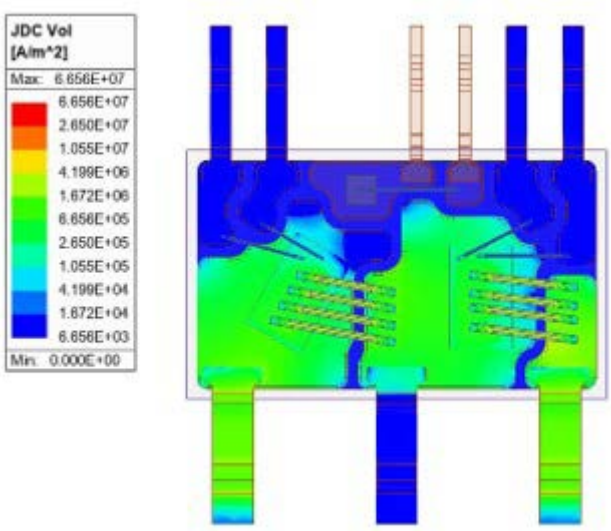

Figure 11. Current density distribution from electromagnetic simulation.

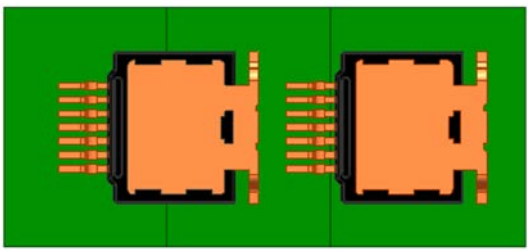

Figure 12. Reference layout used for comparison against discrete packages.

6. Conclusion

The results presented in this study demonstrate that package architecture remains a significant contributor to overall converter performance in wide-bandgap power systems. Through optimisation of substrate design, internal layout, thermal interfaces and interconnection structure, measurable reductions in thermal resistance and power-loop inductance were achieved while maintaining integrated electrical isolation within a compact surface-mount format. These findings highlight the importance of package-level design optimisation in enabling the next generation of high-density SiC power converters

References

1 R. Simpson, L. Longo, R. Russo, S. Cataudo and Z. Wei, *"A New Surface-Mount Power Module for Wide Bandgap Power Devices,"* PCIM Europe 2026; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2026.

2 Bhatt, U. Kulsoom, F. Perraud, M. Schulz and L. Gant, *"ISOPLUS - SMPD: An Advanced Isolated Packaging to Fully Exploit the Advantages of SiC MOSFETs,"* PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2023, pp. 1-6, doi: 10.30420/566091117.

3 M. Papaserio et al., *"Modeling and Thermal Analysis of the ACEPACK SMIT Package in H-Bridge High Voltage Circuits,"* PCIM Europe 2022; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2022, pp. 1-6, doi: 10.30420/565822279.

4 ST, *"ACEPACK SMIT module package guidelines for mounting and thermal management."* www.st.com.

5 Infineon, *"IMCQ120R040M2H CoolSiC 1200V SiC MOSFET G2."* www.infineon.com.

6 Nexperia, *"X.PAK SiC MOSFETs: A Technical Guide."* www.nexperia.com.

7 Rogers, *"curamik ceramic substrates."* www.rogerscorp.com.

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