Whitepaper

Use of ESD Protection Devices as 3D Models in Simulations

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The automotive world is currently undergoing significant technological changes that are looking to reshape the future of the industry. One of the most significant developments is the requirement for enhanced connectivity, data transmission, and infotainment options for both the driver and passengers. This demand has sparked a considerable growth in communication protocols, in-vehicle networks, and electric applications in vehicles. Specifically, the importance of high-speed data links like USB, HDMI, and various video applications has grown significantly within this particular context.

High-Speed Applications in Automotive

With the increasing growth of electric systems in cars and the rapid increase in data rates of Ethernet, it is imperative that in-vehicle networks exhibit improved Signal Integrity (SI), electromagnetic compatibility (EMC), and electrostatic discharge (ESD) robustness. In this article, we will explore the impact of a modern ESD protection on the SI using full-wave 3D modeling techniques (Dassualt, 2023). Consequently, the findings will be examined in the frequency domain, specifically in relation to scattering parameters and time domain reflectometry (TDR).

Figure 1 shows a typical configuration of a differential high-speed channel in automotive. In this point-to-point (P2P) configuration, two system PCBs are connected with a shielded cable. A high-speed automotive cable is a shielded twisted pair (STP) or shielded parallel pair (SPP).

The part between the Rx/Tx and the cable is called a medium dependent interface (MDI) containing the traces, DC block, ESD protection, and connector for the STP or SPP. In the following example, we will focus on the role of ESD in the MDI block.

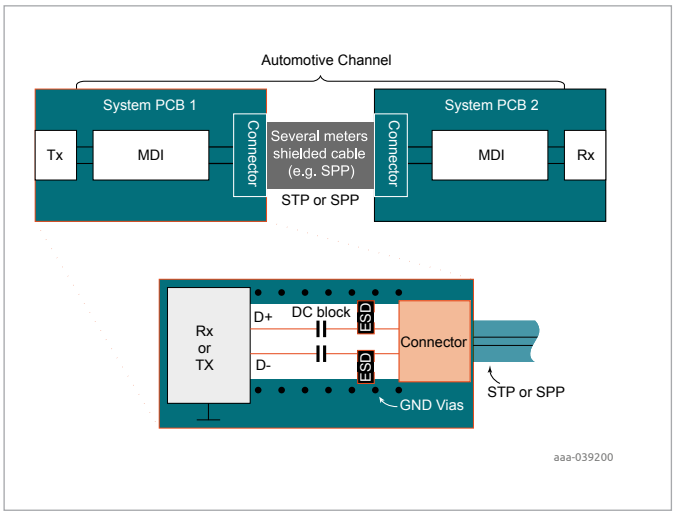

Figure 1: Typical configuration of a High-Speed MDI. Depending on the specific requirements, the position of the ESD protection devices can also be between the high-speed IC and the DC block.

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Simulation Set-up

The investigation is done purely at a simulation level (CST MW Studio), therefore a four layer stack-up PCB with typical dimensions was chosen, see Figure 2. For the sake of simplicity and conserving simulation time, we only used the first two layers (top-layer and GND). The differential lines are routed on the top layer, and the ground is a solid layer without any gaps or openings.

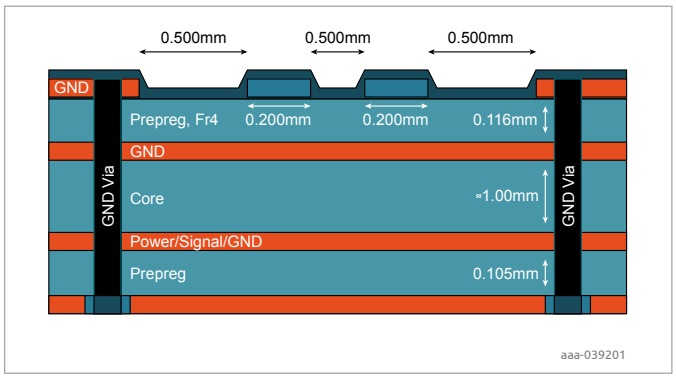

Figure 2: Stack-up of a typical 4-layer PCB. The dimensions were chosen to meet the 100Ω for the microstrip line.

The PCB is 2.5x2.5cm, see Figure 3. Our investigation solely examined the PCB region located between the connector and the PHY, with a particular emphasis on the traces and the consequences of incorporating the ESD protection device into them.

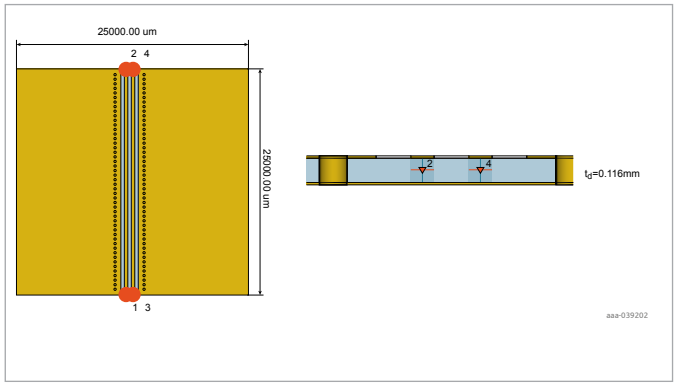

Figure 3: Top view and cross section of the simulated structure in CST

The simulation was performed using discrete, single-ended ports. No external fields were assumed, and the boundary conditions were set to OPEN (add space). All simulations were done using the frequency domain solver. For the prepreg, we used FR4 with ε_r= 4.3 and tanδ = 0.025 at 10GHz. For the conducting material, we used copper with a conductivity of σ=5.8e7 S/m. The TDR was performed in a post-processing step using the S-Parameters and the rise time of the TDR signal was t_r=100ps.

Simulation Results in Frequency and in Time-Domain

The first simulations are focused on the traces only. Here, the microstrip lines are modeled with the dimensions shown in the stack-up, see Figure 2. In order to establish an optimal electromagnetic environment, we incorporated a grounding via a cage in close proximity to the microstrip lines.
The results are shown in frequency and in time domain. The differential scattering parameters (S-Parameters), S_{DD21} are calculated from the single-ended simulation in a post processing step. In Figure 4, we see a typical transmission line behavior, similar to a low-pass filter. The TDR results are showing a small mismatch in the microstrip line. This mismatch is <1Ω and is a reasonable deviation and within the typical manufacturing tolerance of the PCB.

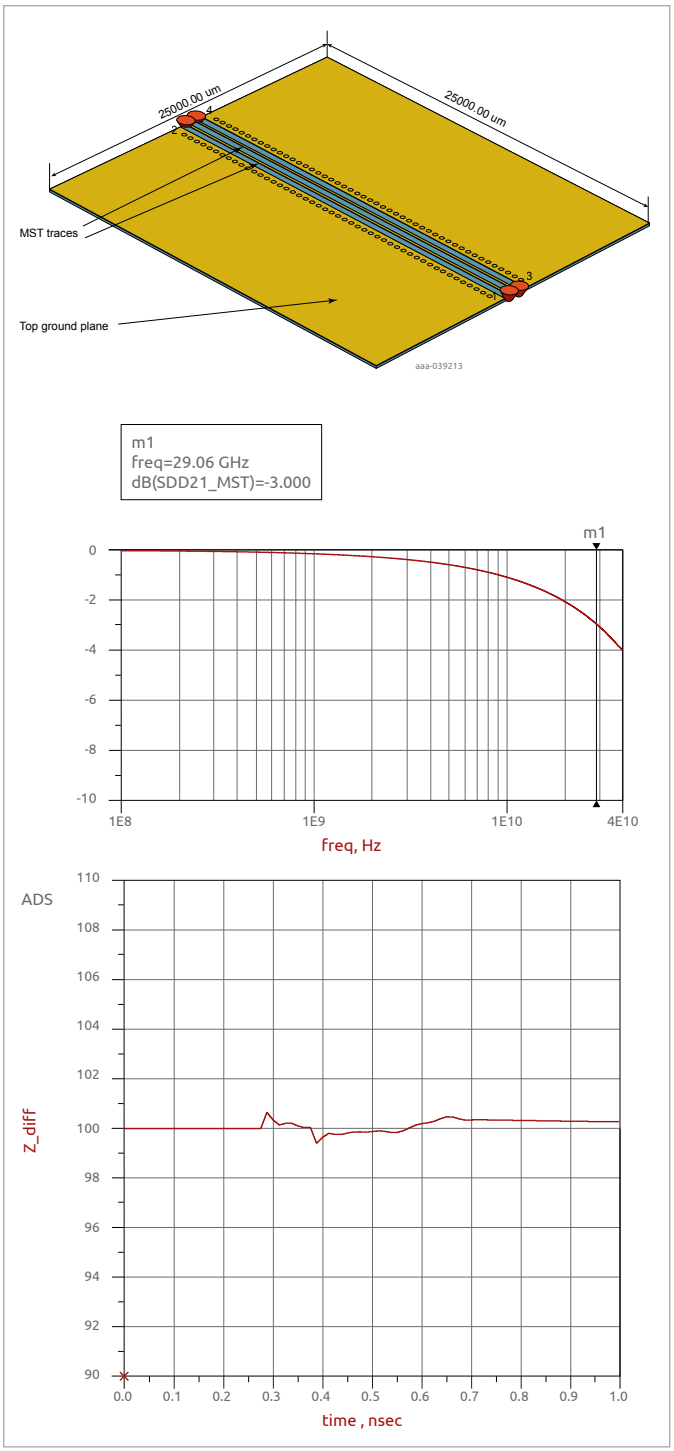

Figure 4: Model and simulation results of the differential transmission lines only.

In the second step, we added a series capacitor and the ESD protection device. It is worth noting the DC caps might show some significant impact on a real application, but within our simulation, an ideal model of a capacitor showed negligible effect, so this element will not be explored further. As an ESD protection device, we added the PESD5V0H1BSF, with roughly 0.15pF. The ESD devices were modeled including the packaging (SOD962), see Figure 5.

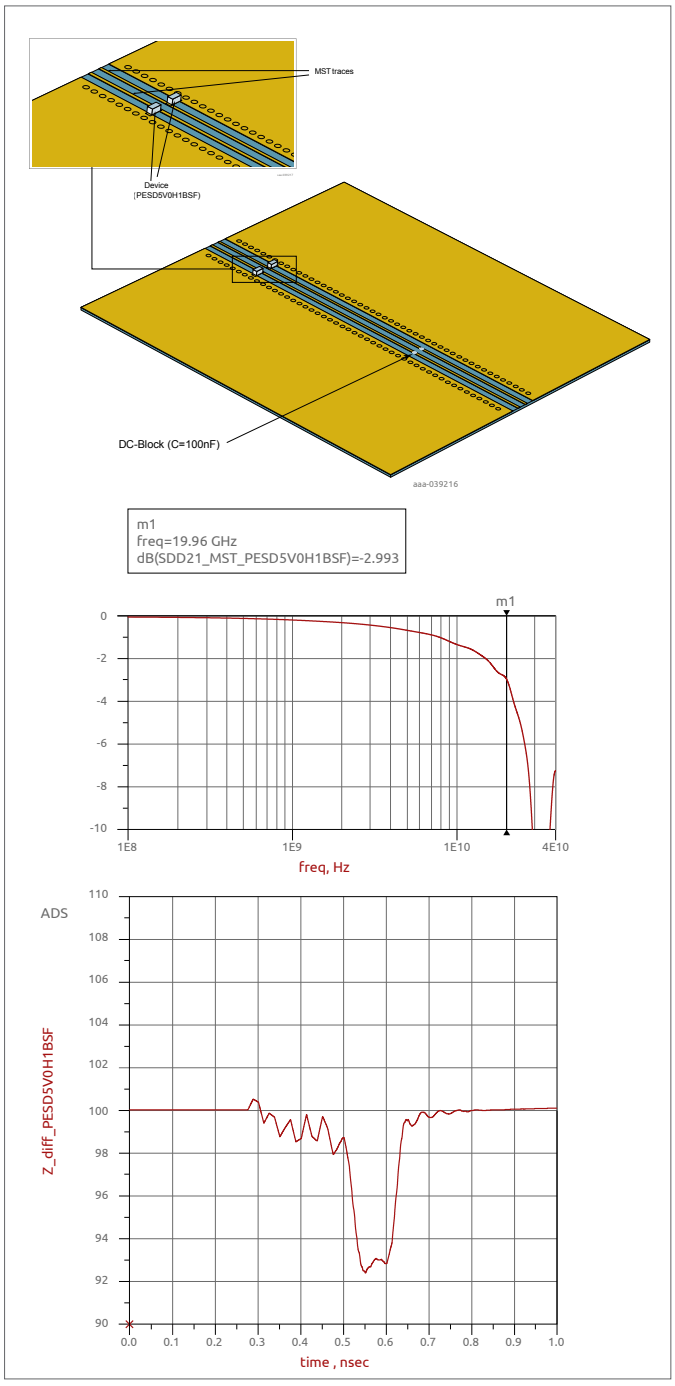

Figure 5: Model and simulation results of the ESD protection device and the DC caps added to the differential traces.

The package was modeled including all package components, such as lead frame, housing etc., including the dimensions and corresponding material parameters. The S-Parameters show a slight reduction in the bandwidth by adding the ESD protection device. In the TDR data, we see that the ESD protection device locally drops the impedance down to ~93Ω, which is typical for ESD protection devices due to their mainly capacitive behavior. In most applications the tolerance window of the impedance along the PCB path is ±10% or even ±15%, which is consistent with the ESD protection device on the line.

Summary/Conclusion

The purpose of this article is to highlight the application of an ESD protection device in a state-of-the-art simulation environment, and the relevance to electronic engineering. Within the simulation environment, the ESD device can be implemented as a full 3D model. All package dimensions and material parameters can be included in the 3D model. The purpose of the analysis is to demonstrate the performance of a portion of the MDI, which includes microstrip lines, DC capacitors, and the ESD protection device. Modeling the ESD protection device as a full 3D model can be highly advantageous, particularly for high-speed interfaces that are sensitive to parasitic elements.

Nexperia offers customers the opportunity to access multiple 3D models for specific ESD packages, and further supports them by facilitating integration into their simulation environment.

References

Dassualt. (20. August 2024). From: www.3ds.com/products-services/simulia/products/cst-studio-suite/

About Nexperia

Headquartered in the Netherlands, Nexperia is a global semiconductor company with a rich European history and over 14,000 employees across Europe, Asia, and the United States. As a leading expert in the development and production of essential semiconductors, Nexperia's components enable the basic functionality of virtually every commercial electronic design in the world – from automotive and industrial to mobile and consumer applications. The company serves a global customer base, shipping more than 100 billion products annually. These products are recognized as benchmarks in efficiency – in process, size, power, and performance. Nexperia's commitment to innovation, efficiency, sustainability, and stringent industry requirements is evident in its extensive IP portfolio, its expanding product range, and its certification to IATF 16949, ISO 9001, ISO 14001 and ISO 45001 standards.

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