Whitepaper

Best practices to protect USB4® data lines
Considering signal integrity and system-level protection aspects

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USB4® SerDes interfaces, operating at 20 Gbit/s, are found in Retimer and SoC ICs. 20 Gbit/s USB4 SuperSpeed signals are sensitive to degradation, and each component of a system carrying 20 Gbit/s signals must limit the amount of attenuation of the signal (also known as insertion loss). USB4 retimer interfaces are connected to the USB Type-C interface receptacle and therefore exposed to external influences such as ElectroStatic Discharge (ESD) strikes. The connected ICs are fabricated at sensitive high-speed silicon nodes with insufficient built-in protection from system-level ESD strikes, so USB4 ICs require the robust protection of specialist external ESD protection devices. These devices must provide sufficient system-level protection without impacting the signal integrity of the USB4 communication link. We will explore best practices for choosing and placing ESD protection devices to ensure high system-level ESD robustness whilst maintaining USB4 signal integrity.

Signal integrity considerations:

USB4 is not simply a minor upgrade to USB 3.x. Doubling the data rate causes significant engineering problems due to the interaction of these high frequency signals with the material properties of the PCB.

Parameter	DDR4	DDR5	USB 3.2 Gen 2	USB4 Gen 3	Units
Data rate	3.3	4.8[2]	10.0	20.0	Gbit/s
Nyquist frequency f1	1.6	2.4	5.0	10.0	GHz
Third Harmonic f3	4.8	7.2	15.0	30.0	GHz
Signal skin depth in copper at frequency f1	1.63	1.33	0.9	0.65	µm
Signal skin depth in copper at frequency f3	0.94	0.77	0.53	0.38	µm
Rise time at transmitter	44.0[3]	29[3]	14.0[3]	10.0	ps
Signal bandwidth at transmitter	8.0[4]	12[4]	25[4]	50.0[4]	GHz

Table 1: Critical signal parameters with significant changes between USB 3.2 and USB4

Table 1 lists several significant differences between USB 3.2 Gen 2 and USB4 Gen 3 parameters, with DDR4 and DDR5 listed for comparison.

The signal bandwidth of USB4 Gen 3 signals is at least twice that of USB 3.2, four times that of DDR5 and six times that of DDR4. With USB4 having significant frequency content at 30 GHz, the designer cannot ignore insertion losses above 10 GHz, causing significant implications for the PCB.

The wide bandwidth of USB4 SuperSpeed signals drives the selection of the PCB material, stack up and PCB routing priorities, especially when the USB Type-C port is more than a short distance from the mother-board SoC host.

If the USB4 SuperSpeed traces are the fastest signals on the PCB, then the engineering team must design the PCB to prioritize USB4 trace requirements, rather than slower signals such as DDR RAM traces.

Attenuation in PCB traces at frequencies of 10 GHz and above has two main components: dielectric dissipation factor (Df) and skin-depth-related losses.

Typically mid and low loss PCB materials have their dielectric dissipation factor specified at 1 or 10 GHz. Table 1 shows that for successful USB4 operation, the design team must select PCB materials which have Dk and Df specifications characterized by the supplier for frequencies above 10 GHz. It is important to obtain real dissipation factor data from potential PCB materials vendors, which may not be published in the manufacturers' data sheet.

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Insertion loss in PCB materials depends heavily on the dissipation factor of the PCB dielectric, and for USB4 this must be sufficiently low at 20+ GHz. Typical FR4 PCB material loss-per-inch is often approximated as 0.1 dB per inch per GHz ([SPIS]), e.g., 0.5 dB at 5 GHz.

Note: This rule of thumb typically does not apply at frequencies greater than 5 GHz.

Further losses are caused by the copper conductor resistance. Skin depth effects cause the series resistance of copper traces to increase with the square root of the frequency. This is simply because there is a smaller volume of copper available for such frequencies to flow through, increasing the resistance. In addition, skin depths below 1 µm, as found at frequencies above 10 GHz, cause high frequency currents to interact with the bumpy crystal structure of the copper foil surface. This increases the path length taken by high frequency currents, as they climb up and down the micron-scale valleys and mountains on the surface of the copper foil. The increased distance to travel for the high frequency (HF) currents results in higher resistance. The copper skin depth of the third harmonic is significantly smaller than the surface roughness peaks of standard copper foil causing increased attenuation, even with higher grades of copper foil.

Standard PCB materials, e.g. FR-4 types, cause significant challenges for signals over 10 GHz such as USB4 and are typically not characterized for operation over 10 GHz. It is possible to use low- cost, standard PCB materials, especially when using a high performance Kandou retimer for signal conditioning but only when trace length requirements are modest and there is Df data available from the chosen PCB material vendor for operation above 10 GHz.

Signal integrity budgets

The USB4 Gen 3 specification includes an informative host insertion loss specification of 7.5 dB. This value of loss assumes an end-to-end total loss of 22.5 dB, as illustrated in Fig. 1.

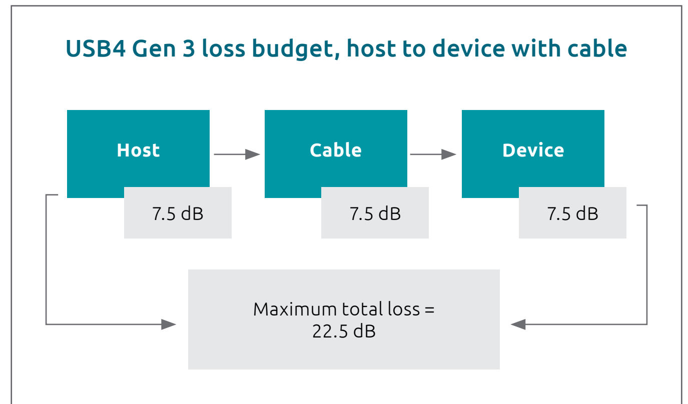

Fig. 1: USB4 link from host to device with loss requirements at 10 GHz for Gen 3

Note: Insertion loss recommendations for USB4 Gen 3 are specified at 10 GHz.

Measurements by Kandou show an average of an additional 8 dB attenuation at 20 GHz compared to 10 GHz using VT-47[1] at 0.85 mm Prepreg thickness with 150 µm microstrip traces. It is important that the channel does not exhibit too much loss at 20 GHz. A channel can comply with loss requirements at 10 GHz but still fail due to excessive ISI caused by too much high frequency attenuation.

Designers must ensure that PCB materials are specified for operation above 10 GHz, and that Df specifications given are also valid at 20 GHz+.

The total retimer-to-USB-C® receptacle loss budget must include any losses due to the IC die + package, discrete components (e.g. electrostatic discharge (ESD) diode) and the solder connection to the USB Type-C receptacle. These component losses reduce the loss budget available for traces and therefore reduce the maximum possible trace length. Typical component losses for the retimer-to-USB-C link segment are illustrated in Fig. 2.

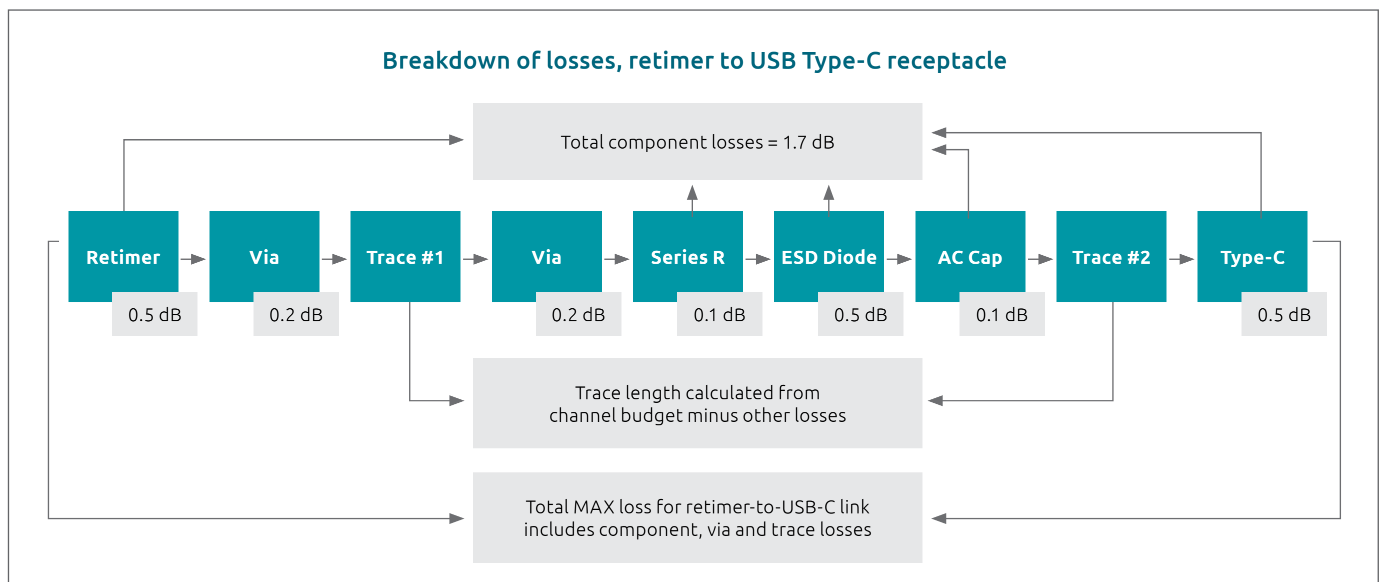

Fig. 2: Host component losses

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The USB4 host insertion loss specification is informative and not part of the USB4 Compliance Test Specification.

The USB-IF expects that hosts which comply with the recommended 7.5 dB host insertion loss budget will be able to pass the mandatory TX eye and RX BER tests. A host is USB4 compliant if it passes the electrical compliance tests, even if the host insertion loss is greater than 7.5 dB.

Kandou retimers tolerate greater channel losses, up to 26 dB over the host-cable-device link. This allows system designers to extend retimer-to-USB-C trace length according to the recalculated trace loss budget illustrated in Fig. 3.

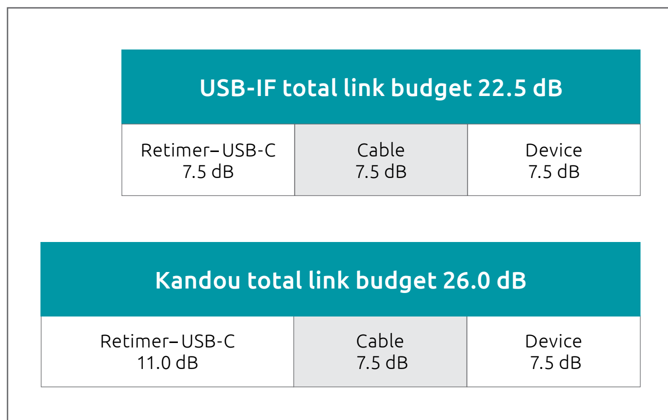


Fig. 3: Increasing host insertion loss tolerance with a Kandou retimer

The maximum possible trace length depends on the trace insertion loss budget. The total insertion loss of the retimer-to-USB-C channel is the sum of the component, trace and via losses:

$$\text{Link_budget} \geq \text{Loss}_{components} + \text{Loss}_{traces} + \text{Loss}_{vias}$$

Designers must therefore subtract component and via losses from the total link budget in order to derive a trace insertion loss budget. Designers should derate the trace insertion loss target by 20% to account for the increase in insertion loss due to transmission line trace geometry variations caused by manufacturing tolerances.

This derating applies to the traces, not the vias, so the total trace budget is therefore calculated as:

$$\text{Trace_budget} = 0.8(\text{Link budget} - \text{Loss}_{components} - \text{Loss}_{vias})$$

The maximum complete channel insertion loss, from retimer to USB-C receptacle, is calculated as:

$$\text{Loss}_{Retimer\text{-}USB\text{-}C} = 0.8\,(\text{Link_budget} - \text{Loss}_{components} - \text{Loss}_{vias}) + \text{Loss}_{components} + \text{Loss}_{vias}$$

PCB layout electromagnetic simulations are expected to include insertion loss of vias and components, but these losses must be excluded from the trace loss budget used for trace length calculations. This document assigns 0.4 dB of worst-case via loss to account for a typical design with two vias per trace.

Designers can substitute the USB4 host insertion loss specification or the Kandou host insertion loss capability into the trace loss budget calculation.

$$\text{Trace_budget} = 0.8\,(\text{Link_budget} - \text{Loss}_{components} - \text{Loss}_{vias})$$

$$\text{Trace_budget(USB4 spec)} = 0.8\,(7.5 - 1.7 - 0.4) = 4.3\text{ dB}$$

$$\text{Trace_budget(Kandou limit)} = 0.8\,(11 - 1.7 - 0.4) = 7.1\text{ dB}$$

Fig. 4 shows a graphical representation of these channel loss budgets. Table 1 presents the trace loss budget calculation results for both USB4 specification and Kandou capability calculations.

Fig. 4: Composition of host insertion loss budgets, USB4 specification vs. Kandou capability

Host insertion loss budget source	Total host budget includes all sources of loss	Trace loss budget excluding vias, with guard band
USB4 informative specification	7.5 dB	4.3 dB
Kandou capability	11 dB	7.1 dB

Table 2: Host and trace insertion loss budget summary

The maximum possible trace length for a USB4 host PCB design can be determined after the designer has calculated the trace loss budget. The maximum PCB trace length is given by:

Trace length ≤ Trace budget / Loss per unit length

The insertion loss per unit length of the trace depends on the PCB material (Df and copper roughness) and the transmission line design. Electromagnetic simulation of the design is strongly recommended to validate the layout before commencing PCB manufacture. To prevent costly PCB iteration, designers should select a PCB material and stackup that result in a loss-per-unit-length that meets the design requirements. Layout engineers must ensure that the trace length, multiplied by the insertion loss per unit length, is within the derated trace loss budget. This proposed design process is illustrated in Fig. 5:

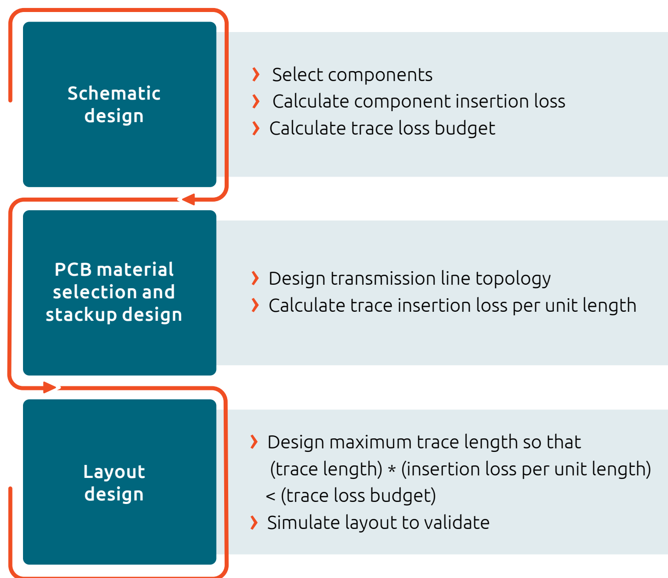


Fig. 5: Design process

Note: USB4 Gen 2 requirements

This app note has focussed on the insertion loss requirements of a USB4 Gen 3 host at 10 GHz. USB4 Gen 2 rates have recommended insertion loss specifications at 5 GHz (see Table 3). Typical characteristics of standard PCB materials are that the loss per unit length in dB doubles if the frequency doubles, so targeting the 10 GHz USB4 Gen 3 requirement is recommended. Products that pass Gen 3 electrical compliance are expected to also pass Gen 2 compliance, but the reverse may not be true.

Router Assembly Support	Insertion Loss Limit (Informative)
USB4 Gen 3	< 7.5 dB at 10 GHz
USB4 Gen 2	< 5.5 dB at 5.0 GHz
USB 3.2	< 8.5 dB at 5.0 GHz

Table 3: Host insertion loss specifications from USB-IF

System-level protection considerations

Although the USB PD specification offers several safety features[1], a key issue of concern for USB designers is how to protect the interface in the event of the V_{BUS} supply lines coming in electrical contact with data lines due to out-of specification connectors or systems. Providing adequate protection is further complicated by the stipulation in the latest USB 4 standard that SuperSpeed line pairs must be AC-coupled. The pinout for the USB Type-C connector is shown in Figure 6.

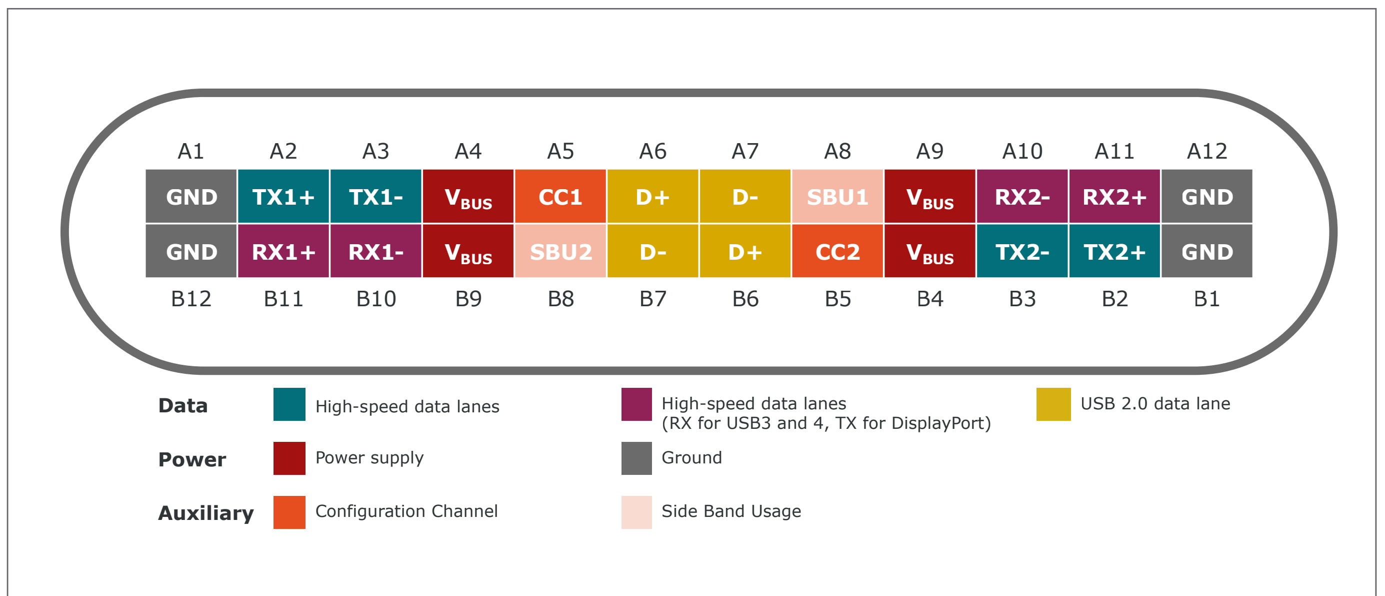


Fig. 6: Pinout of the USB Type-C Interface

Figure 7 shows two alternative locations where ESD protection diodes in AC-coupled SuperSpeed lines can be placed - either behind the connector (POS_USB-C) or between the AC coupling capacitors and the protected transceiver IC (POS_IC).

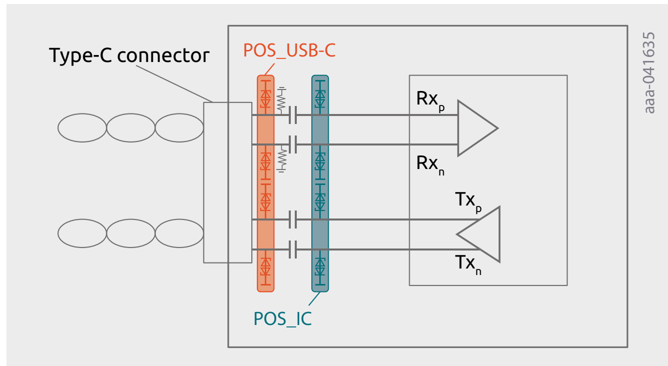


Fig. 7: Two options for locating ESD protection diodes in SuperSpeed data lines

Investigating the impact of ESD stress on AC-coupling capacitors

Initial investigations focused on how ESD stress impacted the AC-coupling capacitors, since placing protection diodes in POS_IC renders them unprotected against ESD events.

Various 0402" AC-coupling capacitors commonly used in Nexperia designs[4] all provided adequate ESD robustness when subjected to a transmission line pulse (TLP) with 100 ns duration and 1 ns rise time (1/100 ns). In these tests, the 330 nF capacitor showed no signs of damage up to ~60 A TLP, while for the 220 nF capacitor, no damage was seen up to ~55 A TLP (roughly equivalent to a ~30kV and ~27kV IEC 61000-4-2 pulse, respectively).

25 V-rated 220 nF 0201" AC-coupling capacitors from two manufacturers were also evaluated. The results of measurements are shown in Figure 9. Firstly, a robustness limit was established (blue trace) before a new device was stressed five times with 1/100 ns TLP pulses up to 22 A (below the robustness limit). This device did not show any degradation during these runs. Similarly, for the more robust capacitor from the second manufacturer (Figure 8), five runs of up to 25 A 1/100 ns TLP did not result in any device degradation.

Sample capacitors from both manufacturers were subsequently tested using very-fast TLP (vfTLP) with 5 ns duration and a 600 ps rise time (0.6/5 ns) up to 120 A (Figure 10), and these results also did not reveal any signs of device degradation.

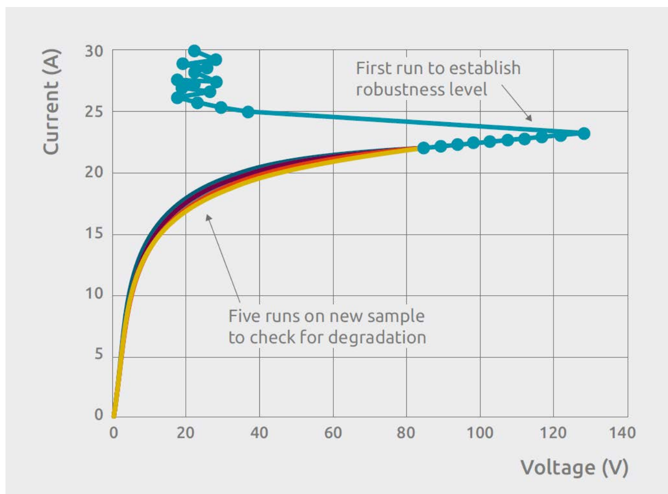


Fig. 8: Measurement results on the less robust 0201" coupling capacitor

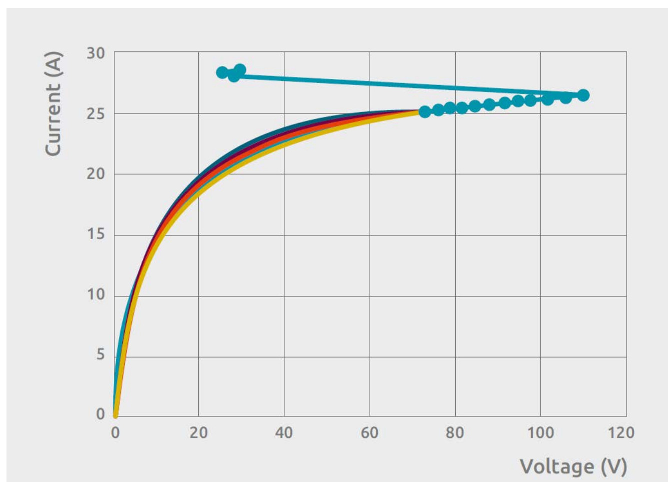
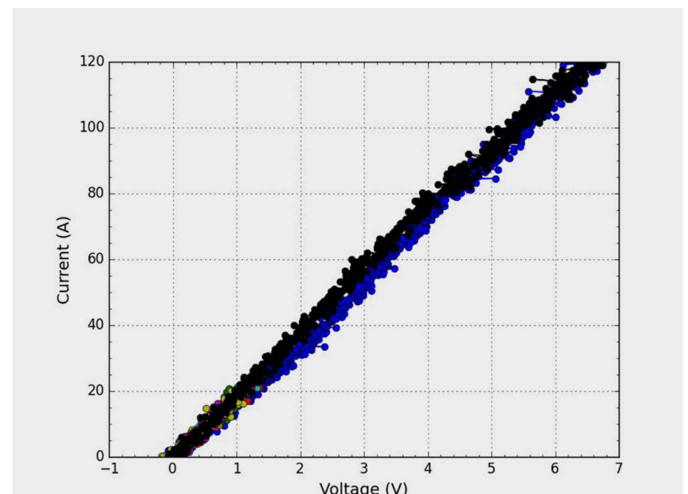


Fig. 9: Measurement results for the more robust 0201" coupling capacitor



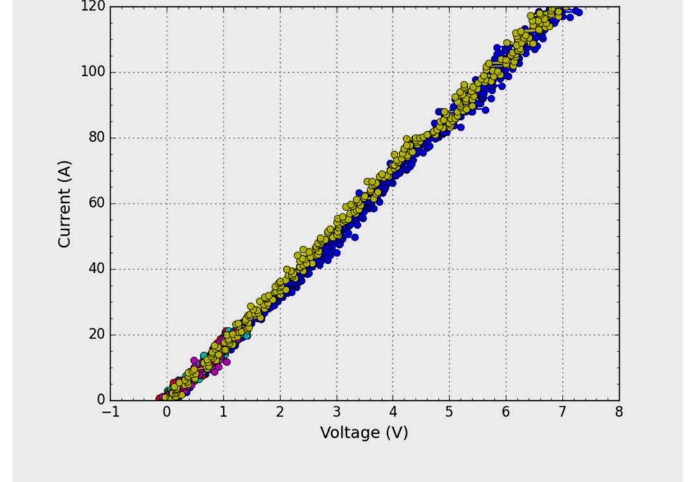


Fig. 10: Testing two 25 V-rated 220 nF 0201 capacitors with 0.6/5 ns very-fast TLP up to 120 A

Since investigations showed the AC-coupling capacitors to be robust up to 120 A 0.6/5ns very-fast TLP, it can be concluded that degradation due to an ESD pulse happens because of the energy content rather than the peak voltage. This allows the 22 A 1/100 ns TLP trials to be viewed as equivalent to an 11 kV IEC 61000-4-2 pulse. In other words, the robustness of all investigated AC-coupling capacitors exceeded level 4 of an IEC 61000-4-2 contact discharge.

During these tests, a discharge resistor avoided a possible accumulation of charge.

Investigating the impact of ESD stress on the protected IC

Nexperia investigated several transceiver ICs (re-timer and re-driver devices) used in SuperSpeed data lines and found that their TLP characteristics closely resemble those of a forward-biased diode in series with a resistor (Figure 11). This means that the on-chip ESD protection of these ICs becomes conductive at very low voltages (between 1 V and 1.5 V). Therefore, any external ESD protection diodes used must have a low trigger voltage to limit the ESD current flowing into the protected IC before damage occurs.

In summary, investigations on several SuperSpeed transceiver ICs showed:

- On-chip ESD protection typically turns on at around 1 V
- On-chip ESD protection of the example above is damaged at 2 A 1/100 ns TLP
- On-chip ESD protection of this IC is damaged at approximately 5 A for a 0.6/5 ns vf-TLP pulse

The higher vfTLP current damage level indicates that the IC is more sensitive to pulse energy than the peak clamping voltage.

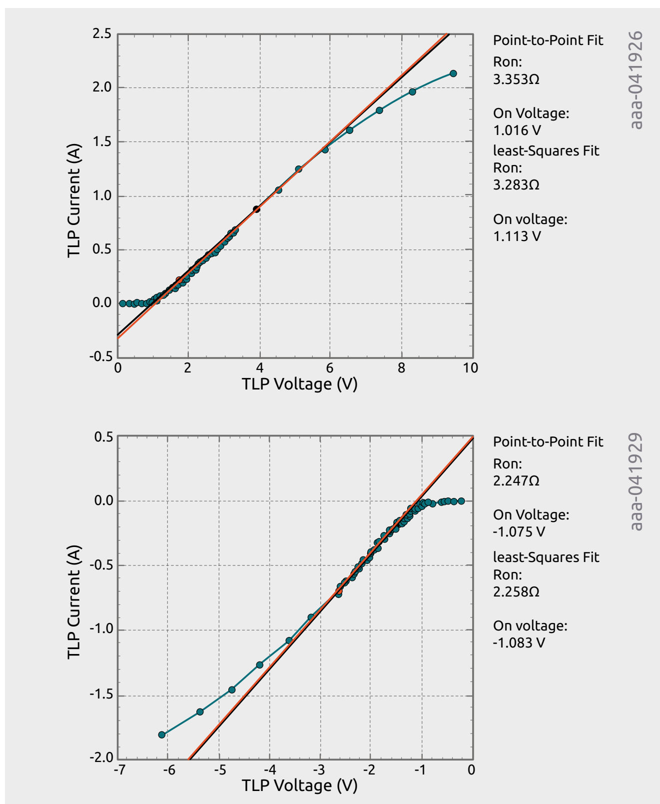


Fig. 11: 1/100 TLP results of a typical USB SuperSpeed IC shows on-chip protection becomes conductive at ~ 1 V.

The previously described IC is sensitive to residual clamping after ESD protection. Nexperia also tested systems capable of withstanding up to 6 A TLP. However, these systems still begin conducting around 1 V and start shunting transients. To assess how such systems respond to different ESD protection strategies, SEED (System-Efficient ESD Design) simulations were complemented with measurements on test boards, comparing high-voltage protection diodes placed at POS_USB-C versus low-voltage diodes at POS_IC, using the test setup shown below[3].

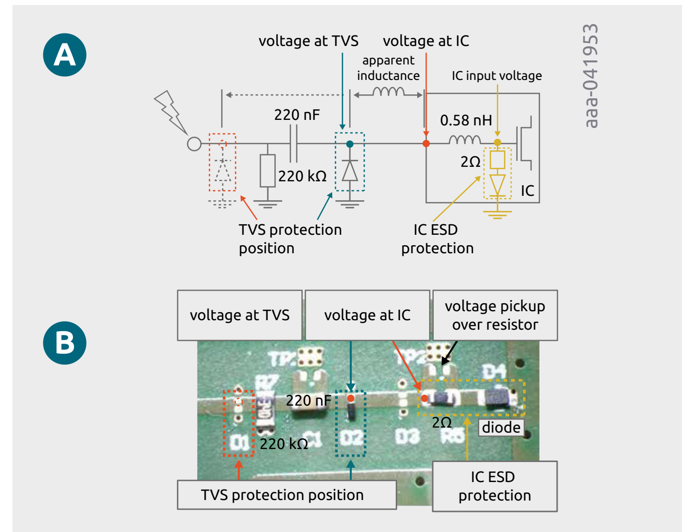


Fig.13: Test interface for an AC-coupled SuperSpeed data line with, from left to right: connector (not shown), ESD footprint for POS_USB-C, pull-down resistor, AC-coupling capacitance, ESD footprint for POS_IC, IC replacement circuit (resistor plus diode).

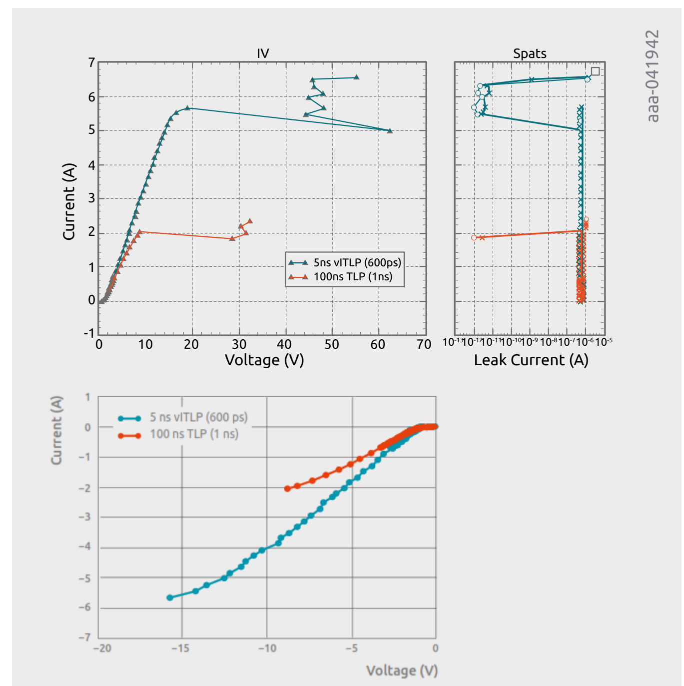


Fig. 12: Leakage current measurements checking for damage to on-chip ESD protection structures

Four different ESD protection devices with a 1 V rating (1–4) were placed in POS_IC and two 18–24 V-rated ESD protection devices (5–6) were placed in POS_USB-C. The results are shown in Figure 14. The dashed line shows the curve of the IC ESD protection model.

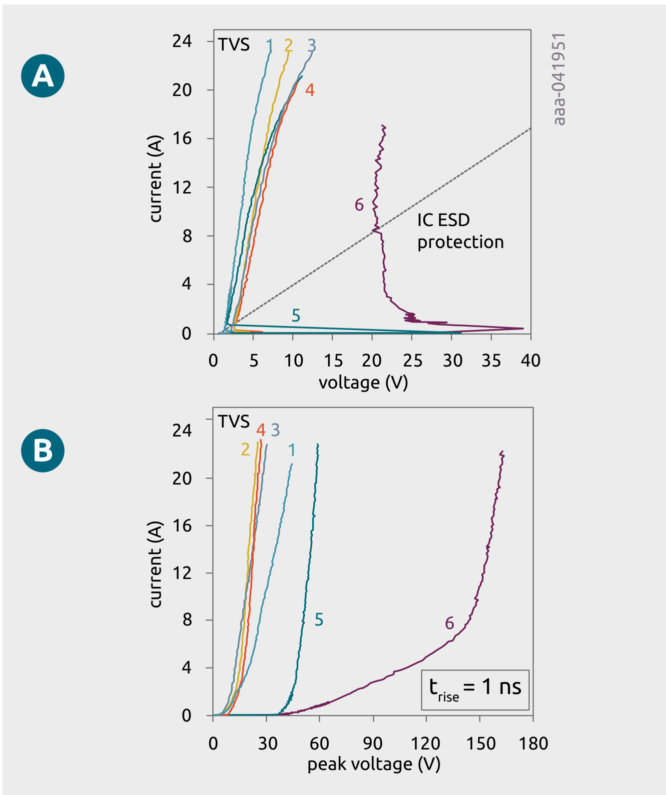


Fig.14: Comparison of TLP curves (A) and peak clamping voltages (B) for ESD protection diodes with 1 V rating (1–4)

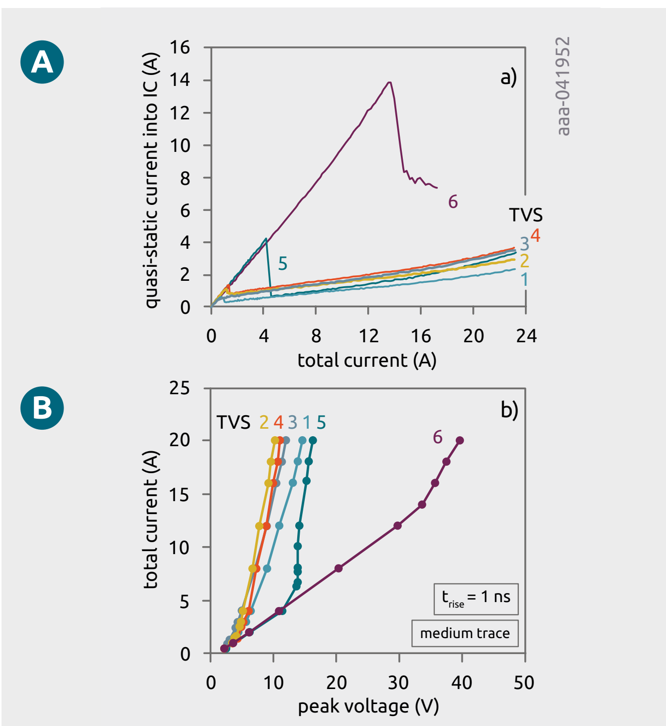


Fig.15: TLP current (A) and peak voltage (B) seen by the transceiver IC

Device 5 could potentially protect transceivers that can survive more than 4 A TLP flowing into it before the device triggers, but the IC shown in Figure 11 and 12 would not be able to survive this type of pulse. In any case, the overall transient current stress to the IC for all four protection devices in POS_IC is significantly lower compared to POS_USB-C.

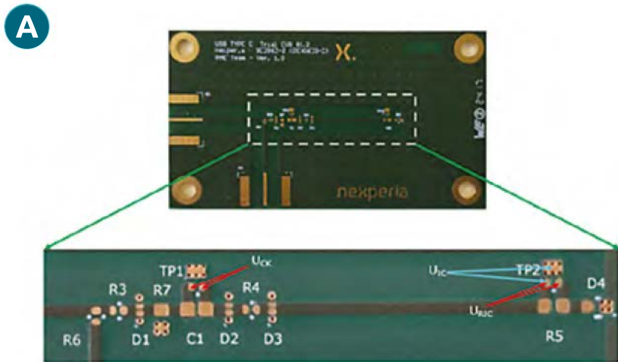
These results demonstrate that using a low-voltage protection diode in POS_IC offers better system-level ESD protection, since the device begins to protect the transceiver while a significantly lower transient current is flowing through the IC.

Independent of the discussion above, maximising the available trace length between ESD protection device and protected IC will maximize system-level protection due to the increased trace inductance and resistance. Therefore, mounting the ESD protection as close as possible to the USB-C receptacle is recommended.

Mounting the ESD protection in position POS_IC slightly reduces protection-to-IC trace length (and inductance) compared to POS_USB-C. However, mounting the ESD protection in this position POS_IC (AC coupled) allows a protection device with a very low trigger voltage to be used, compared to using position POS_USB-C (DC coupled) which requires a very high trigger voltage Vt1 > V_{bus} if a short circuit condition to V_{bus} is possible. Such high trigger voltages allow a significant ESD current to flow into the IC until the external ESD protection starts to protect the IC. System protection is best with low trigger voltage protection devices in position POS_IC.

Does the AC-coupling capacitor protect against short circuits?

The short answer to this question is that AC-coupling capacitors do not provide reliable protection against short circuits of V_{BUS} to the SuperSpeed data lines. Detailed investigations have shown that when a short-circuit is applied (or removed), a transient can pass through the AC-coupling capacitor and expose the IC to surge pulses lasting in the μs range. For this evaluation[4], a test board with the IC representation circuit as described in the ESD tests previously was used.



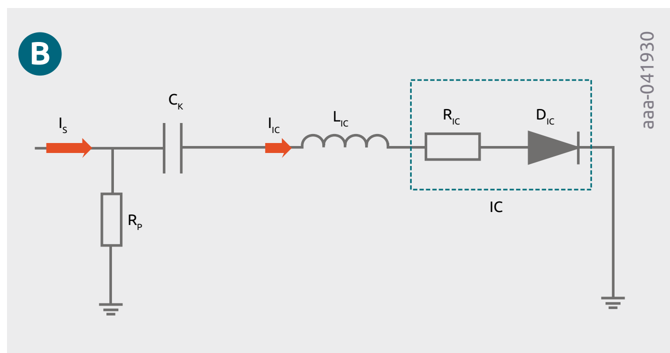


Fig. 16: (A) Test PCB using the elements of a SuperSpeed line and test points. (B) Measurement setup with either high-voltage ESD in POS_USB-C or no ESD protection

The short-circuit was applied using a signal generator driving a MOSFET, giving a rise time duration of ~ 50 ns (Figure 17)

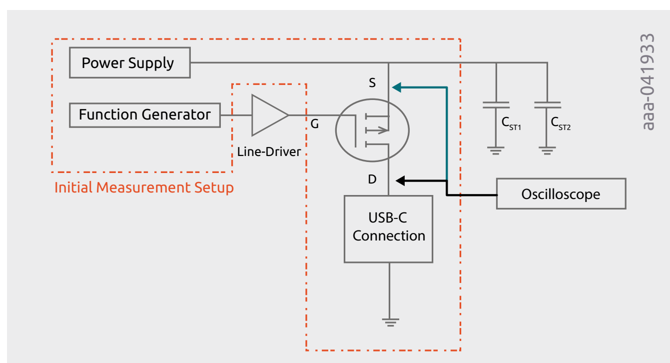


Fig. 17: Short-circuit driving circuit

As shown in Figure 18, various waveforms result from the application of this type of short circuit. The signals at the input (U_input) rise to 20 V with a rise time in the order of tens of nanoseconds, while the rise time of the voltage drop over the AC-coupling capacitor (U_ck) depends on the capacitance value, as expected. The duration of the voltage drop over the IC replacement circuit (U_IC) also depends on the capacitance value, with both resulting in a surge pulse in the range of 1 μs.

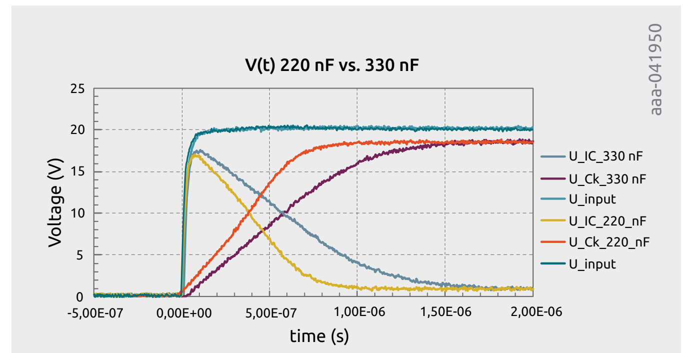


Fig.18: Voltage waveforms for a 20 V short circuit applied to an AC-coupled SuperSpeed line with either a 220 nF or 330 nF capacitor.

In the next step we would like to investigate how the transient current of the short circuit event is shared between the protected IC and the ESD protection device. Again, a MOSFET has been used to apply a 20 V short circuit to the test circuit. The result can be seen in Figure 19:

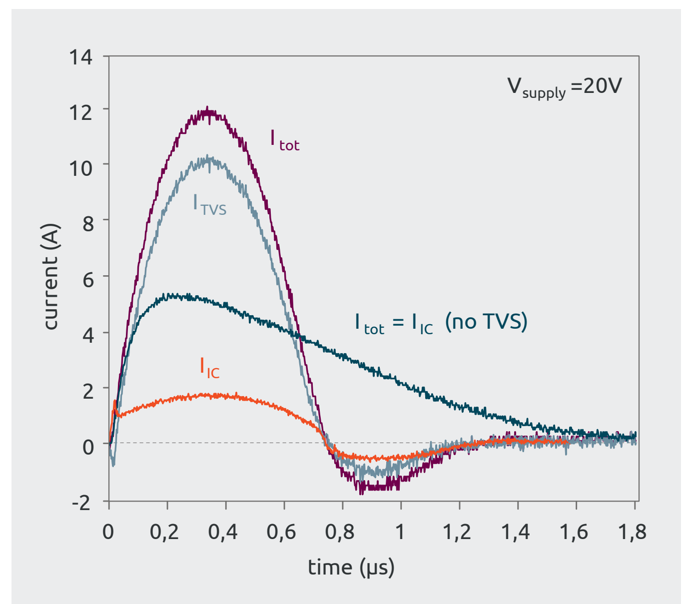


Fig. 19: Transient current flowing through the IC replacement circuit and ESD protection (TVS) after applying a 20 V short circuit to the test setup. The shorter oscillation frequency of the protected case is caused by the triggered ESD protection lowering the system resistance, which changes the behaviour from an overdamped to an underdamped RLC circuit.

The green curve represents the I(t) behaviour of the IC replacement circuit without external ESD protection (no TVS) or a high-voltage protection in POS_USB-C. A surge pulse of this current level is highly likely to damage the IC.

Adding an ESD protection device to the circuit will give two current paths, one through the ESD protection device (I_{TVS}, blue-grey), and one through the IC replacement circuit (I_{IC}, orange line). The total current flowing through both is shown in the violet line.

The total current of the protected solution is significantly higher due to the lower system resistance, however, the current flowing through the protected IC is nevertheless lower. This means that the ESD protection device will have to dissipate this additional current on top of the current reduction through the protected IC.

The resulting signal is a damped oscillation. The whole setup can be replaced by an RLC circuit with L being the parasitic inductance of the test setup, C the value of the AC coupling capacitance and R the total resistance.

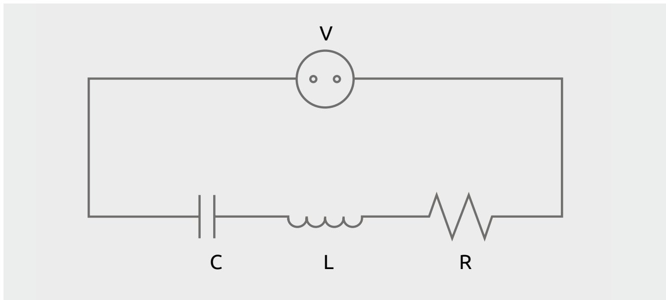


Fig. 20: RLC circuit

The resonance frequency of a LC circuit is given by:	$\omega_0 = \frac{1}{\sqrt{LC}}$
The behaviour of an RLC circuit is defined by the ratio between system resistance and -inductance:	$\alpha = \frac{R}{2L}$
The circuit will be overdamped if:	$\frac{R}{2L} > \frac{1}{\sqrt{LC}}$
In contrast, an underdamped circuit will result if:	$\frac{R}{2L} < \frac{1}{\sqrt{LC}}$

By triggering the ESD protection of the protected circuit, the resistance of the system will be significantly reduced since the internal resistance of the protected IC should be notably larger than the resistance of the ESD protection device to ensure that most of the transient pulse will flow through the ESD protection device. This is changing the pulse response of the test board from an underdamped to an overdamped system.

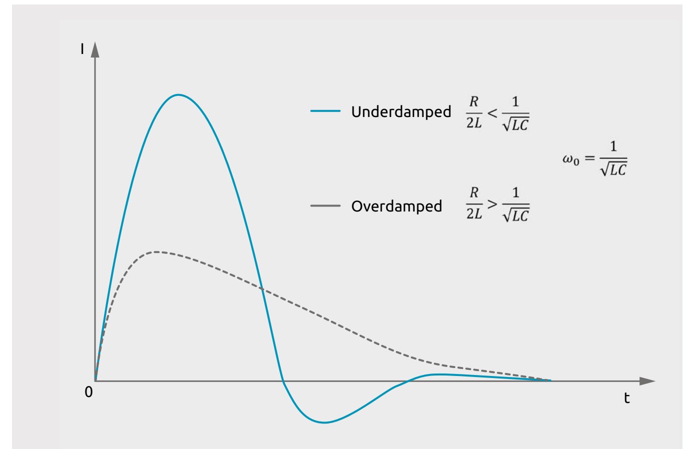


Fig. 21: Triggering the ESD protection will reduce the total system resistance. This can change the system response to a short circuit from an over-damped to an under-damped oscillation.

The investigations should be taken as a qualitative description of the investigated test setup. Since the behaviour depends notably on the system resistance and - inductance, the behaviour of individual PCBs and systems with different values will differ.

In any case, a step-pulse short circuit applied to an AC coupled data line will create a significant surge pulse to be clamped by the ESD protection device, placing a high focus on surge robustness for the protecting device.

Conclusion

The ESD robustness of investigated AC-coupling capacitors used in SuperSpeed USB interfaces exceeded the equivalent of IEC61000-4-2 level 4 contact discharge and are unlikely to be the weak link in system-level protection. Instead, the protected transceiver IC is more likely to fail, due to the high clamping voltages imposed by suboptimal ESD protection strategies.

A comparison of protection strategies reveals that placing a high-voltage ESD diode (>20 V) at POS_USB-C (further from the IC) results in large and long-duration surge currents during short-circuit events (e.g., ~7 A for 1 µs at 20 V V_{BUS}). This level of stress exceeds what many ICs can survive, even if the ESD protection itself remains intact.

Using a low-voltage (~1 V) ESD diode at POS_IC (between AC coupling C and transceiver IC) significantly reduces the magnitude and duration of the surge current of a surge event resulting from applying a V_{BUS} short circuit to an AC coupled data line. In our investigations, it provided superior protection during both ESD and short-circuit events. Transient currents can be reduced even further by inserting a small series resistor, though this must be balanced against RF performance.

While this placement contradicts traditional advice to maximize the distance between IC and ESD protection (to utilize trace inductance), the benefits of a low-voltage device at POS_IC clearly outweigh the traditional advantages of longer trace lengths, compared to high-voltage protection in POS_USB-C.

Our key recommendation is to use low-voltage ESD diodes at POS_IC for robust protection, especially in systems where short circuits to V_{BUS} are possible.

With USB Power Delivery EPR enabling up to 48 V V_{BUS}, the importance of effective low-voltage protection becomes even more critical.

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Kandou AI is a fabless semiconductor design company dedicated to advancing high-speed, longer reach, low power connectivity solutions. Leveraging its differentiated interconnect IP and system design capabilities, Kandou AI builds high-performance connectivity products for its customers across datacenter infrastructure, AI and consumer electronics with over 20M silicon units shipped using its technology. Kandou AI is headquartered in Saint-Sulpice, Switzerland, with offices worldwide.

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