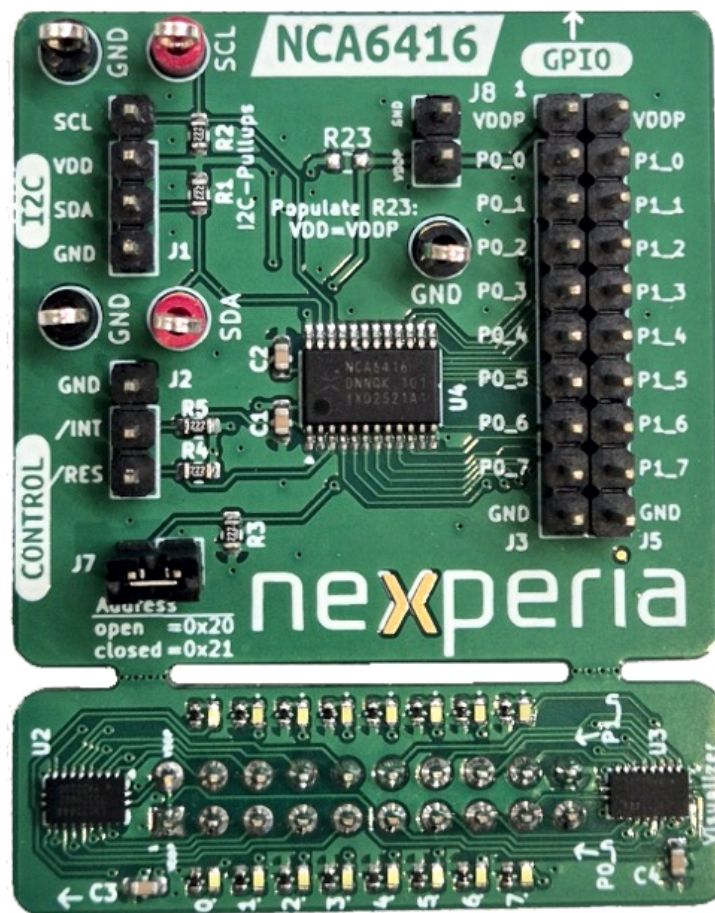




## NEVB-NCA6416 Low-voltage translating 16-bit I<sup>2</sup>C-bus/SMBus I/O expander evaluation board



**Abstract:** The NCA6416 Evaluation Board (EVB) is designed to evaluate the Nexperia NCA6416 I<sup>2</sup>C-controlled 16-bit general-purpose I/O expander. It allows seamless prototyping, verification, and validation of I<sup>2</sup>C-based GPIO control applications. The board includes convenient headers for interfacing, configurable pull-up resistors

**Keywords:** I<sup>2</sup>C GPIO Expander, Evaluation Board (EVB), Fast Mode, 400 kHz, Schmitt-Trigger Inputs, RESET, INT

## 1. Introduction

The NEVB-NCA6416 is an evaluation board (EVB) designed for the NCA6416 I<sup>2</sup>C-controlled 16-bit GPIO expander. The EVB is shipped in an ESD-safe bag with labeling. It provides test points for I<sup>2</sup>C lines and GND, headers for GPIOs, configuration jumpers, and pull-up resistor networks for quick prototyping.

The NCA6416 is a general-purpose I/O expander that provides 16-bit GPIO ports controlled via the I<sup>2</sup>C interface. It includes a configurable interrupt output for monitoring input changes.

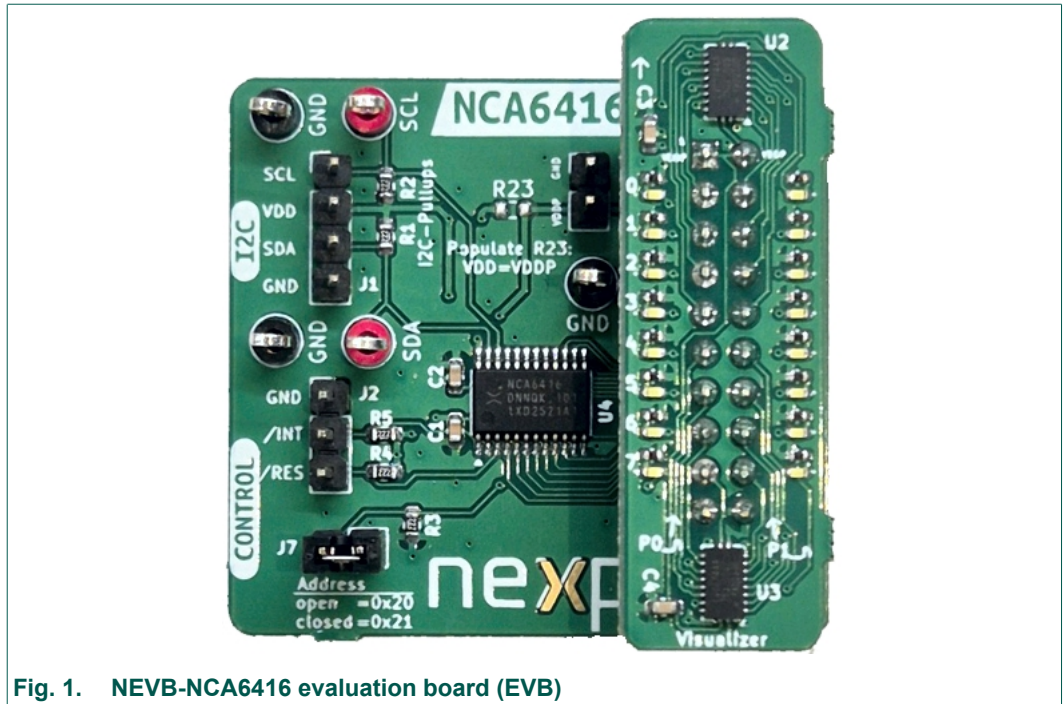


Fig. 1. NEVB-NCA6416 evaluation board (EVB)

### 1.1. Features

- EVB name = NEVB-NCA6416
- Device = NCA6416
- I<sup>2</sup>C-bus to parallel port GPIO expander
- Input voltage = 1.65 V to 5.5 V
- 16 GPIO pins, individually programmable as input or output
- Push-pull and open-drain output options
- Current drive capability = ±25 mA (ideal for LEDs)
- I<sup>2</sup>C interface, compatible with SMBus standards
- Fast-Mode 400 kHz
- 5.5 V tolerant inputs
- 1 address pin allowing up to two devices on the I<sup>2</sup>C-bus
- Active LOW reset input and open-drain INT output
- Supports partial power-down applications
- Glitch free powerup
- No specific power up sequence required

Further details about the specification and parameters of NCA6416 can be found in its data sheet, but a high-level summary is provided in [Table 1](#):

Table 1. Low-voltage translating 16-bit I<sup>2</sup>C-bus/SMBus I/O expander features

Device	Package	Feature
NCA6416PW	TSSOP24	Low-voltage translating 16-bit I <sup>2</sup> C-bus/SMBus I/O expander
NCA6416BY	HWQFN24	

## 2. Hardware setup

The following sections describes the EVB jumper and header description.

### 2.1. Headers J1/J2/J3/J5/J6/J7/J8

Header J1 is for connecting I<sup>2</sup>C interface to NCA6416. J2 is for signals /RESET and /INT pins. J7 is for address configuration. J3 & J5 are to access all 16 GPIO ports and J6 helps to dock the visualizer board strip to J3 & J5 so that GPIO control can be visualized using LEDs. J8 helps to connect VDDP supply voltage when visualizer is docked.

A detailed description of the header pinouts is provided in the tables presented below:

**Table 2. J1 header**

J1 net name	Pin number	Description
SCL	1	SCL I <sup>2</sup> C bus signal line
VDD	2	Supply voltage of I <sup>2</sup> C-bus. Connect directly to the VDD of the external I <sup>2</sup> C master.
SDA	3	SDA I <sup>2</sup> C bus signal line
GND	4	GND connection

**Table 3. J2 header**

J2 net name	Pin number	Description
GND	1	GND connection
/INT	2	Interrupted output. $\overline{\text{INT}}$ pins are both pulled up to VDD using onboard 2.2 k $\Omega$ resistor (R5)
/RES	3	Active Low reset input. $\overline{\text{RESET}}$ pin is pulled up to VDD using onboard 2.2 k $\Omega$ resistor (R4). To trigger $\overline{\text{RESET}}$ , connect to GND test point manually and release to VCC.

**Table 4. J3 and J5 headers**

J3 and J5 net name	Pin number	Description
VDDP	1	Supply voltage of NCA6416 for Port P
J3 → P0_0 to P0_7 J5 → P1_0 to P1_7	2 to 9	16 GPIO port pins on port 0 (J3) and port 1 (J5)
GND	10	GND connection

**Table 5. J6 socket (visualizer socket)**

J6 net name	Pin number	Description
VDDP	1, 2	Supply voltage of NCA6416 for Port P, supply voltage to octal buffers U2 and U3
P0_n	3, 5, 7, 9, 11, 13, 15, 17	LED inputs through octal buffers. Gets connected to P0_n ports of J3 when visualizer is docked on J3
P1_n	4, 6, 8, 10, 12, 14, 16, 18	LED inputs through octal buffers. Gets connected to P1_n ports of J5 when visualizer is docked on J5
GND	19, 20	GND connection

**Table 6. J7 header**

J7 net name	Pin number	Description
ADDR	1	Address pin of NCA6416
VDD	2	VDD pin of NCA6416. Connecting pin 1 and pin 2 configures 0x21 I <sup>2</sup> C target address whereas opening the jumper configures 0x20

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**Errata:** Important note on ADDR pin (address selection):

On this EVB, the ADDR pin is connected to VCCI. However, ADDR is internally referenced to VCCP, and must meet logic level thresholds relative to VCCP:

$$V_{IH} \text{ (High): } \geq 0.7 \times VCCP$$

$$V_{IL} \text{ (Low): } \leq 0.3 \times VCCP$$

Therefore, if you use  $VCCI < 0.7 \times VCCP$ , the device may incorrectly interpret ADDR = LOW, even when VCCI is HIGH.

**Recommendation:**

For full address logic compatibility across all voltage combinations, tie ADDR to **VCCP** in your system or modify the EVB accordingly by connecting ADDR pin to VCCP using a wire.

**Table 7. J8 header**

J8 net name	Pin number	Description
GND	1	GND connection
VDDP	2	Supply voltage of NCA6416 for Port P, helps to access the VDDP pin when visualizer is docked

## 2.2. Test points

There are 5 test points. Two Red and 3 Black. The red test points are labelled SCL and SDA for probing upstream I<sup>2</sup>C bus signals. The rest of the three black test points are connected to GND.

**Table 8. Test points**

Net name	Description
SCL	To probe SCL I <sup>2</sup> C bus signal line
SDA	To probe SDA I <sup>2</sup> C bus signal line
GND	To connect ground leads of probes or to connect power supply ground

## 2.3. Resistor configuration for pull-ups and supply routing

The NCA6416 device support voltage level translation between the I<sup>2</sup>C bus and GPIO port domains.

- R23 connects VDD to VDDP. By default, it is unpopulated to allow independent dual-supply operation. If VDD = VDDP is desired, R23 may be shorted.

Allows bidirectional voltage-level translation and GPIO expansion between

- 1.8 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
- 2.5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
- 3.3 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P
- 5 V SCL/SDA and 1.8 V, 2.5 V, 3.3 V or 5 V Port P

## 2.4. LED visualizer module (breakaway & dockable)

The evaluation board includes a breakaway LED visualizer module designed to provide a quick and convenient way to observe the output state of the NCA6416 GPIO ports. This module interfaces with the EVB through GPIO headers J3 (Port 0) and J5 (Port 1) using the J6 visualizer socket.

When docked:

- P0\_n signals on J3 connect to the P0\_n lines of the J6 socket
- P1\_n signals on J5 connect to the P1\_n lines of the J6 socket
- VDDP (pins 1, 2) supplies power to the visualizer LEDs and buffer
- GND (pins 19, 20) provides ground reference

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Refer to [Table 5](#) for the detailed J6 socket pinout and connection mapping.

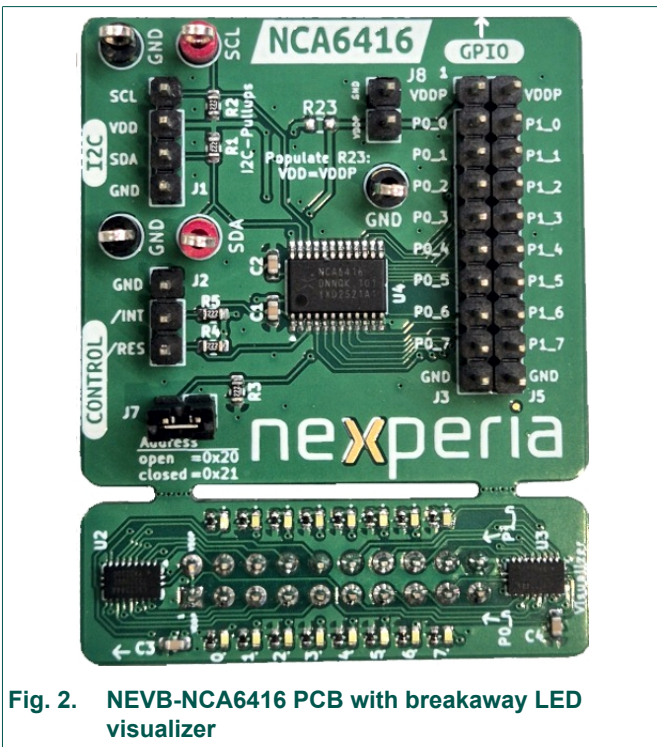
The visualizer receives buffered outputs from the NCA6416, enabling safe LED indication without directly loading the GPIO pins. It can be detached for direct GPIO access or alternative output use.

This evaluation board uses two Nexperia 74LVC2244A octal buffers (U2 and U3) to drive the on-board LEDs. While the NCA6416 features latched outputs capable of sourcing or sinking up to 25 mA per pin, the buffer is included to:

- Isolate the NCA6416 from direct LED current loads
- Improve thermal and electrical robustness during evaluation
- Support higher current fan-out and enhanced signal integrity

For end applications where current requirements are lower and PCB space is limited, designers may choose to drive LEDs directly from the NCA6416 GPIO ports, provided the per-pin and per-port current limits (see data sheet) are observed.

[Fig. 2](#) and [Fig. 3](#) shows the visualizer board detached and plugged in to the GPIO interface.



**Fig. 2. NEVB-NCA6416 PCB with breakaway LED visualizer**



**Fig. 3. NEVB-NCA6416 PCB with dockable LED visualizer**

### 3. Schematics

Fig. 4 shows the schematic of NEVB-NCA6416 evaluation board.

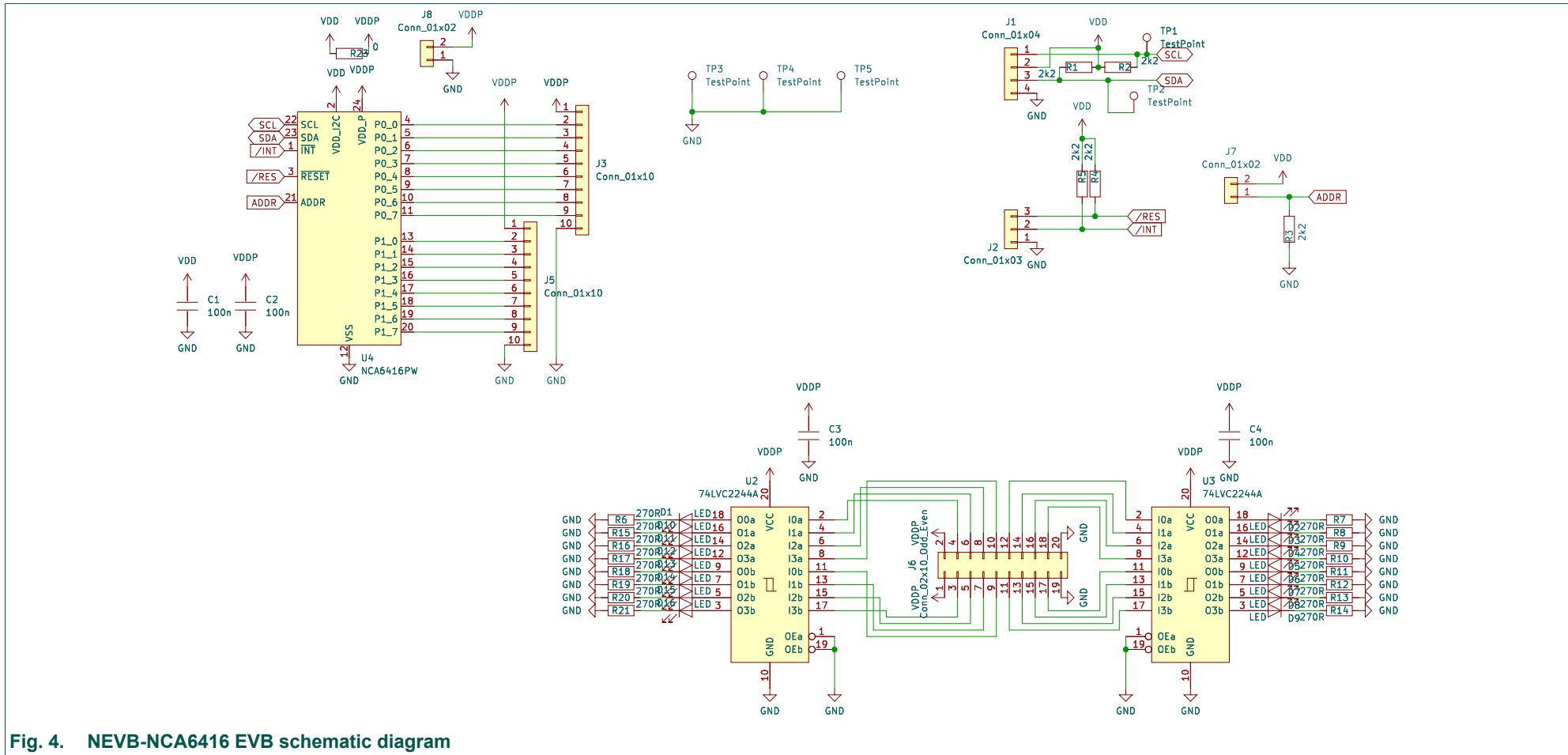


Fig. 4. NEVB-NCA6416 EVB schematic diagram

### 4. PCB Layout

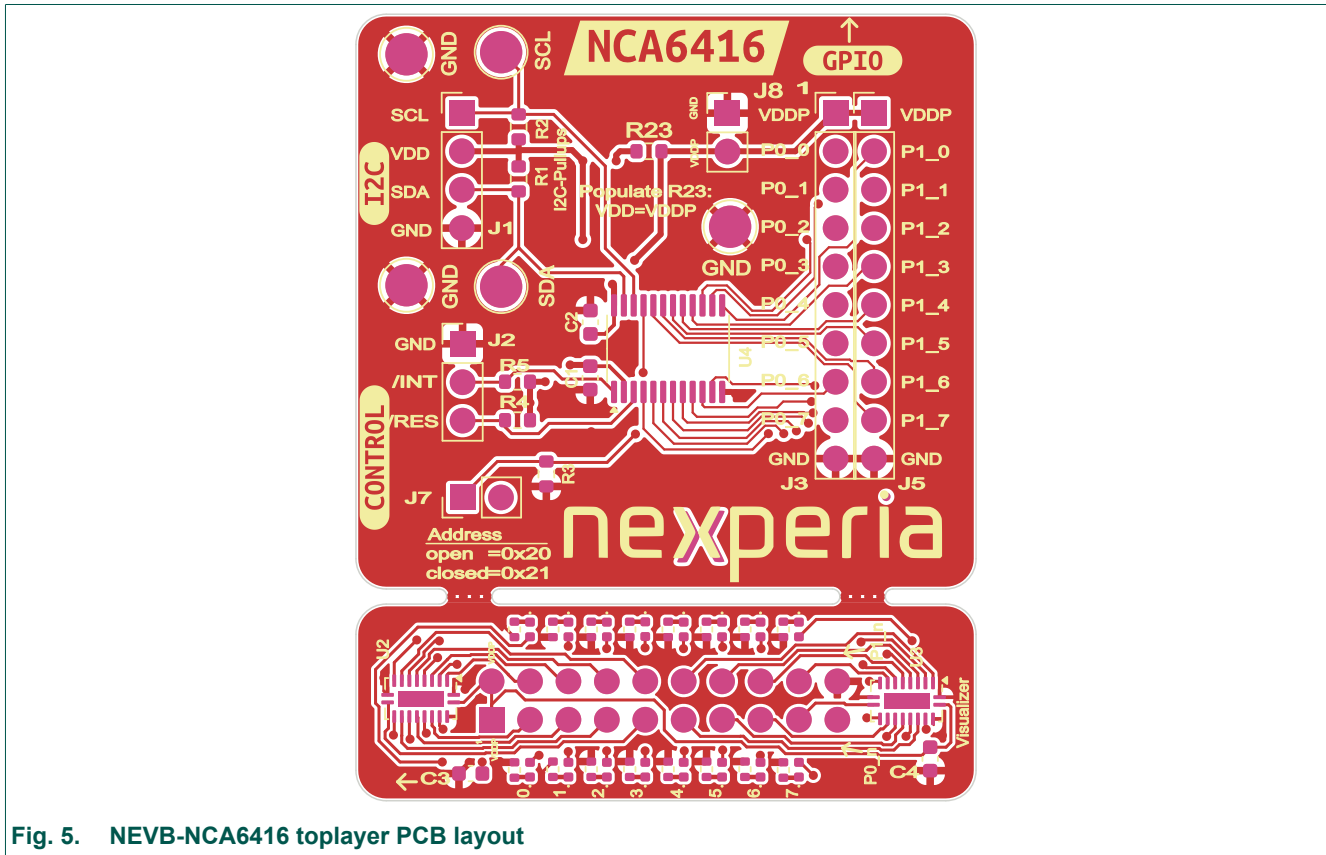


Fig. 5. NEVB-NCA6416 toplayer PCB layout

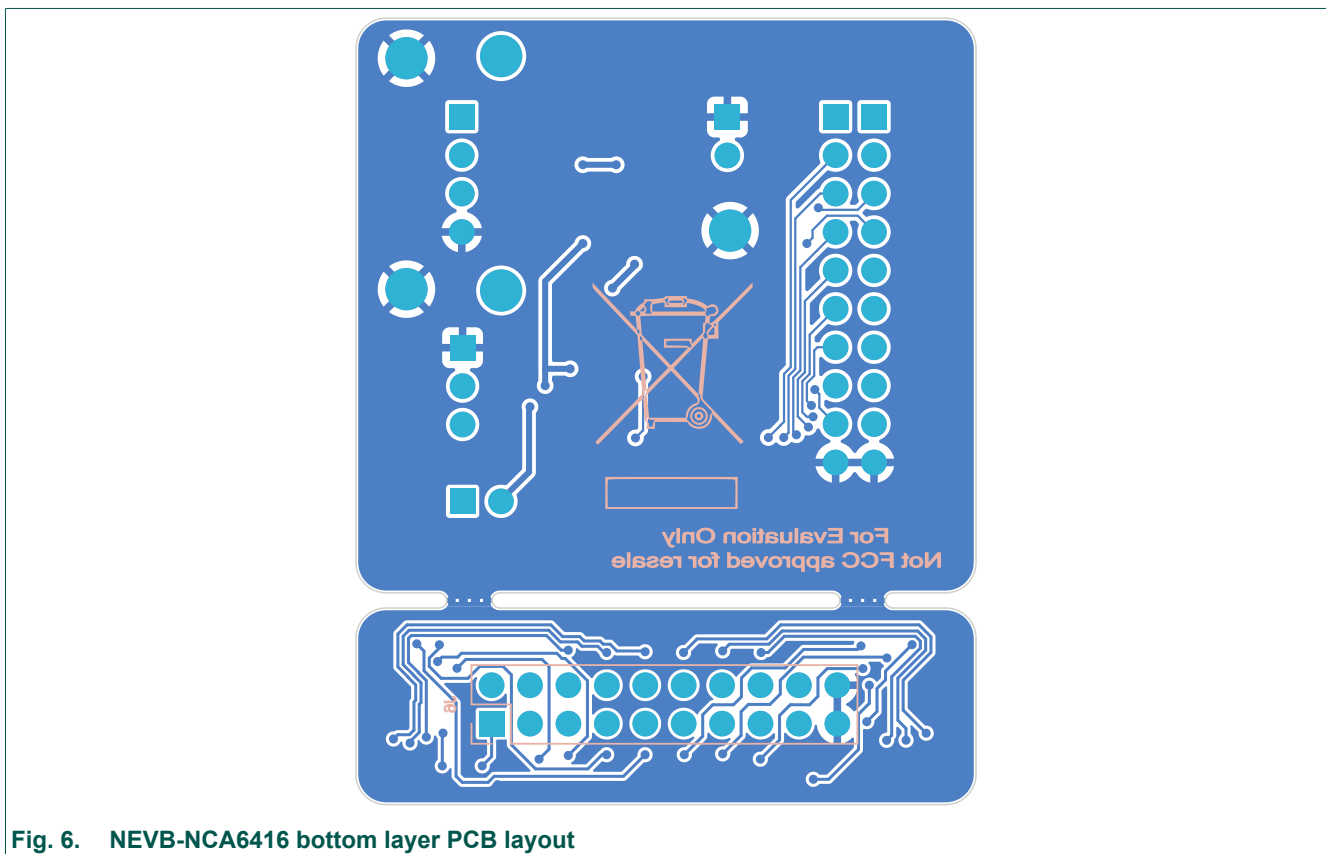


Fig. 6. NEVB-NCA6416 bottom layer PCB layout

## 5. Bill of Materials

Table 9. Bill of Materials

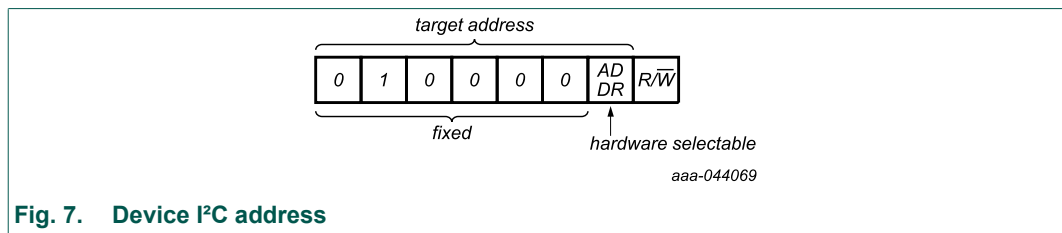
Designator	Description	Component	Quantity
C1, C2, C3, C4	50 V 100 nF X7R ±10% 0603 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS	CC0603KRX7R9BB104	4
D1, D10, D11, D12, D13, D14, D15, D16, D2, D3, D4, D5, D6, D7, D8, D9	5 mA Yellow Lens op View Mount White 120° 75 mW 2.8 V 0402 LED Indication - Discrete ROHS	XL-1005UWC	16
J1	Through Hole 2.54 mm 4P 6 mm -40 °C to +105 °C 3 mm 2.54 mm 1 Black Brass 1x4P Through Hole, P=2.54 mm Pin Headers ROHS	61300411121	1
J2	Through Hole Tin 3P -55 °C to +105 °C 2.54 mm Black 1 Phosphor Bronze Through Hole, P=2.54 mm Pin Headers ROHS	TSW-103-07-T-S	1
J7, J8	Connector Header Through Hole 2 position 0.100" (2.54 mm)	TSW-102-07-T-S	2
J5, J3	Connector Header Through Hole 10 position 0.100" (2.54 mm)	TSW-110-07-G-S	2
J6	20 Position Receptacle Connector 0.100" (2.54 mm) Through Hole Gold	SSW-110-01-G-D	1
R1, R2, R3, R4, R5	100 mW Thick Film Resistor 75 V ±100 ppm/°C ±1% 2.2 kΩ 0603 Chip Resistor - Surface Mount ROHS	0603WAF2201T5E	5
R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R21, R6, R7, R8, R9	62.5 mW Thick Film Resistor 50 V ±100 ppm/°C ±1% 270 Ω 0402 Chip Resistor - Surface Mount ROHS	0402WGF2700TCE	16
R23	100 mW Thick Film Resistor 75 V ±5 % 0 Ω 0603 Chip Resistor - Surface Mount ROHS	RC0603JR-070RL	1
SCL, SDA	Test Points / Test Rings ROHS	5010	2
GND, GND, GND	Test Points / Test Rings ROHS	5011	3
U4	Integrated Circuit- 16bit I <sup>2</sup> C GPIO expander	NCA6416PW	1
U2, U3	Integrated Circuit- Buffer/translator or auxiliary logic — refer to schematic for function	74LVC2244ABQ	2

## 6. Address and register information

### 6.1. Device address

ADDR is referenced to the VCCP (I/O) domain and must be held HIGH ( $\geq 0.7 \times VCCP$ ) or LOW ( $\leq 0.3 \times VCCP$ ) to select the address. See [Table 10](#). The last bit of the target address (R/W) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

Following a START condition, the bus controller must output the address of the target it is accessing. The address of NCA6416 is shown in [Fig. 7](#). To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pin, and they must be pulled HIGH or LOW. The last bit of the target address defines the operation to be performed. When set to logic 1 a read is selected, while logic 0 selects a write operation.



**Fig. 7.** Device I<sup>2</sup>C address

There are two unique addresses possible with the ADDR pin. [Table 10](#) below shows the two combinations.

**Table 10.** Possible I<sup>2</sup>C addresses on NCA6416 based on ADDR pin state

ADDR	7 bit I <sup>2</sup> C address
GND	0x20
VCC	0x21

Ensure that the I<sup>2</sup>C address assigned to the NCA6416 does not overlap with any other target device address, as this can lead to bus contention or unintended access during control register communication.

### 6.2. Interface definition

The I<sup>2</sup>C-bus target address follows the fixed pattern 0b010000\_ADDR with the R/W bit as LSB. The I/O data bus byte maps GPIO pins as follows:

- Byte 0: P0\_0 to P0\_7 (LSB to MSB)
- Byte 1: P1\_0 to P1\_7 (LSB to MSB)

These correspond to the I/O expander ports accessed via register read/write.

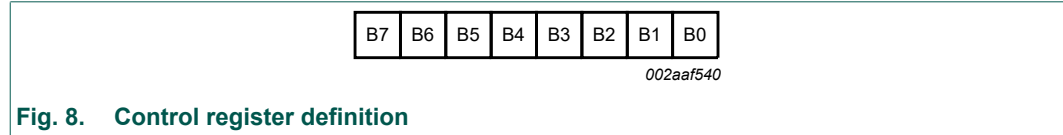
**Table 11.** Interface definition

Byte	Bit							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I <sup>2</sup> C-bus target address	L	H	L	L	L	L	ADDR	R/W
I/O data bus	P0_7	P0_6	P0_5	P0_4	P0_3	P0_2	P0_1	P0_0
	P1_7	P1_6	P1_5	P1_4	P1_3	P1_2	P1_1	P1_0

### 6.3. Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus controller sends a command byte, which is stored in the Pointer register in NCA6416. The lower three bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register is write only.

Once a new command has been sent, the register that was last addressed continues to be accessed by reads until a new command byte is sent.



**Table 12. Command byte**

Pointer register bits								Command byte	Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0				
0	0	0	0	0	0	0	0	00h	Input port 0	read byte	xxxx xxxx <sup>[1]</sup>
0	0	0	0	0	0	0	1	01h	Input port 1	read byte	xxxx xxxx <sup>[1]</sup>
0	0	0	0	0	0	1	0	02h	Output port 0	read/write byte	1111 1111
0	0	0	0	0	0	1	1	03h	Output port 1	read/write byte	1111 1111
0	0	0	0	0	1	0	0	04h	Polarity inversion port 0	read/write byte	0000 0000
0	0	0	0	0	1	0	1	05h	Polarity inversion port 1	read/write byte	0000 0000
0	0	0	0	0	1	1	0	06h	Configuration port 0	read/write byte	1111 1111
0	0	0	0	0	1	1	1	07h	Configuration port 1	read/write byte	1111 1111

[1] undefined input state depending on external logic

### 6.4. Register descriptions

#### 6.4.1. Input port registers (00h, 01h)

The Input port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in Section 8 of the NCA6416 data sheet.

**Table 13. Input port 0 register (address 00h)**

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

**Table 14. Input port 1 register (address 01h)**

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

### 6.4.2. Output port registers (02h, 03h)

The Output port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, not the actual pin value. A register pair write and a register pair read are described in Section 8 of the NCA6416 data sheet.

**Table 15. Output port 0 register (address 02h)**

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

**Table 16. Output port 1 register (address 03h)**

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

### 6.4.3. Polarity inversion registers (04h, 05h)

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained. A register pair write and a register pair read are described in Section 8 of the NCA6416 data sheet.

**Table 17. Polarity inversion port 0 register (address 04h)**

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

**Table 18. Polarity inversion port 1 register (address 05h)**

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

### 6.4.4. Configuration registers (06h, 07h)

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register pair write and a register pair read are described in Section 8 of the NCA6416 data sheet.

**Table 19. Configuration port 0 register (address 06h)**

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

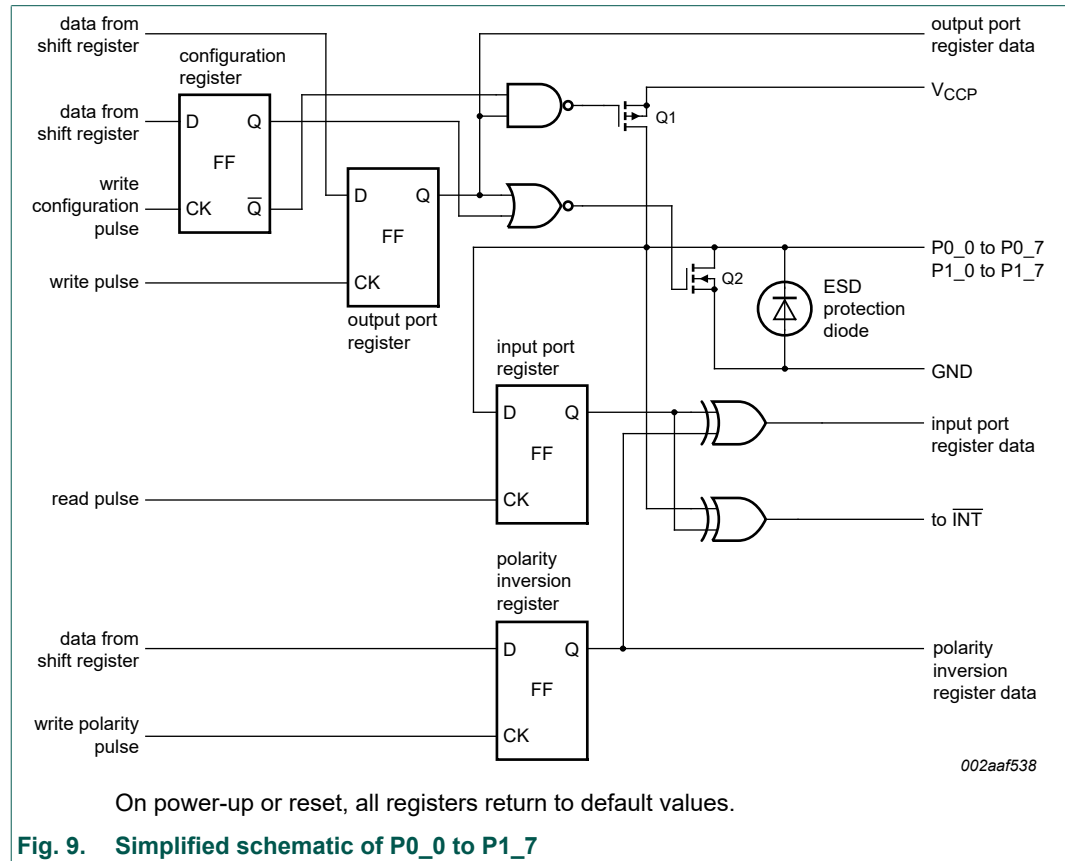
**Table 20. Configuration port 1 register (address 07h)**

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

## 7. I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V<sub>CCP</sub> to a maximum of 5.5 V. The I/Os are 5.5 V tolerant regardless of V<sub>CCP</sub>, when configured as inputs. For output mode, do not exceed recommended levels.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either V<sub>CCP</sub> or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.



**Fig. 9.** Simplified schematic of P0\_0 to P1\_7

## 8. Power-on reset

When power (from 0 V) is applied to V<sub>CCP</sub>, an internal power-on reset holds the NCA6416 in a reset condition until V<sub>CCP</sub> has reached V<sub>POR</sub>. At that time, the reset condition is released and the NCA6416 registers and I<sup>2</sup>C-bus/SMBus state machine initializes to their default states. After that, V<sub>CCP</sub> must be lowered to below V<sub>POR</sub> and back up to the operating voltage for a power-reset cycle. See Section 9 requirements on the NCA6416 data sheet.

## 9. Reset input ( $\overline{\text{RESET}}$ )

The  $\overline{\text{RESET}}$  input can be asserted to initialize the system while keeping the VCCP at its operating level. A reset can be accomplished by holding the  $\overline{\text{RESET}}$  pin LOW for a minimum of  $t_{w(\text{rst})}$  (see NCA6416 data sheet for spec). The NCA6416 registers and I<sup>2</sup>C-bus/SMBus state machine are changed to their default state once  $\overline{\text{RESET}}$  is LOW (Logic 0). When  $\overline{\text{RESET}}$  is HIGH (Logic 1), the I/O levels at the P port can be changed externally or through the controller. This input requires a pull-up resistor to V<sub>CCI</sub> if no active connection is used.

## 10. Interrupt output ( $\overline{\text{INT}}$ )

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time  $t_{v(\text{INT})}$ , the signal  $\overline{\text{INT}}$  is valid. The interrupt is reset when data on the port changes back to the original value or when data is read from the port that generated the interrupt (see Section 8 on NCA6416 data sheet). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the I/Os after resetting is detected and is transmitted as  $\overline{\text{INT}}$ .

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

The  $\overline{\text{INT}}$  output has an open-drain structure and requires pull-up resistor to VCCP or VCCI depending on the application.  $\overline{\text{INT}}$  should be connected to the voltage source of the device that requires the interrupt information.

## 11. Partial power-down and power-up sequence

The NCA6416 has two supplies and a voltage translation function, translating between the I<sup>2</sup>C bus and the P-PORTs.

Fig. 1 on the NCA6416 data sheet shows the block diagram that features a Power-On Reset block that senses both VCCI and VCCP. This is part of the implementation of the feature allowing partial power-down. [Table 21](#) gives an overview of supply and reset condition combinations.

**Table 21. NCA6416 modes based on combinations of V<sub>CCI</sub>, V<sub>CCP</sub> and  $\overline{\text{RESET}}$**

V <sub>CCI</sub>	V <sub>CCP</sub>	$\overline{\text{RESET}}$	Mode
L	L	X	Not functional
H	H	L	Reset
H	H	H	Functional
L	H	X	Partial power-down / Reset
H	L	X	Partial power-down / Reset

In the absence of both power supplies (VCCP and VCCI), the product is non-functional. However, overvoltage protection on the P-PORTs remains permissible, consistent with other operational modes. The overvoltage protection ensures that when a P-PORT is biased with an input voltage (V<sub>i</sub>) exceeding VCCP, input current is prevented. This protection is disabled only when a P-PORT is configured as an output in functional mode. When both VCCP and VCCI are present, the  $\overline{\text{RESET}}$  signal determines the product's operational state, toggling between functional mode and reset mode. If VCCP is present but VCCI is absent, the product enters reset mode. In this state, configuration registers are initialized to their default values, configuring all P-PORTs as input ports, with their output drivers disabled. When VCCI is present but VCCP absent, the SDA and  $\overline{\text{INT}}$  open drain drivers are off. In partial power-down scenarios, where only one supply is active, there is no risk of excessive current draw on the active supply. The power supplies, VCCP and VCCI, can be sequenced (ramped-up or -down) in any order while output glitches are prevented. Regardless of the power-up sequence, the product initializes in its default state. During power-up, the  $\overline{\text{RESET}}$  signal can be pulled HIGH to enable functional mode at startup. Alternatively, if  $\overline{\text{RESET}}$  is pulled LOW during power-up, the product remains in reset (disabled) mode. De-asserting  $\overline{\text{RESET}}$  subsequently transitions the product to functional mode.

## 12. Abbreviations

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**Table 22. Abbreviations**

Acronym	Description
ESD	ElectroStatic Discharge
EVB	Evaluation Board
I <sup>2</sup> C	Inter-Integrated Circuit
PCB	Printed Circuit Board

## 13. Revision History

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**Table 23. Revision History**

Revision number	Date	Description
UM90077 v.1	20260130	Initial version

## 14. Legal information

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