UM90073

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user manual

# NEVB-NCA9548A (NCA9547A and NCA9548A) evaluation board


Abstract: The NEVB-NCA9548A EVB (Evaluation Board) is designed for the Nexperia I²C controlled 8-channel Switch/Mux family. The board provides convenient test points for GND, I²C-Bus signals SCL and SDA as selection options for Address and RESET pins. The EVB can be used for the NCA9548A and NCA9547A.

Keywords: I²C Switch, I²C Multiplexer, Evaluation Board (EVB), Fast Mode, 400kHz, 6 V tolerant input, RESET

nexperia

# 1. Introduction

The NEVB-NCA9548A is an evaluation PCB designed for the Nexperia I²C controlled 8-channel Switch/Mux family. The EVB arrives enclosed in an antistatic ESD bag with labeling. The board provides convenient test points for GND, I²C-Bus signals SCL and SDA as selection options for Address and $\overline{\text{RESET}}$ pins. The EVB can be used for the NCA9548A and NCA9547A.

The NCA9548A is an octal bidirectional translating switch controlled via the I²C-bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Any individual SCn/SDn channel or combination of channels can be selected, determined by the contents of the programmable control register.

The NCA9547A is an octal bidirectional translating multiplexer controlled by the I²C-bus. The SCL/SDA upstream pair fans out to eight downstream pairs, or channels. Only one SCn/SDn channel can be selected at a time, determined by the contents of the programmable control register. The device powers up with Channel 0 connected, allowing immediate communication between the controller and downstream devices on that channel.

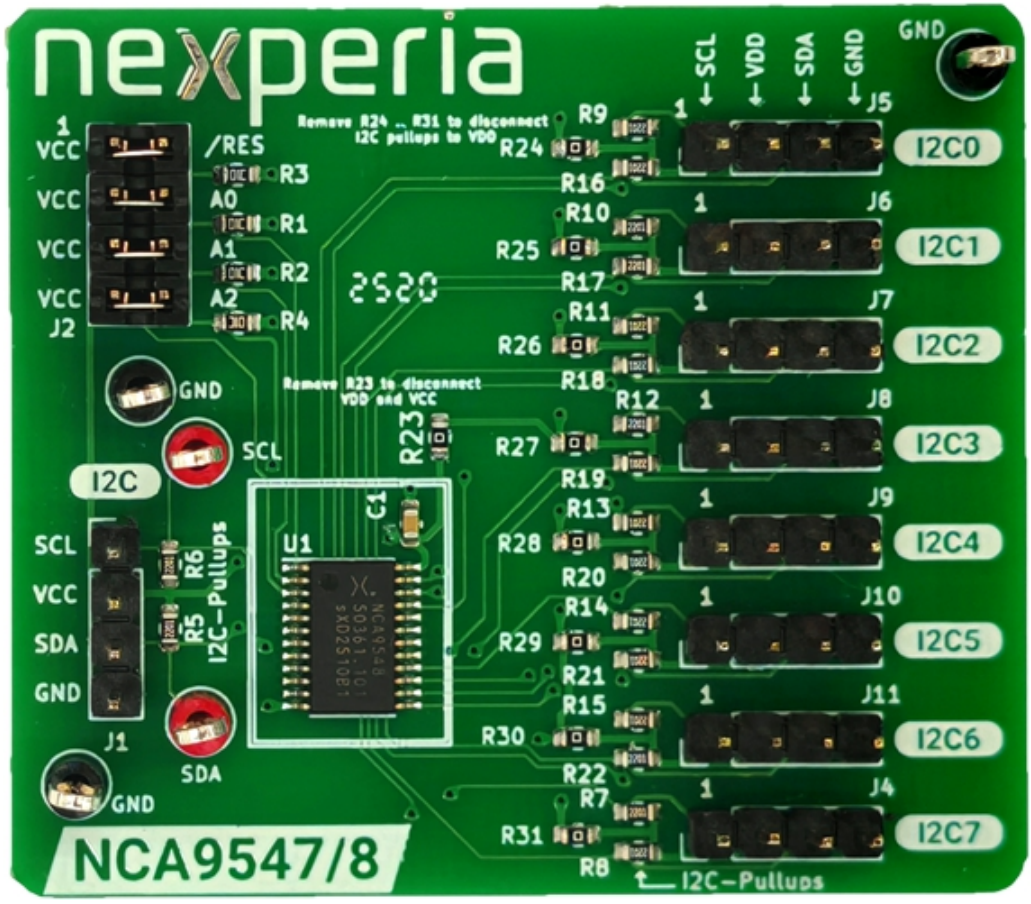


**Fig. 1. NEVB-NCA9548A evaluation board (EVB)**

## 1.1. Features

- EVB name = NEVB-NCA9548A
- Device = NCA9548A, NCA9547A
- Input voltage = 1.65 V to 5.5 V
- 8 bidirectional translating I²C channels
- Current drive capability = ±25 mA
- I²C interface, compatible with SMBus standards
- Fast-Mode 400 kHz
- 6 V tolerant inputs
- Three address pins allowing up to eight devices on the I²C-bus
- Active LOW reset input

Further details about the specification and parameters of NCA9548A, NCA9547A can be found in their respective data sheets, but a high-level summary is provided in Table 1:

**Table 1. 8-channel I²C Switch/Mux family features**

| Device | Package | Feature |
|---|---|---|
| NCA9548APW | TSSOP24 | Any individual SCn/SDn channel or combination of channels can be selected |
| NCA9548ABY | HWQFN24 | |
| NCA9547APW | TSSOP24 | Only one SCn/SDn channel can be selected at a time |
| NCA9547ABY | HWQFN24 | |

# 2. Hardware setup

The following sections describes the EVB jumper and header description.

## 2.1. Headers J1/J2/J4/J5/J6/J7/J8/J9/J10/J11

Header J1 is for connecting upstream I²C interface to NCA9548A/NCA9547A. J2 is for selection signals – $\overline{\text{RESET}}$ and address pins. J4, J5, J6, J7, J8, J9, J10, J11 eight headers for eight downstream channels with connections for eight I²C downstream interfaces.

A detailed description of the header pinouts is provided in the tables presented below:

**Table 2. J1 headers**

| J1 net name | Pin number | Description |
|---|---|---|
| SCL | 1 | SCL I²C-Bus signal line |
| VCC | 2 | Power supply for NCA9548A/NCA9547A |
| SDA | 3 | SDA I²C-Bus signal line |
| GND | 4 | GND connection |

**Table 3. J2 headers**

| J2 net name | Pin number | Description |
|---|---|---|
| /RES | 1 | Active Low reset input; Connect to $V_{CC}$ using a jumper short if $\overline{\text{RESET}}$ assertion is NOT intended |
| A0 | 2 | Connect to $V_{CC}$ by placing a jumper, or leave open to default to GND through the onboard 10 kΩ pull-down |
| A1 | 3 | Connect to $V_{CC}$ by placing a jumper, or leave open to default to GND through the onboard 10 kΩ pull-down |
| A2 | 4 | Connect to $V_{CC}$ by placing a jumper, or leave open to default to GND through the onboard 10 kΩ pull-down |

**Table 4. J4-J11 headers**

| J4 net name | Pin number | Description |
|---|---|---|
| SCL | 1 | SCL I²C-Bus signal line on downstream side |
| VDD | 2 | Voltage pull-up for SCL (SCn) and SDA (SDn) lines of downstream connected devices |
| SDA | 3 | SDA I²C-Bus signal line on downstream side |
| GND | 4 | GND connection |

## 2.2. Test points

There are 5 test points. Two red and 3 black. The red test points are labelled SCL and SDA for probing upstream I²C bus signals. The rest of the three black test points are connected to GND.

**Table 5. J1 headers**

| J5 net name | Description |
|---|---|
| SCL | To probe SCL I²C-Bus signal line on upstream side |
| SDA | To probe SDA I²C-Bus signal line on upstream side |
| GND | To connect ground leads of probes or to connect power supply ground |

## 2.3. Resistor configuration for pull-ups and supply routing

The NCA9548A and NCA9547A devices support voltage level translation between the upstream and downstream I²C buses.

- R23 connects $V_{CC}$ to $V_{DD}$ by default; removing it enables independent $V_{DD}$, which must be externally supplied.
- R24–R31 route the common $V_{DD}$ pull-up to all downstream channels; removing them isolates the pull-up path per channel.
- R7–R22 are individual pull-up resistors for each downstream channel and can be replaced to tune the value or support different pull-up voltages.

When selecting the downstream pull-up voltage, ensure that $V_{pass}$ characteristics are respected. Refer to the device datasheet for detailed $V_{pass}$ specifications and limitations.

# 3. Schematics

Fig. 2 shows the schematic of NEVB-NCA9548A evaluation board.

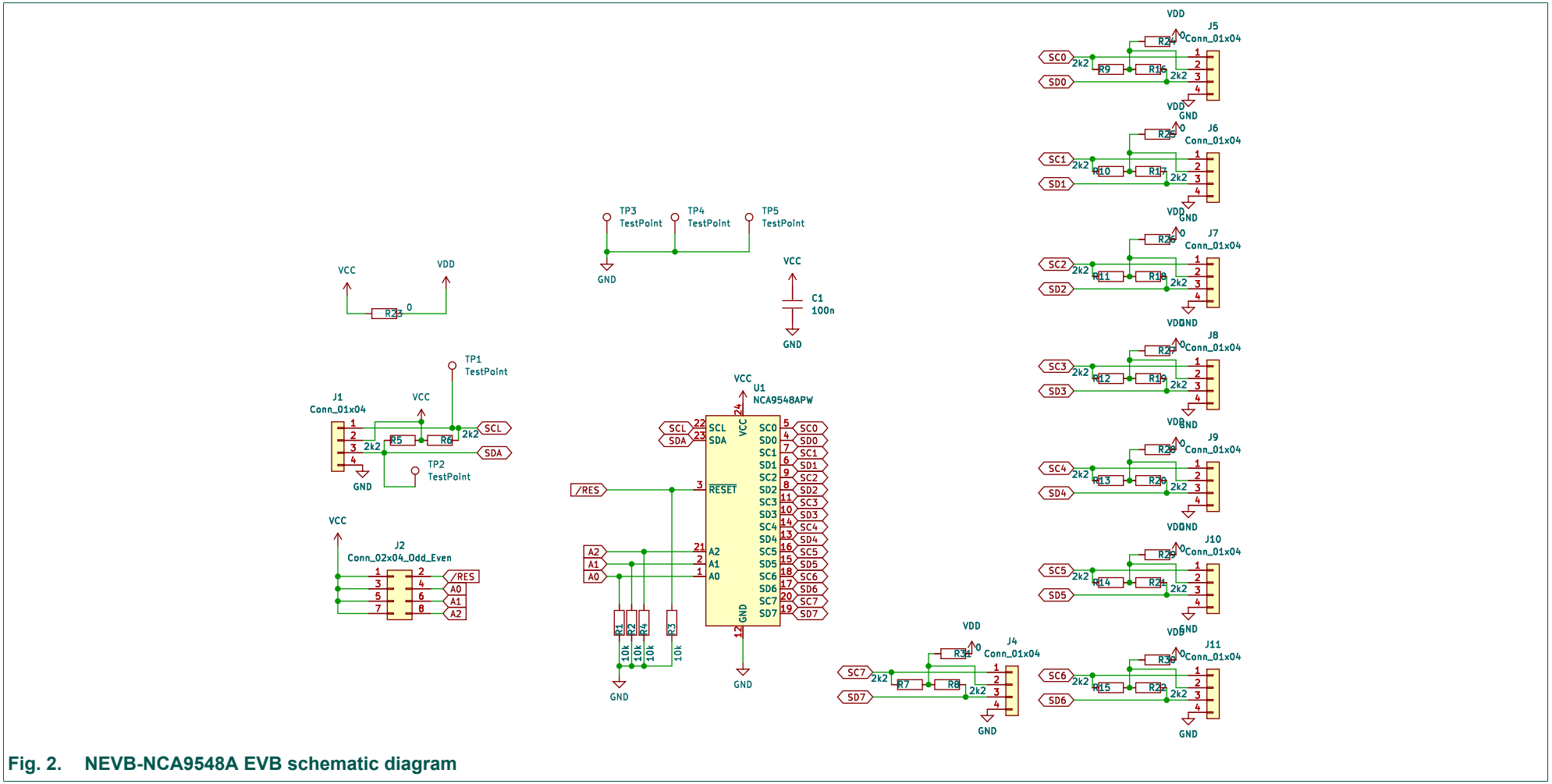


**Fig. 2. NEVB-NCA9548A EVB schematic diagram**

## 4. PCB Layout

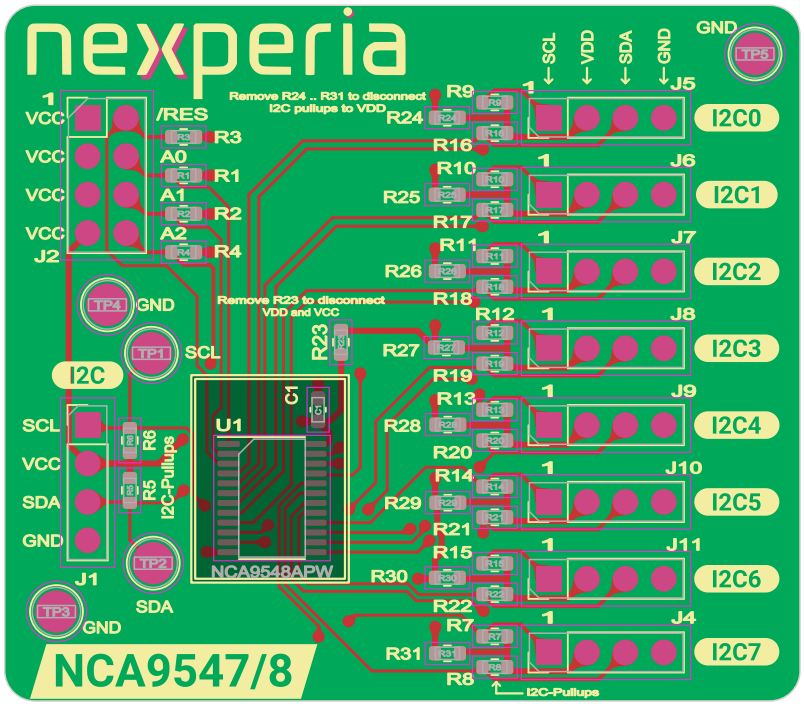


Fig. 3. Top Copper Layer

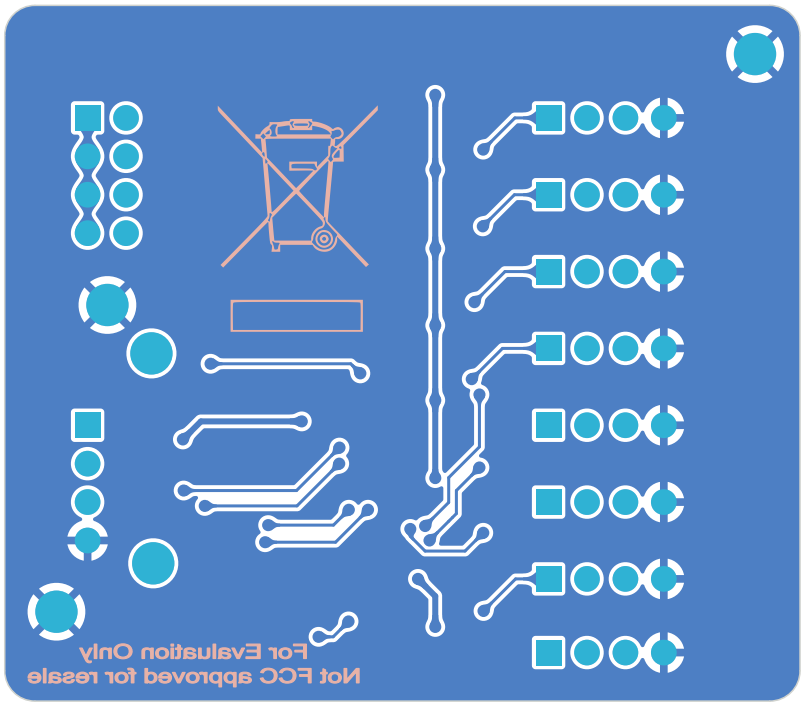


Fig. 4. Bottom Copper Layer

# 5. Bill of Materials

**Table 6. Bill of Materials**

| Designator | Description | Component | Quantity |
|---|---|---|---|
| C1 | 50 V 100 nF X7R ±10% 0603 Multilayer Ceramic Capacitors MLCC - SMD/SMT ROHS | CL10B104KB8NNNC | 1 |
| J1, J10, J11, J4, J5, J6, J7, J8, J9 | Through Hole 2.54 mm 4P 6 mm -40Ω to +105 Ω 3 mm 2.54 mm 1 Black Brass 1x4P Through Hole,P=2.54 mm Pin Headers ROHS | 61300411121 | 9 |
| J2 | Through Hole 2.54 mm 8P 6mm -40 Ω to +105 Ω 3mm 2.54 mm 2 Black Brass 2x4P 2.54 mm Through Hole,P=2.54 mm Pin Headers ROHS | 0010897082 | 1 |
| R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R5, R6, R7, R8, R9 | 100mW Thick Film Resistor ±100 ppm/Ω ±1% 2.2 kΩ 0603 Chip Resistor - Surface Mount ROHS | CRCW06032K20FKEAC | 18 |
| R23, R24, R25, R26, R27, R28, R29, R30, R31 | 100 mW Thick Film Resistor 75 V ±5% 0Ω 0603 Chip Resistor - Surface Mount ROHS | RC0603JR-070RL | 9 |
| R1, R2, R3, R4 | 100 mW Thick Film Resistor 75 V ±100 ppm/Ω ±1% 10 kΩ 0603 Chip Resistor - Surface Mount ROHS | RC0603FR-0710KL | 4 |
| SCL, SDA | Test Points / Test Rings ROHS | 5010 | 2 |
| GND, GND, GND | Test Points / Test Rings ROHS | 5011 | 3 |
| U1 | Integrated Circuit | NCA9548APW | 1 |

# 6. Address and register information

## 6.1. Device address

Following a START condition, the bus controller must output the address of the target it is accessing. The address of the NCA9548A is shown in Fig. 5. To conserve power, no internal pull-up resistors are incorporated on the hardware selectable address pins, and they must be pulled HIGH or LOW. The last bit of the target address defines the operation to be performed. When set to logic 1 a read is selected, while logic 0 selects a write operation.

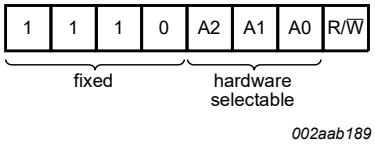


**Fig. 5. Device I²C address**

There are eight unique addresses possible with the three address pins A2, A1, A0. Table 7 below shows all combinations.

**Table 7. Possible I²C addresses on NCA9548A/NCA9547A**

| A2 | A1 | A0 | 7 bit I²C address |
|---|---|---|---|
| GND | GND | GND | 0x70 |
| GND | GND | VCC | 0x71 |
| GND | VCC | GND | 0x72 |
| GND | VCC | VCC | 0x73 |
| VCC | GND | GND | 0x74 |
| VCC | GND | VCC | 0x75 |
| VCC | VCC | GND | 0x76 |
| VCC | VCC | VCC | 0x77 |

Ensure that the I²C address assigned to the NCA9548A does not overlap with any downstream target device address, as this can lead to bus contention or unintended access during control register communication.

## 6.2. Control register

Following the successful acknowledgement of the target address, the bus controller will send a byte to NCA9548A, which will be stored in the control register. If multiple bytes are received by the NCA9548A, it will save the last byte received. This register can be written and read via the I²C-bus.

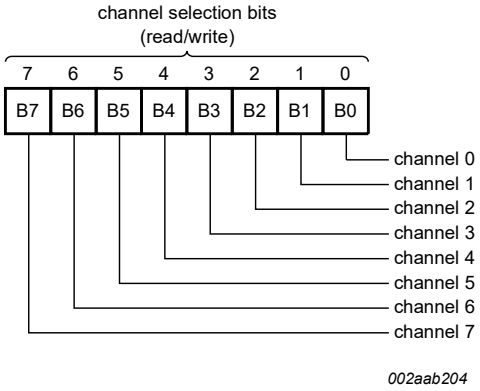


**Fig. 6. Control register definition**

In NCA9548A, one or several SCn/SDnx downstream pair, or channel, can be selected by the contents of the control register. In NCA9547A only one SCn/SDn downstream pair, or channel, can be selected by the contents of the control register. This register is written after the NCA9548A/NCA9547A has been addressed. The contents of the control byte are used to determine which channel is to be selected. When a channel is selected, the channel will become active after a STOP condition has been placed on the I²C-bus. This ensures that all SCn/SDn lines will be in a HIGH state when the channel is made active, so that no false conditions are generated at the time of connection.

**Table 8. Control register: Write-channel selection; Read-channel status on NCA9548A**

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Command |
|---|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | X | 0 | channel 0 disabled |
| | | | | | | | 1 | channel 0 enabled |
| X | X | X | X | X | X | 0 | X | channel 1 disabled |
| | | | | | | 1 | | channel 1 enabled |
| X | X | X | X | X | 0 | X | X | channel 2 disabled |
| | | | | | 1 | | | channel 2 enabled |
| X | X | X | X | 0 | X | X | X | channel 3 disabled |
| | | | | 1 | | | | channel 3 enabled |
| X | X | X | 0 | X | X | X | X | channel 4 disabled |
| | | | 1 | | | | | channel 4 enabled |
| X | X | 0 | X | X | X | X | X | channel 5 disabled |
| | | 1 | | | | | | channel 5 enabled |
| X | 0 | X | X | X | X | X | X | channel 6 disabled |
| | 1 | | | | | | | channel 6 enabled |
| 0 | X | X | X | X | X | X | X | channel 7 disabled |
| 1 | | | | | | | | channel 7 enabled |

**Remark**: Multiple channels can be enabled at the same time. Example: B7 = 0, B6 = 1, B5 = 0, B4 = 0, B3 = 1, B2 = 1, B1 = 0, B0 = 0, means that channels 7, 5, 4, 1 and 0 are disabled and channels 6, 3, and 2 are enabled. Care should be taken not to exceed the maximum bus capacitance. Default condition is all zeroes.

**Table 9. Control register: Write-channel selection; Read-channel status on NCA9547A**

| B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Command |
|---|---|---|---|---|---|---|---|---|
| X | X | X | X | 0 | X | X | X | no channel selected |
| X | X | X | X | 1 | 0 | 0 | 0 | channel 0 enabled |
| X | X | X | X | 1 | 0 | 1 | 0 | channel 2 enabled |
| X | X | X | X | 1 | 1 | 0 | 0 | channel 4 enabled |
| X | X | X | X | 1 | 1 | 1 | 0 | channel 6 enabled |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | channel 0 enabled; power-up/reset default state |

### 6.3. $\overline{\text{RESET}}$ input

The $\overline{\text{RESET}}$ input is an active LOW signal which may be used to recover from a bus fault condition. By asserting this signal LOW for a minimum of $t_{w(rst)L}$, the NCA9547A will reset its register and I²Cbus state machine and will deselect all channels except channel 0. The $\overline{\text{RESET}}$ input must be connected to VCC through a pull-up resistor. See the data sheet for more details.

## 7. Abbreviations

**Table 10. Abbreviations**

| Acronym | Description |
|---|---|
| ESD | ElectroStatic Discharge |
| EVB | Evaluation Board |
| I²C | Inter-Integrated Circuit |
| PCB | Printed Circuit Board |

## 8. Revision History

**Table 11. Revision History**

| Revision number | Date | Description |
|---|---|---|
| UM90073 v.1 | 20250904 | Initial version |

# 9. Legal information

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