UM90071

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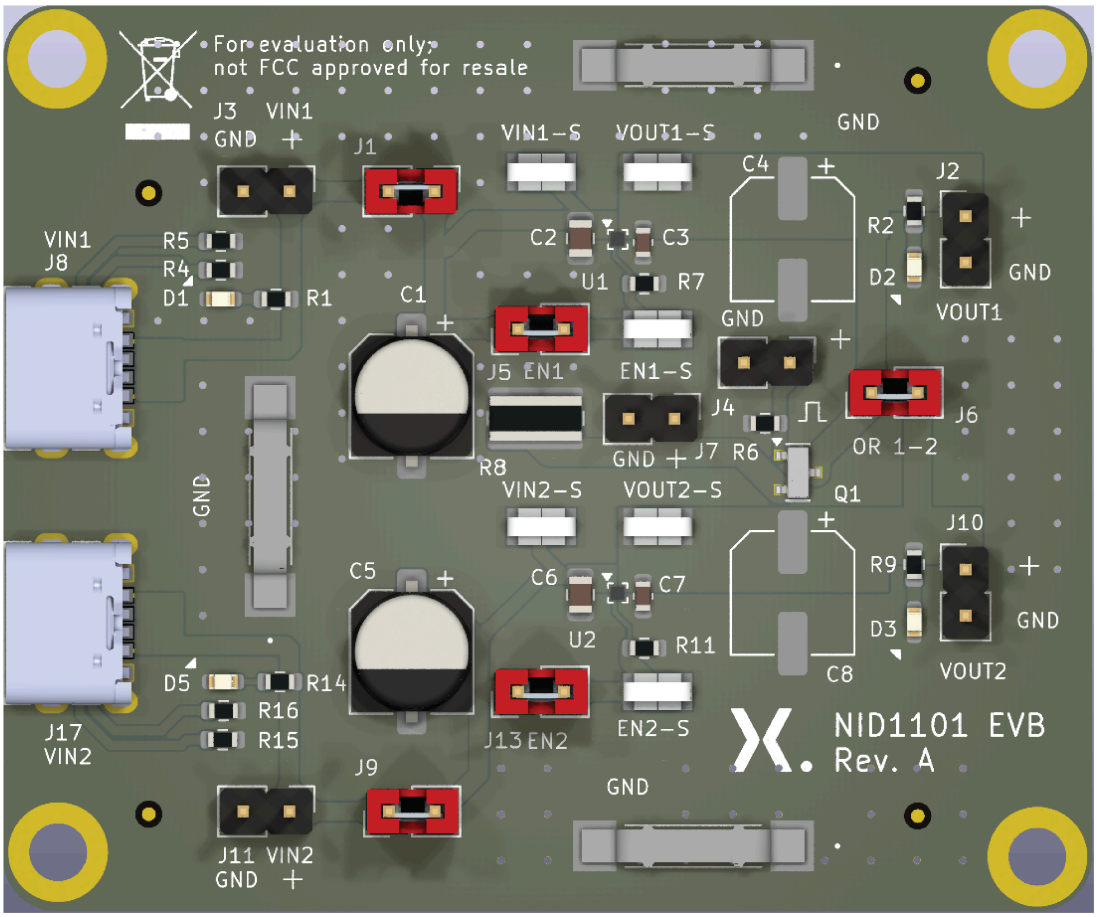
user manual

NEVB-NID1101 Evaluation board user manual



Abstract: NEVB-NID1101 evaluation board is a two-layer PCB equipped with two NID1101 ideal diodes. It allows users to explore the device's behavior under various application conditions.

Keywords: ideal diode, Schottky replacement, Oring, evaluation board (EVB), forward voltage blocking

nexperia

1. Introduction

NID1101 is a low-forward voltage integrated ideal diode designed to replace traditional diodes in low-voltage systems that cannot tolerate the high voltage drops of conventional rectifier components.

This device supports a continuous current of 1.5 A and operates over an input voltage range of 1.5 V to 5.5 V. Unlike standard diodes, it offers forward voltage and reverse current blocking, short-circuit protection, controlled inrush current, and thermal protection.

This evaluation PCB incorporates two NID1101 ideal diodes, enabling the assessment of performance and behavior across various use cases, such as OR-ing, power supply multiplexing, and parallel operation. NEVB-NID1101 offers convenient access to multiple power supply inputs, as well as probe hook-ups for evaluation. Additionally, it includes an NMOS transistor at the output to test short circuit behavior.

2. Key parameters

- Input operating voltage range (V_{IN}): 1.5 V to 5.5 V
- Continuous output current: 1.5 A
- Two supply inputs (V_{IN1}, V_{IN2})
- Two optional USB-C supply inputs for V_{IN1} and V_{IN2}
- Access to all device pins
- Use case selection by means of jumpers
- Short circuit testing

3. Schematics

Fig. 1 shows the schematic of NEVB-NID1101.

Explanation of the test pins, jumpers, and other features can be found in the following sections.

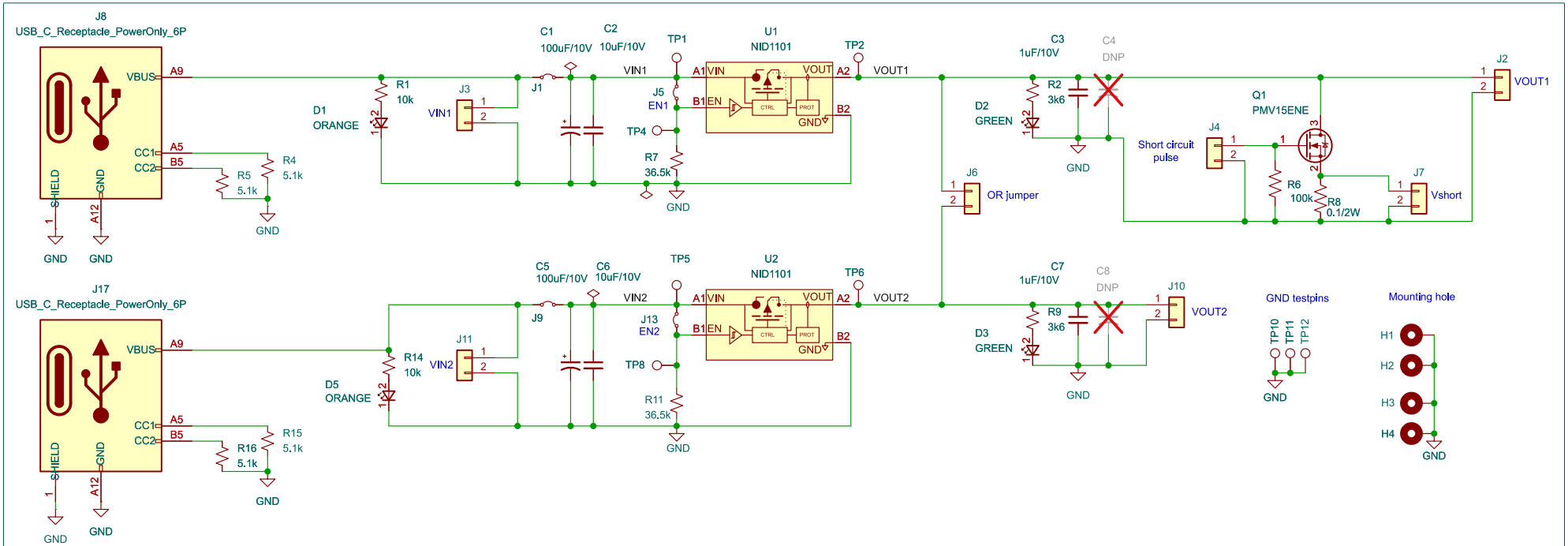


Fig. 1. Evaluation PCB schematic

4. PCB layout

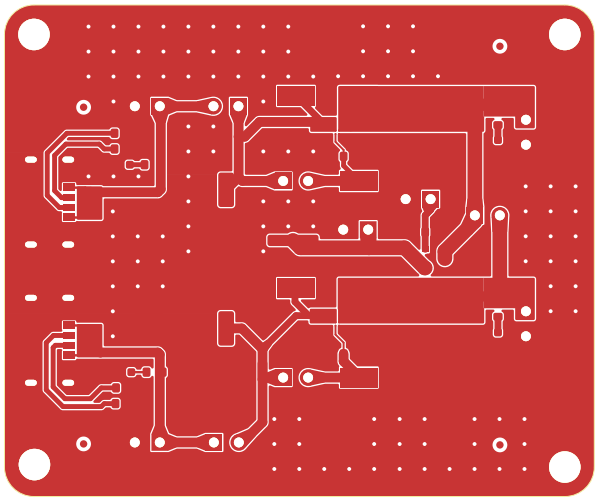


Fig. 2. Top copper layer

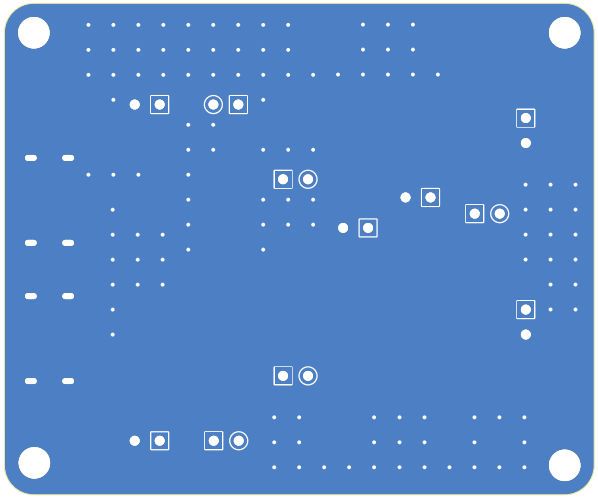


Fig. 3. Bottom copper layer

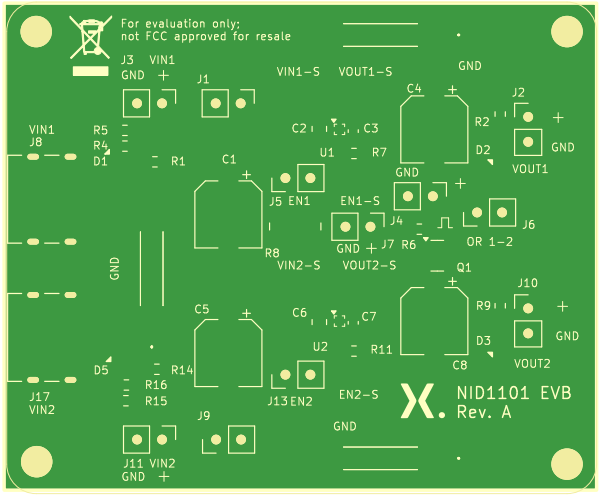


Fig. 4. Silkscreen top

5. Bill of materials

Table 1. Bill of materials

Reference(s)	Quantity	Value	Manufacturer	Manufacturer Part Number
C1, C5	2	100 µF/10 V	KEMET	EDK107M010A9GAA
C2, C6	2	10 µF/10 V	Murata Electronics	GRM21BR71A106KA73L
C3, C7	2	1 µF/10 V	KEMET	C0603C105K8RACTU
C4, C8	2	DNP	KEMET	EDK107M010A9GAA
D1, D5	2	ORANGE	Lite-On	LTST-C191KFKT
D2, D3	2	GREEN	Lite-On	LTST-C191KGKT
J1, J9	2	Jumper_2_Bridged	Wurth Elektronik	61300211121
J2, J3, J4, J5, J6, J7, J10, J11, J13	9	Conn_01x02	Wurth Elektronik	61300211121
J8, J17	2	USB_C_Receptacle_PowerOnly_6P	Same Sky	UJC-HP2-3-SMT-TR
Q1	1	PMV15ENE	Nexperia	PMV15ENER
R1, R14	2	10 kΩ	YAGEO	RC0603JR-0710KL
R2, R9	2	3.6 kΩ	YAGEO	RT0603DRE073K6L
R4, R5, R15, R16	4	5.1 kΩ	Bourns	CR0603-FX-5101ELF
R6	1	100 kΩ	Vishay / Dale	CRCW0603100KJNEAC
R7, R11	2	36.5 kΩ	KOA Speer	RK73H1JTTD3652F
R8	1	0.1 Ω/2 W	Vishay / Dale	RCWE1020R100FKEA
TP1, TP2, TP4, TP5, TP6, TP8	6	TestPoint	Keystone Electronics	5019
TP10, TP11, TP12	3	TestPoint-GND	Harwin	S1621-46R
U1, U2	2	NID1101UP	Nexperia	NID1101UP
J1, J5, J6, J9, J13	5	JUMPER SKT RED OPEN TOP	Harwin	M7581-46

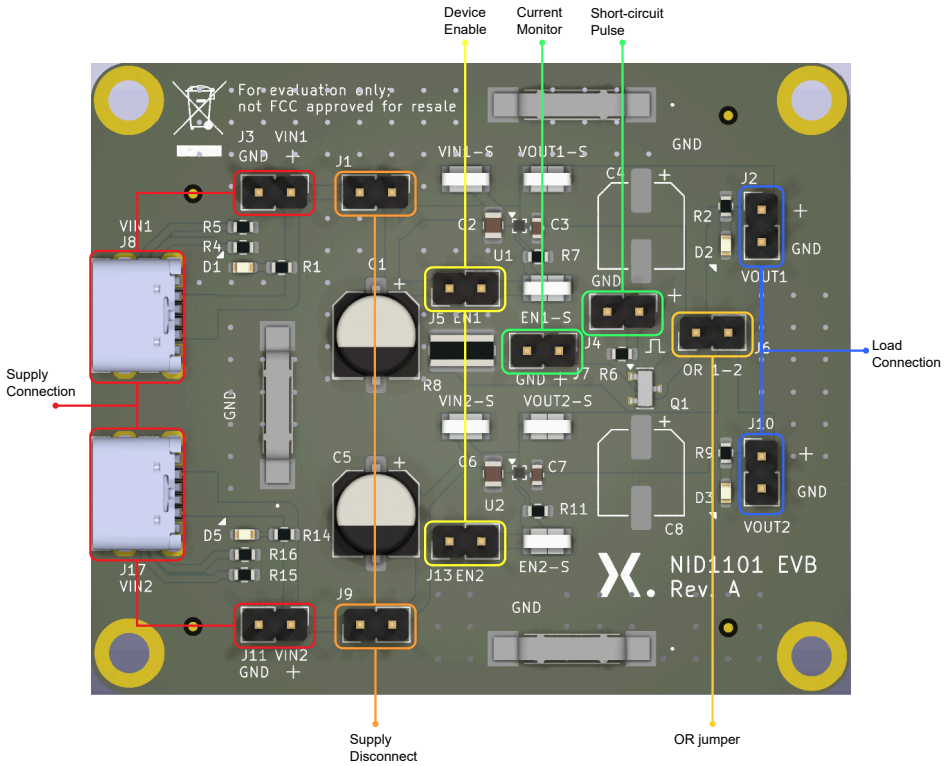
6. Quick start

By default, the PCB is configured for a dual-input OR-ing application:

When both USB-C ports are connected to power sources (for example, two separate USB ports on a PC), the port with the higher input voltage supplies the output available at V_{OUT1} (J2) and V_{OUT2} (J10). Disconnecting either input source does not interrupt the output, and the remaining source continues to provide voltage to the outputs.

7. Configuration and operation

Fig. 5 depicts the location of available jumpers, supply, and load connections.



Connection	Description	Color
J8, J17, J3, J11	Supply Connection	Red
J1,J9	Supply Disconnect	Orange
J5, J13	EN Device	Yellow
J4, J7	Short Circuit Pulse Current Sense	Green
J6	OR jumper	Gold
J2, J10	Load Connection	Blue

Fig. 5. Jumper positions and supply connections

Multiple supply inputs are available for this PCB: two USB-C ports (J8 and J17) and two headers (J3, J11). Headers J3 and J11 are in parallel with USB-C port J8 and J17 respectively and can be used to connect a battery pack or lab supply. An orange LED indicates the presence of an input voltage.

Output voltages are available at J2, J10. If present a green LED lights up.

Jumpers J1 and J9 can be used to disconnect the NID1101 from the supply or measure the supply current.

Jumpers J5, J6, and J13 are used to set the use cases in Table 4.

Table 2 and Table 3 summarize the usage of all jumpers and test points present on the evaluation PCB.

Table 2. Jumper settings

Jumper	Default position	Usage
J1	Closed	• Disconnect V_{IN1} • Measure V_{IN1} supply current
J5	Closed	Enable U1
J6	Closed	OR V_{OUT1} - V_{OUT2}
J9	Closed	• Disconnect V_{IN2} • Measure V_{IN2} supply current
J13	Closed	Enable U2

Table 3. Test points and supply I/O's

Test point	Connected to
J2	Output 1 (V_{OUT1})
J3	External supply 1 (V_{IN1})
J4	Short circuit NMOST
J7	Short circuit series resistor
J8	USB-C supply 1 (V_{IN1})
J10	Output 2 (V_{OUT2})
J11	External supply 2 (V_{IN2})
J17	USB-C supply 2 (V_{IN2})
TP1	V_{IN} U1
TP2	V_{OUT} U1
TP4	Enable U1
TP5	V_{IN} U2
TP6	V_{OUT} U2
TP8	Enable U2

Table 4 shows a summary of the jumper settings for all use cases.

Table 4. Use case jumper settings

Use case	J1	J5	J6	J9	J13
Reverse current blocking	Closed	Closed	X	Closed	Closed
Single operation	Closed	Closed	Open	Open	X
Dual OR	Closed	Closed	Closed	Closed	Closed

7.1. Reverse current blocking

Reverse current blocking remains active regardless of the device's enable state. This behavior can be confirmed by raising V_{OUT1} or V_{OUT2} typically 33 mV above V_{IN}.

7.2. Single device operation

Fig. 6 shows the board setup for operating a single device, where the enable pin is controlled by a pulse generator with the same voltage level as V_{IN1}.

Fig. 7 displays the device's startup behavior.

When V_{IN1} (5.5 V) is applied and the enable signal stays below the low threshold ($V_{EN,LO}$ = 0.4 V), the device blocks forward voltage, so V_{OUT} remains at 0 V. Once the enable signal rises above the high threshold ($V_{EN,HI}$ = 1.2 V), the device turns on. The output capacitor then charges at a controlled rate until V_{OUT} matches V_{IN1}.

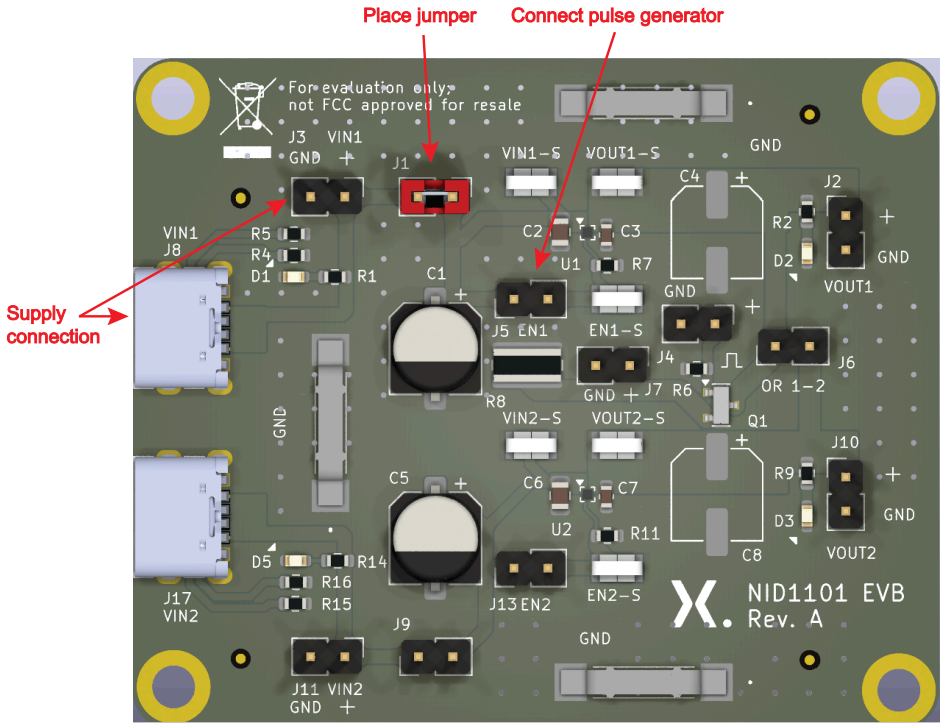


Fig. 6. Board setup for single device operation

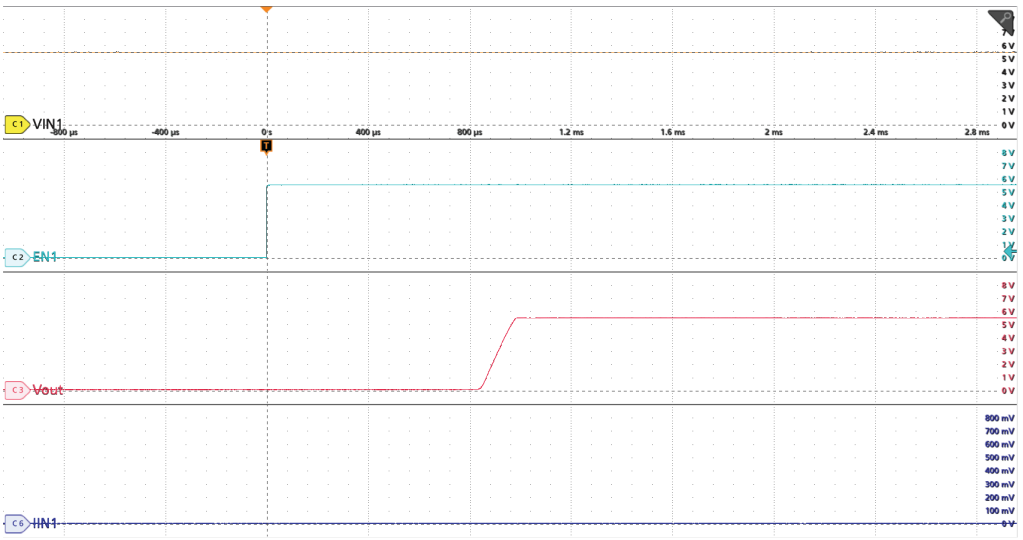


Fig. 7. Forward voltage blocking and inrush current control

7.3. Short-circuit testing

Short-circuit performance can be tested using the onboard FET. The test setup is shown in Fig. 8. Connect a pulse generator with a 10 V_{peak} square wave to connector J4. The voltage across R8 can be monitored to observe the current (10 A/V). The voltage drop across the current sense resistor can be measured at connector J7.

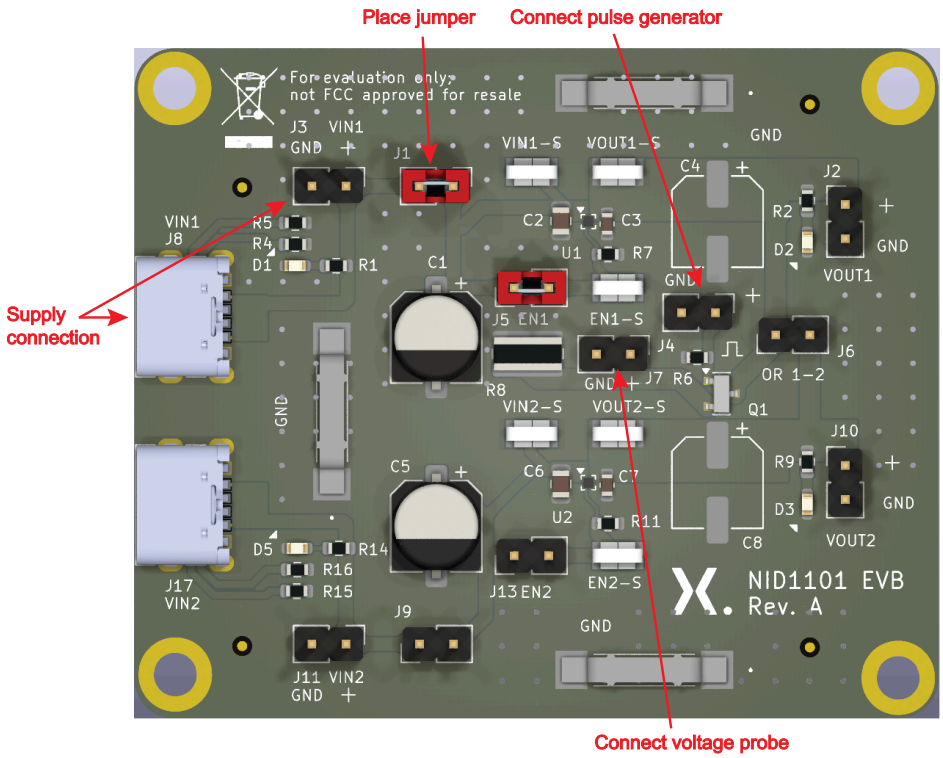


Fig. 8. Board setup for short circuit testing

Fig. 9 shows the device's short-circuit response.

At time t = 0 s, the short-circuit FET is turned on. The voltage across resistor R8 is monitored on channel 6, which represents the output current (10 A/V). When the output current exceeds the current limit (I_{LIM}), the current limiting function is activated.

If the short-circuit condition continues, the device triggers over-temperature shutdown (OTSD) and turns off the internal pass FET for protection. Once the die temperature drops below the hysteresis threshold, the internal pass FET is re-enabled. This cycle repeats if the over-temperature condition occurs again.

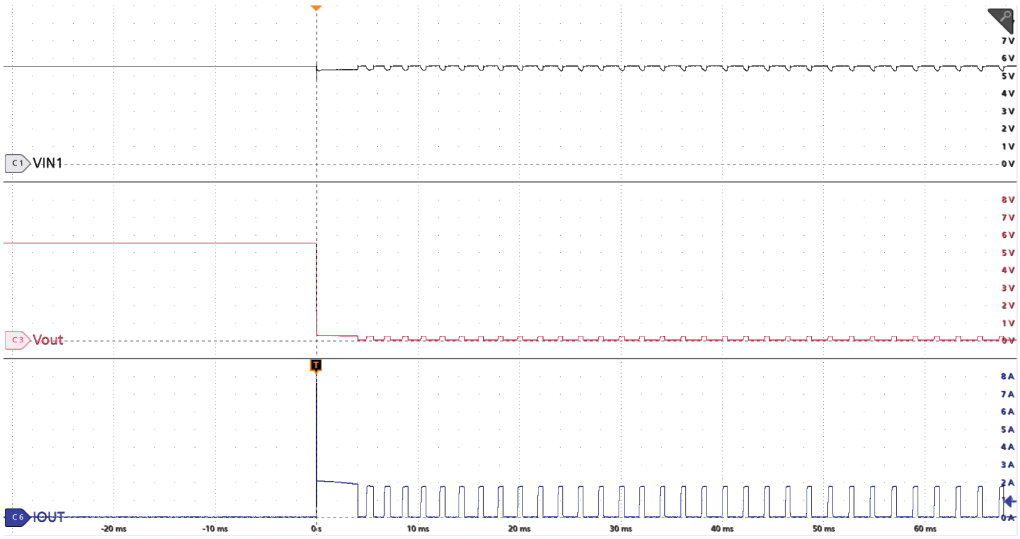


Fig. 9. Short circuit testing

7.4. Dual OR-ing

The evaluation PCB can be configured for ORing between V_{IN1} and V_{IN2}. To do this, both U1 and U2 must be enabled and connected in parallel. Enable both devices by placing jumpers on J5 and J13 and connect them in parallel by placing a jumper on J6. The board setup and jumper configurations are illustrated in Fig. 10.

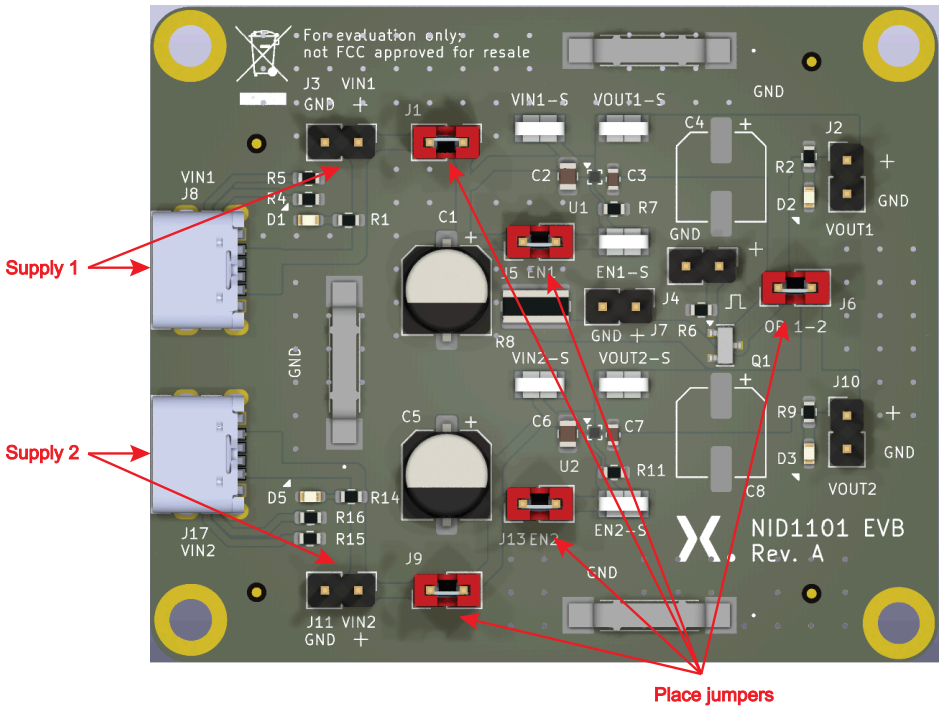


Fig. 10. Board setup for OR-ing supply 1 and supply 2

Fig. 11 shows the results when Oring two supplies.

V_{IN1} has been connected to a 5.5 V source while V_{IN2} has been connected to a 3.3 V source. Initially V_{IN1} is supplying V_{OUT}. When V_{IN1} drops below V_{IN2}, V_{IN2} takes over. If V_{IN1} rises again above V_{IN2}, the initial situation is restored.

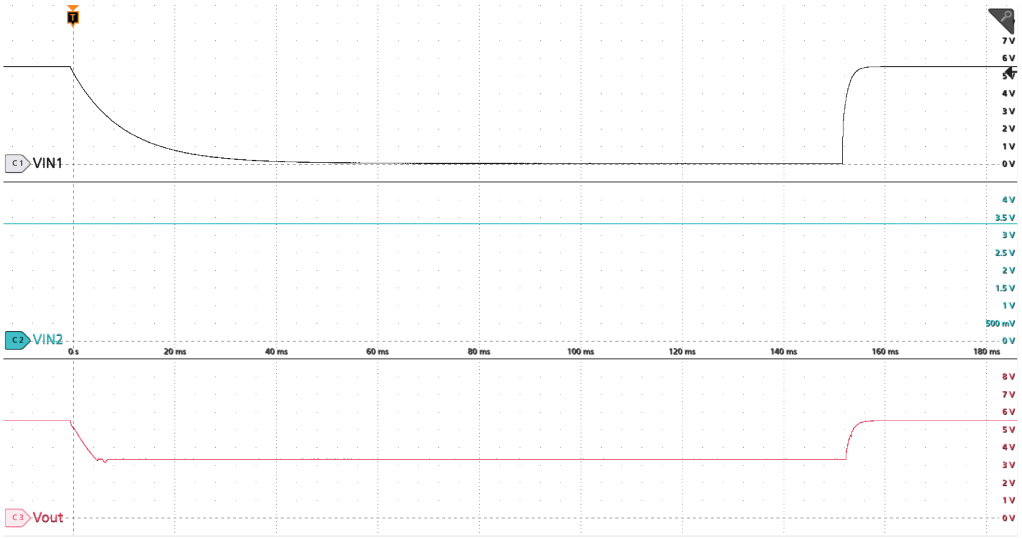


Fig. 11. Oscilloscope traces showing OR-ing between supply 1 and supply 2

8. Abbreviations

Table 5. Abbreviations

Acronym	Description
FET	Field-Effect Transistor
NMOS	N-type Metal-Oxide-Semiconductor
PCB	Printed Circuit Board
USB	Universal Serial Bus

9. Revision history

Table 6. Revision History

Revision number	Date	Description
UM90071 v.1	20251010	Initial version

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