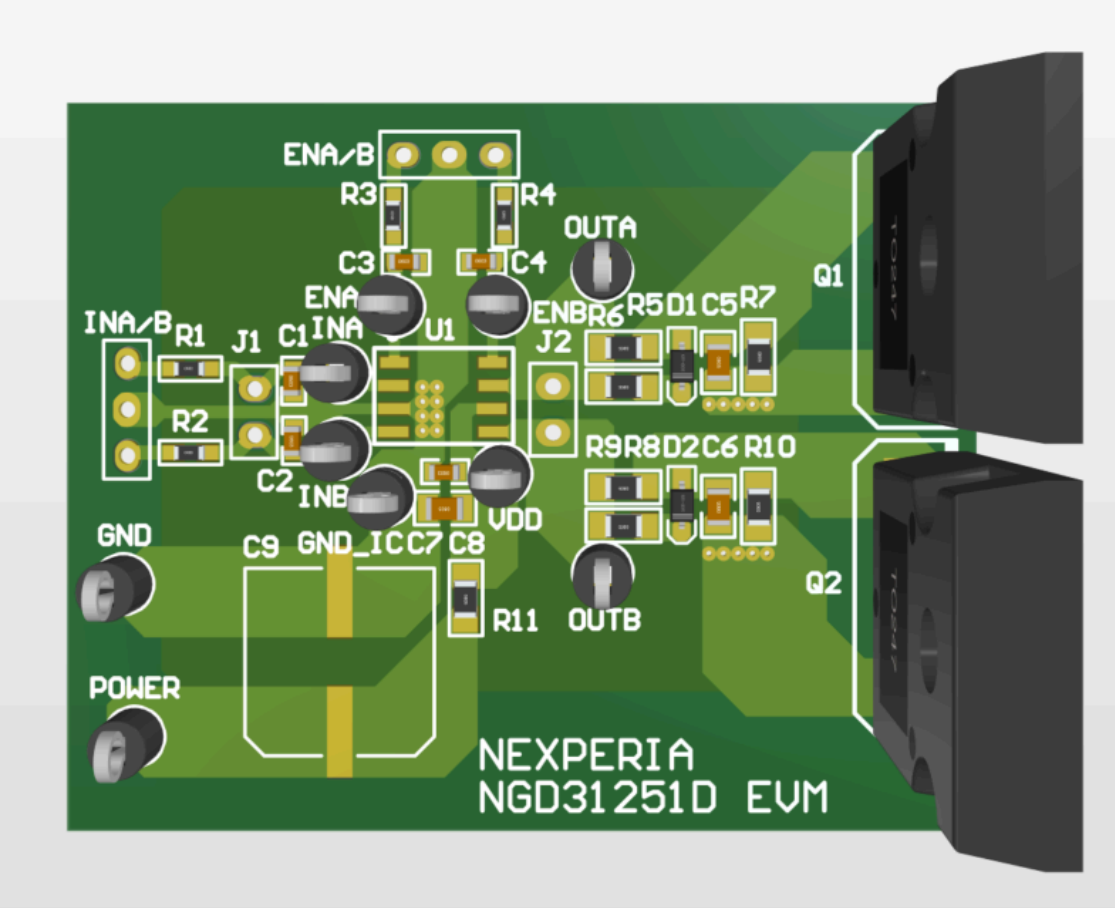
UM90060

Rev. 1 — 4 July 2025 user manual

NGD31251D 28 V, 5 A dual-channel non-isolation gate driver evaluation board



Abstract: This user manual describes the NEVB-NGD31251D. The NGD31251D is a 28 V dual-channel low-side driver with 5 A peak source and 5 A peak sink current for driving Si/IGBTs/SiC FETs. This document contains the EVB schematics, EVB configuration, bill of materials (BOM), board layout and assembly drawings.

Keywords: NGD31251D, dual-channel gate driver, evaluation board

nexperia

1. Introduction

NEVB-NGD31251D is designed for NGD31251D. It helps engineers evaluate the operation and performance of NGD31251D.

NGD31251D is a 28 V dual-channel low-side driver with 5 A peak source and 5 A peak sink current for driving Si/IGBTs/SiC FETs. NGD31251D has low propagation delay and delay matching between the two channels' rising and falling edges of the driver outputs for reliable timing of the gate-drive signals. NGD31251D inputs can tolerate signals from -10 V to 28 V, which enhances device robustness.

NEVB-NGD31251D can be used to evaluate other pin-to-pin compatible parts in the supported package.

1.1. Features

The following features are available on this EVB:

- 4.5 V to 24 V VDD power supply range
- 5 A source and 5 A sink current
- -5 V to 24 V input voltage capability
- TTL-compatible inputs
- Capacitive load, external gate drive resistor and TO-247 footprint for N-channel MOSFETs gate drive network evaluation
- Able to parallel both OUTA and OUTB channels for higher pulsed output current
- Allows quick verification of most parameters specified in the data sheet
- Its test points allow probing all the key pins of NGD31251D

1.2. Applications

NGD31251D is used in the following applications:

- Switch-mode power supplies
- Power factor correction (PFC) circuits
- Center-type synchronous rectification (SR) circuits
- DC/DC converters
- Solar power supplies

2. Schematic

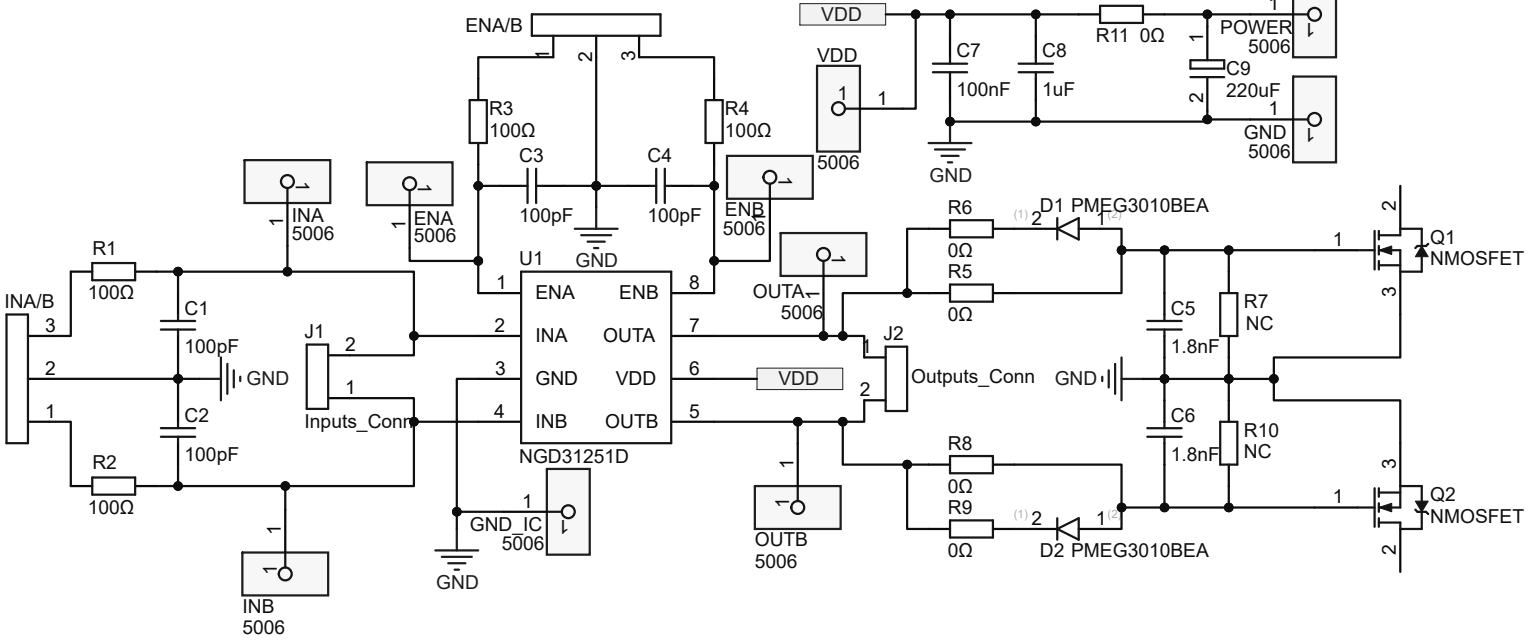


Fig. 1. NEVB-NGD31251D schematic diagram

3. General configuration and description

This section describes the connectors and test points on the EVB and how to properly connect, set up and use NEVB-NGD31251D.

3.1. Physical access

Table 1 lists the connectors and test point functionality of NEVB-NGD31251D.

Table 1. Connectors and test points

Connector	Label	Descriptions
INA/B	INA/B	Channel A and B control signal input
INA	INA	Channel A input test point
INB	INB	Channel B input test point
ENA/B	ENA/B	Channel A and B enable signal input
ENA	ENA	Channel A enable test point
ENB	ENB	Channel B enable test point
POWER	POWER	EVM power supply
GND	GND	Ground of power supply
VDD	VDD	VDD pin test point
IC_GND	IC_GND	Ground of test points
J1 and J2	N/A	These two connectors are used to make two channels operate in parallel
OUTA	OUTA	Gate driver A channel output test point
OUTB	OUTB	Gate driver B channel output test point

3.2. Test setup

The following steps show how to set up this EVB.

1. Make sure that all the output of the function generator, voltage source are disabled before connection.
2. Function generator channel A applies to pin INA.
3. Function generator channel B applies on pin INB.
4. Connect a power supply with positive voltage between Power and GND connectors, ensure that the input range is 4.5 V to 24 V.
5. Connect oscilloscope channel 1 probes to test points marked as OUTA, smaller measurement loop is preferred.
6. Connect oscilloscope channel 2 probes to test points marked as OUTB, smaller measurement loop is preferred.
7. Turn on the power supply and function generator.

4. PCB layout

Figure 2 and Figure 3 show the PCB layouts for the NEVB-NGD31251D.

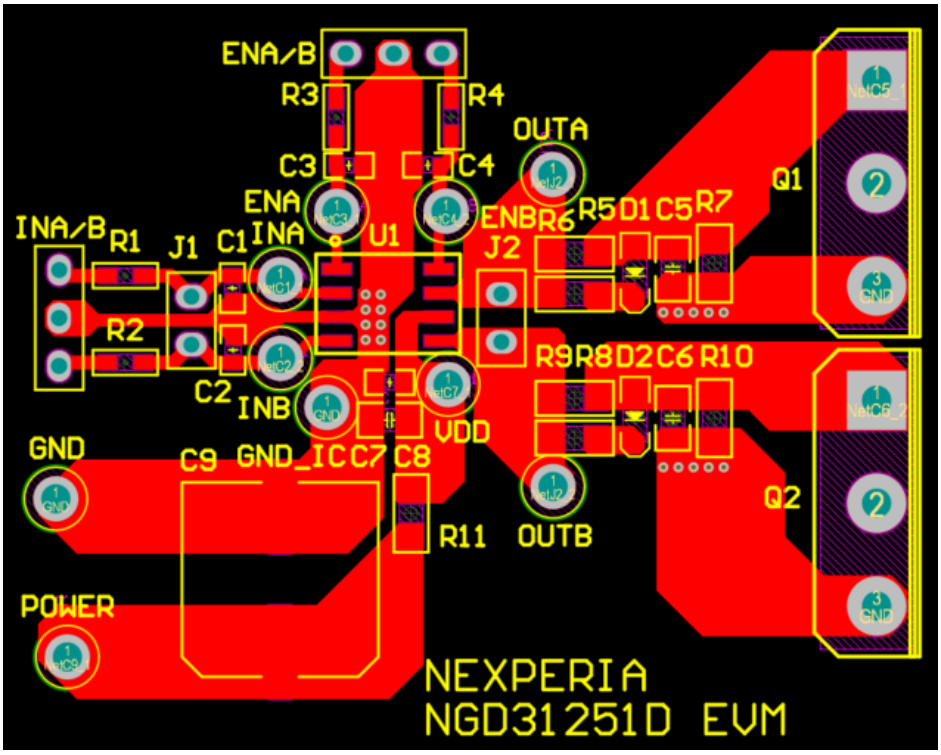


Fig. 2. NEVB-NGD31251D top layer diagram

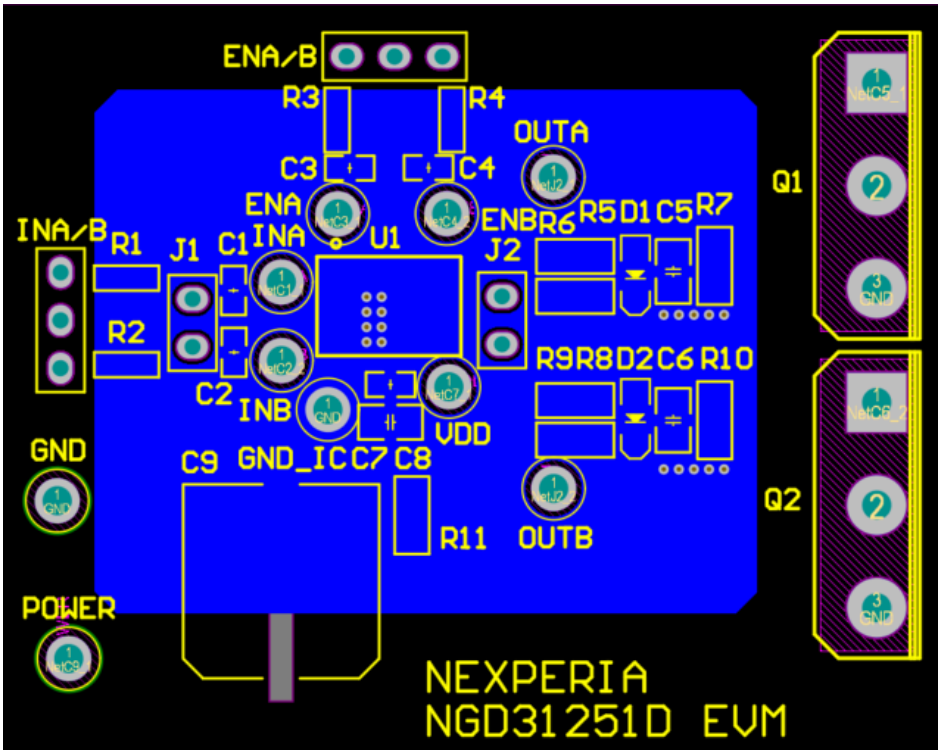


Fig. 3. NEVB-NGD31251D bottom layer diagram

5. Bill of materials

Table 2 details the bill of materials of NGD31251D EVB.

Table 2. Bill of materials (BOM)

Designator	Value	Description	Quantity	Part number	Manufacturer
C1, C2, C3, C4	100 pF	Cap Ceramic 100 pF, ±5%, 50 V, X7R Pad SMD 0603	4	CC0603KRX7R9BB101	YAGEO
C5, C6	1.8 nF	Cap Ceramic 1.8 nF, ±10%, 50 V, X7R Pad SMD 0805	2	CC0805KRX7R9BB182	YAGEO
C7	100 nF	Cap Ceramic 100 nF, ±10%, 50 V, X7R Pad SMD 0603	1	CC0603KRX7R9BB104	YAGEO
C8	1 uF	Cap Ceramic 1 µF, ±10%, 50 V, X7R Pad SMD 0805	1	CC0805KKX7R9BB105	YAGEO
C9	SMA	220 µF, ±20%, 50 V, 220 mA at 120 Hz, Pad SMD D10 mm x L10 mm	1	UWT1H221MNL1GS	Nichicon
D1, D2	30 V, 1 A	30 V, 1 A 450 mV at 1 A Pad SMD SOD-323	2	PMEG3010BEA	Nexperia
R1, R2, R3, R4	100 Ω	RES Thick Film, 100 Ω, ±1%, 100 mW, 200 ppm/°C, 0603	1	RC0603FR-07100RL	YAGEO
R5, R8	2.2 Ω	RES Thick Film, 2.2 Ω, ±1%, 125 mW, 200 ppm/°C, 0805	2	RC0805FR-072R2L	YAGEO
R6, R9, R11	0 Ω	RES Thick Film, 0 Ω, ±1%, 125 mW, 200 ppm/°C, 0805	3	RC0805FR-070RL	YAGEO
U1	-	28 V, 5 A dual channel low side gate driver	1	NGD31251D	Nexperia
Q1, Q2	NC	-	-	-	-
INA, INB, ENA, ENB, OUTA, OUTB, VDD, POWER	TH	PC test point compact	8	5005	Keystone Electronics
GND_IC, GND	TH	PC test point compact	2	5006	Keystone Electronics
INA/B, ENA/B	TH	1 x 3P, pitch = 2.54 mm	2	PZ254V-11-02P	XFCN
J1, J2	TH	1 x 2P, pitch = 2.54 mm	2	PZ254V-11-02P	XFCN

6. Revision history

Table 3. Revision history

Revision number	Date	Description
UM90060 v. 1	20250704	Initial version

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