



UM90019

Dual output LCD bias power supply evaluation module

Rev. 1 — 24 January 2024

user manual

Document information

Information	Content
Keywords	NEX10000UB and NEX10001UB evaluation module
Abstract	This user's guide describes the NEX10000UB and NEX10001UB evaluation module. NEX10000UB and NEX10001UB are designed to provide power supply with positive and negative output voltage for TFT-LCD panel. This document contains the EVM schematics, EVM configuration, bill of materials (BOM), board layout drawing and assembly drawing.

1. Introduction

This evaluation module (EVM) is designed for NEX10000UB and NEX10001UB, it can generate one positive output voltage and one negative output voltage. The EVM has I²C interface, which is used to change the output voltage. For easy evaluate this EVM board, you may need a tool to send command through I²C.

2. Features

The following features are available on this EVM:

- Input voltage range: 2.7 V to 5.0 V
- Positive output range (V_{POS}):
 - NEX10000UB: 4 V to 6 V
 - NEX10001UB: 4 V to 6.5 V
- Negative output range (V_{NEG}):
 - NEX10000UB: -4 V to -6 V
 - NEX10001UB: -4 V to -6.5 V
- Maximum output current:
 - NEX10000UB: 80 mA
 - NEX10001UB: 220 mA
- Use jumper to enable or disable Positive output and Negative output
- I²C interface to configure the output voltage

3. Application

- The EVM is used in the following applications:
 - Smart Phone TFT LCD
 - Tablet TFT LCD

4. Schematic

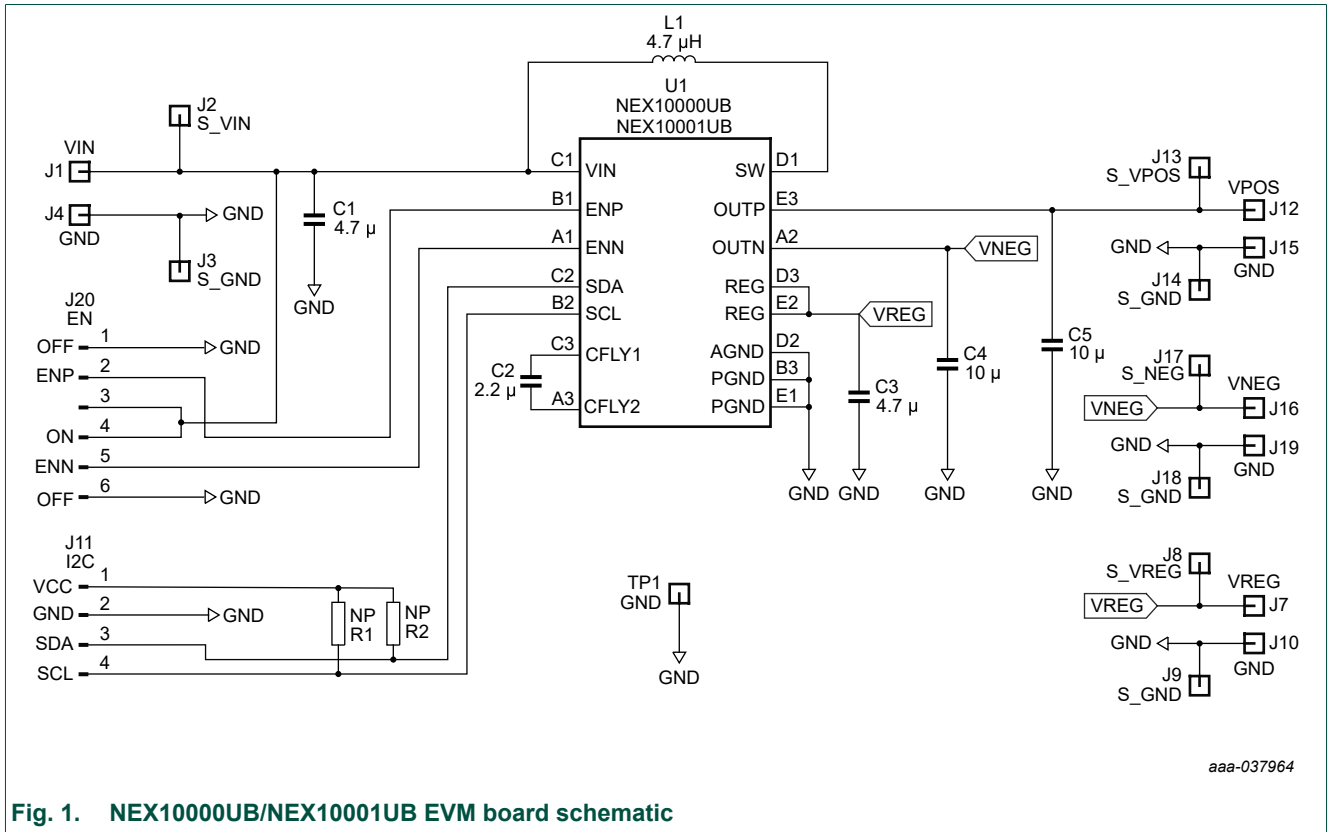


Fig. 1. NEX1000UB/NEX1001UB EVM board schematic

5. General configuration and description

This section describes the connectors, jumpers, and test points on the EVM and how to properly connect, set up and use the NEX10000UB/NEX10001UB EVM.

5.1. Physical access

[Table 1](#) lists the NEX10000UB/NEX10001UB EVM connector, jumper and test points configuration.

Table 1. Connectors

Connector	Label	Descriptions
J1	VIN	Power input for this board
J2	S_VIN	V_{IN} sense and test point
J3, J9, J14, J18	S_GND	GND sense pins and test point
J4, J10, J15, J19, TP1	GND	Power ground
J7	VREG	V_{REG} output pin
J8	S_VREG	V_{REG} sense pin and test point
J11	I2C	I ² C connector, includes SDA, SCL, V_{CC} and GND. V_{CC} is external pull-up voltage, if needed.
J12	VPOS	V_{POS} output pin
J13	S_VPOS	V_{POS} sense pin and test point
J16	VNEG	V_{NEG} output pin
J17	S_NEG	V_{NEG} sense pin and test point
J20	EN	Enable connector, includes ENN, ENP, GND and High (V_{IN}). User can use jumper to enable and disable V_{POS} and V_{NEG}

5.2. Test setup

[Fig. 2](#) shows a typical setup for NEX10000UB/NEX10001UB EVM, apply 2.7 V to 5.0 V input voltage to V_{IN} , then connect the enable jumper, the output will have default 5.4 V on V_{POS} and -5.4 V on V_{NEG} . You can connect I²C master to SDA and SCL, then you can send I²C command to NEX10000UB/NEX10001UB to change the output voltage and other configurable function. [Table 2](#) shows the register map of NEX10000, [Table 3](#) shows the register map of NEX10001. For the details, you can refer to the data sheet of NEX10000UB and NEX10001UB.

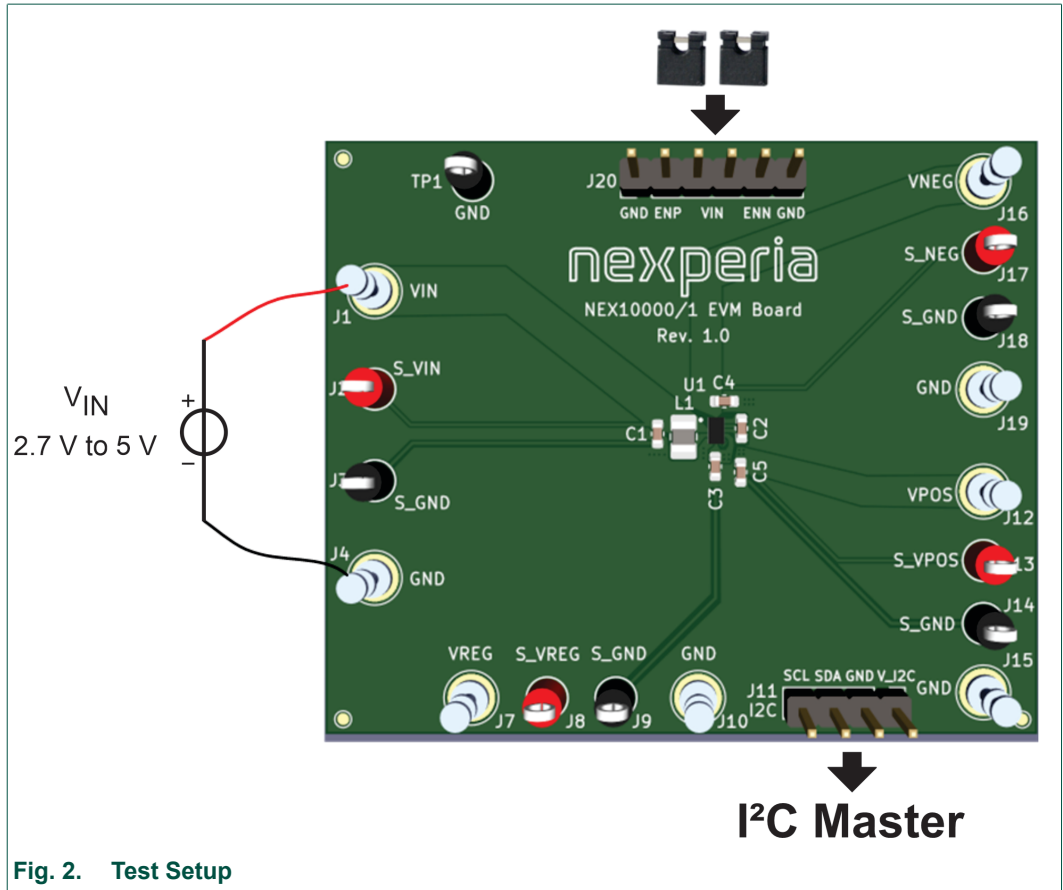


Fig. 2. Test Setup

Below is the register map of NEX10000UB and NEX10001UB.

Table 2. NEX10000UB register map

Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	V _{POS} Register	R/W	Reserved			V _{POS} [4:0]				0x0E	
0x01	V _{NEG} Register	R/W	Reserved			V _{NEG} [4:0]				0x0E	
0x02	Vendor ID	R/W	Reserved						11	0x03	

Table 3. NEX10001UB register map

Address	Register Name	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
0x00	V _{POS} Register	R/W	Reserved			V _{POS} [4:0]				0x0E	
0x01	V _{NEG} Register	R/W	Reserved			V _{NEG} [4:0]				0x0E	
0x02	CL & Vendor ID	R/W	Reserved			LDO_CL	Reserved		11	0x03	

6. Board layout

Below is the board layout for different layer.

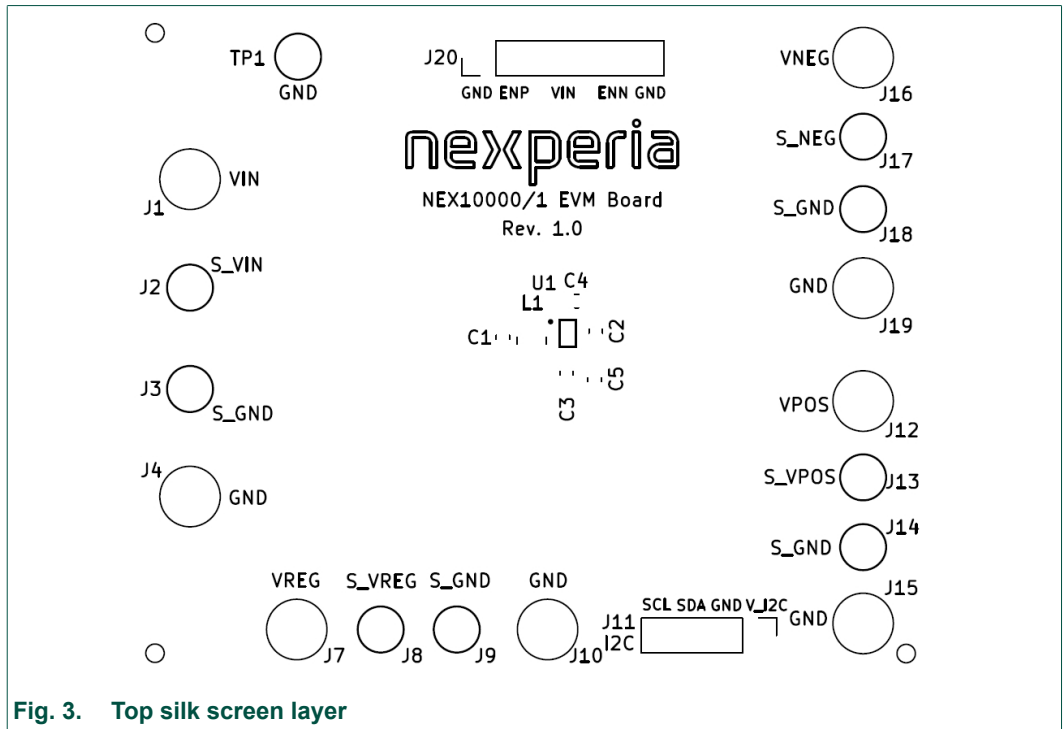


Fig. 3. Top silk screen layer

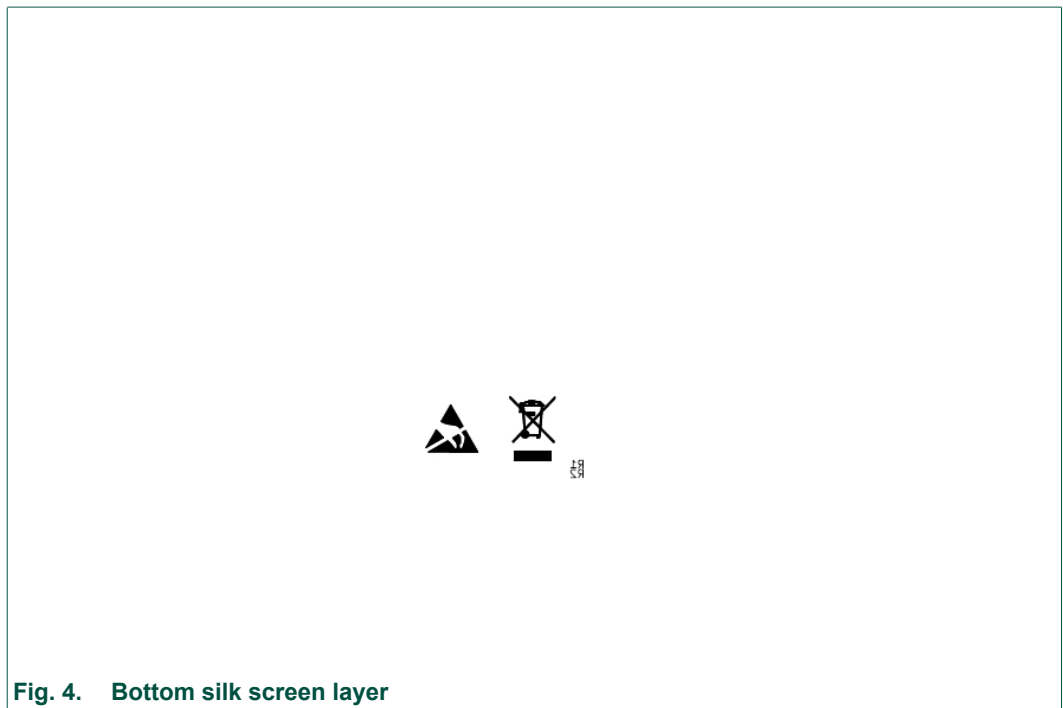


Fig. 4. Bottom silk screen layer

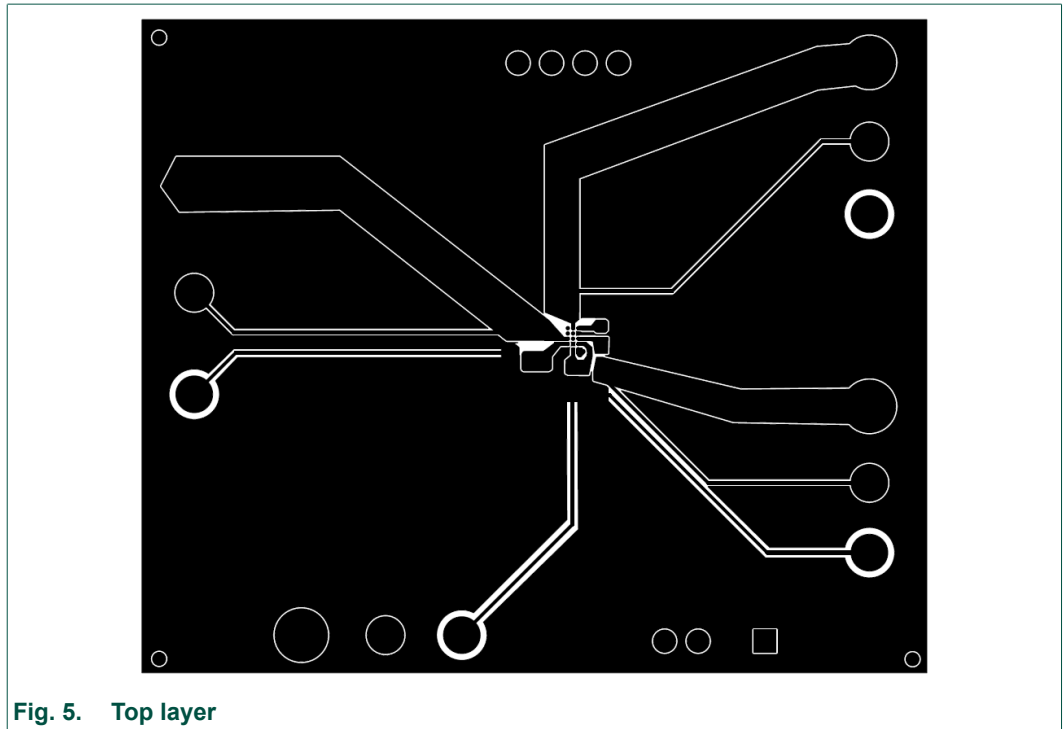


Fig. 5. Top layer

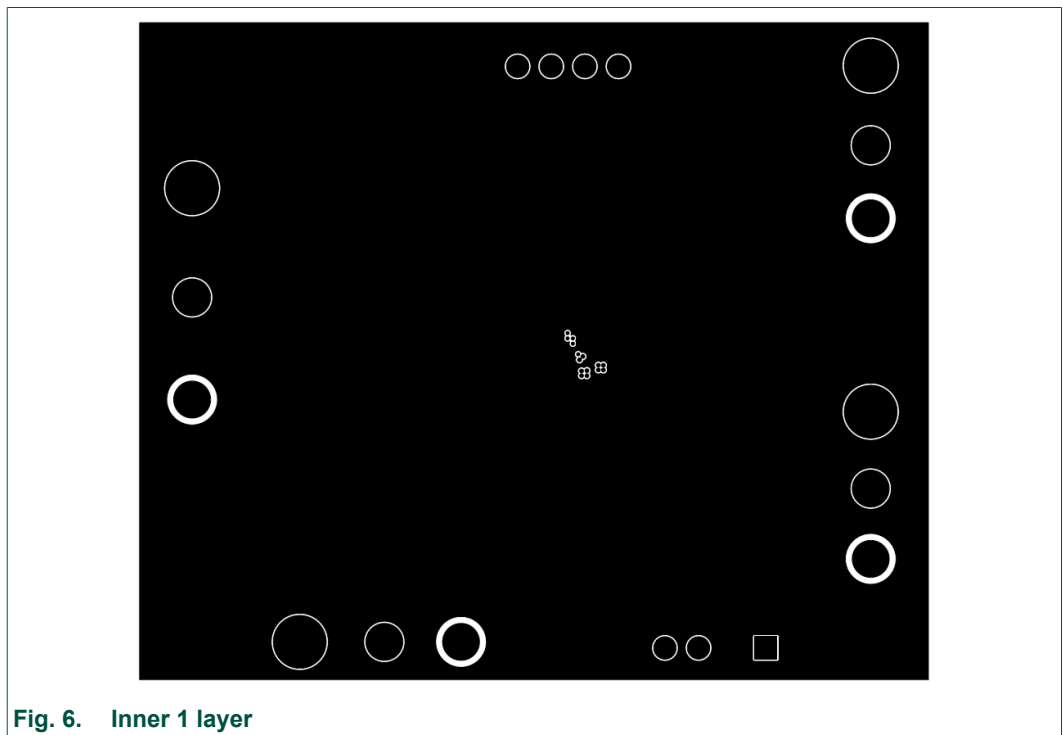


Fig. 6. Inner 1 layer

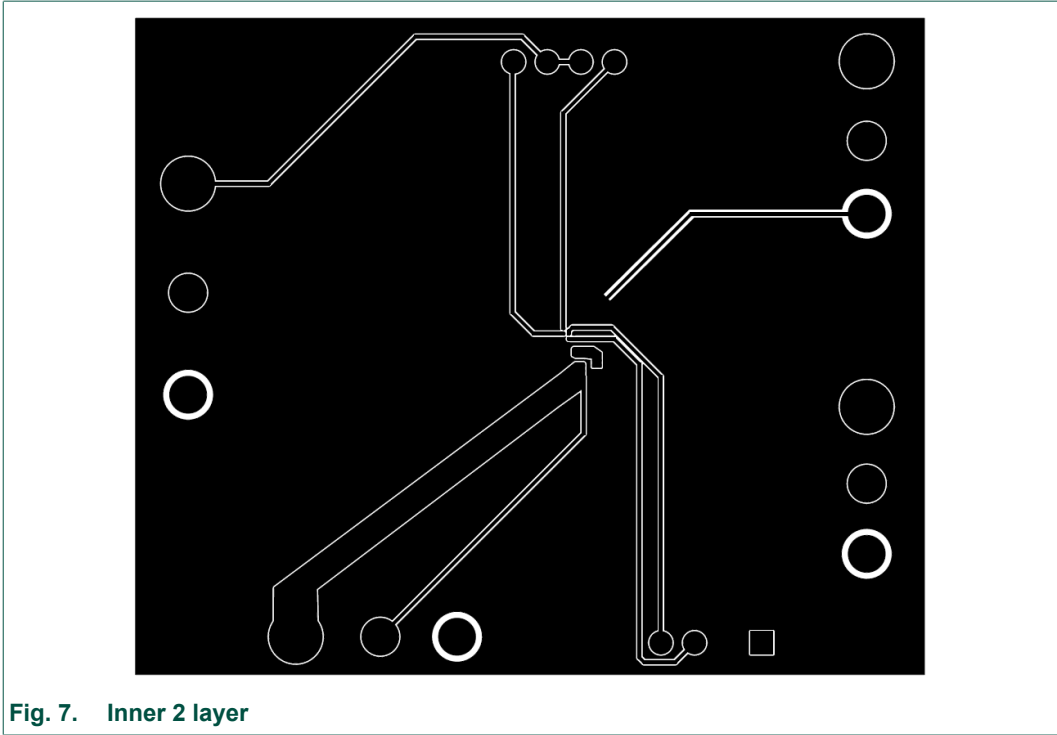


Fig. 7. Inner 2 layer

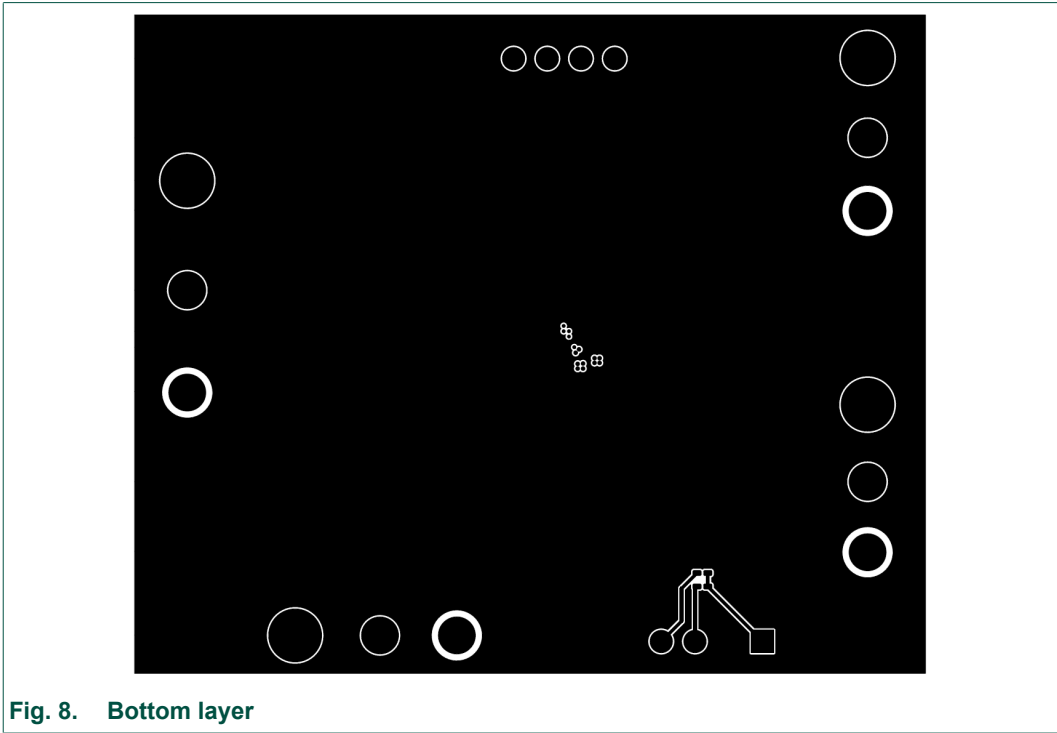


Fig. 8. Bottom layer

7. NEX1000UB and NEX10001UB EVM board Bill of Materials (BOM)

Table 4. NEX1000UB and NEX10001UB EVM board Bill of Materials

References	Value	Footprint	Quantity	Part Number	Manufacturer
NEX1000UB and NEX10001UB EVM board [1]					
C1, C3	4.7 μ F	C_0603_1608Metric	2	C1608X5R1E475K080AC	TDK
C4, C5	10 μ F	C_0603_1608Metric	2	C1608X5R1E106K080AC	TDK
C2	2.2 μ F	C_0603_1608Metric	1	C1608X5R1C225KTK00E	TDK
R1, R2	NP	R_0201_0603Metric_Pad0.64x0.40mm_HandSolder	2	not place	
L1	4.7 μ H	L_1008_2520Metric_Pad1.43x2.20mm_HandSolder	1	TMS252012ALM-4R7MTAA	TDK
U1	NEX1000UB/NEX10001UB	NEX1000UB/NEX10001UB (WLCSP15)	1	NEX1000UB/NEX10001UB	Nexperia
TP1	GND	TestPoint_Keystone_5005-5009_Compact	1	Keystone 5006	Keystone
J3, J9, J14, J18	S_GND	TestPoint_Keystone_5005-5009_Compact	4	Keystone 5006	Keystone
J4, J10, J15, J19	GND	TestPoint_Loop_D3.80mm_Drill2.5mm	4	Keystone1502-2	Keystone
J1	VIN	TestPoint_Loop_D3.80mm_Drill2.5mm	1	Keystone1502-2	Keystone
J2	S_VIN	TestPoint_Keystone_5005-5009_Compact	1	Keystone 5005	Keystone
J7	VREG	TestPoint_Loop_D3.80mm_Drill2.5mm	1	Keystone1502-2	Keystone
J8	S_VREG	TestPoint_Keystone_5005-5009_Compact	1	Keystone 5005	Keystone
J11	I2C	PinHeader_1x04_P2.54mm_Vertical	1	Header, 2.54 mm, 4x1, Gold, TH	Würth Elektronik
J12	VPOS	TestPoint_Loop_D3.80mm_Drill2.5mm	1	Keystone1502-2	Keystone
J13	S_VPOS	TestPoint_Keystone_5005-5009_Compact	1	Keystone 5005	Keystone
J16	VNEG	TestPoint_Loop_D3.80mm_Drill2.5mm	1	Keystone1502-2	Keystone
J17	S_NEG	TestPoint_Keystone_5005-5009_Compact	1	Keystone 5005	Keystone
J20	EN	PinHeader_1x06_P2.54mm_Vertical	1	Header, 2.54 mm, 6x1, Gold, TH	Würth Elektronik
C2 and C3 value for NEX10001UB EVM board [1]					
C2	4.7 μ F	C_0603_1608Metric	1	C1608X5R1C225KTK00E	TDK
C3	10 μ F	C_0603_1608Metric	1	C1608X5R1E106K080AC	TDK

[1] For NEX10001UB: Due to the output current of 220 mA, some capacitor values (C2 and C3) are different.

8. Revision history

Table 5. Revision history

Revision number	Date	Description
UM90019 v.1	20240124	Initial version

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