UM90013

NCA95xx EVB GPIO expander evaluation board

Rev. 1.0 — 22 June 2022 user manual

Document information

Information	Content
Keywords	General Purpose Input/Output (GPIO) Expander, Evaluation Board (EVB), I²C-Bus, write and read operation, interrupt output
Abstract	The NCA95xx evaluation board allows to perform various application tests and device measurements. The board can be operated with a supply voltage from 1.6 V to 5.5 V and features 16 GPIO pins, clustered into two ports, which can be programmed via I²C bus to work as digital output or as input. An interrupt output indicates that an input state has changed.

1. Introduction

1.1. Short description

The NCA95xx EVB is a PCB designed for the Nexperia I²C controlled GPIO expander IC family. The board is a 2-layer PCB with a solid ground bottom layer. The NCA95xx IC can either be mounted directly or via a 24-pin piggyback sub-module which can be plugged into the board for an easy exchange of test components. The 16 GPIO pins of the expander can be connected to red LEDs via two banks of switches. The LEDs have series resistors to ground and can be turned on via I²C-Bus commands if a GPIO is defined as output and programmed to high state. The port pins can be accessed via jumper rows and be used as digital inputs for read-back of logic state. The I²C addresses can be configured via jumpers. Power of the EVB can be turned on and off with a switch. The module features reverse polarity protection for the supply voltage as well as a current back-drive protection.

The board provides convenient test points for GND, I²C-Bus signals SCL and SDA as well as an interrupt open drain output. The EVB can be used for the GPIO expander derivatives NCA9555, NCA9539 and NCA9595.

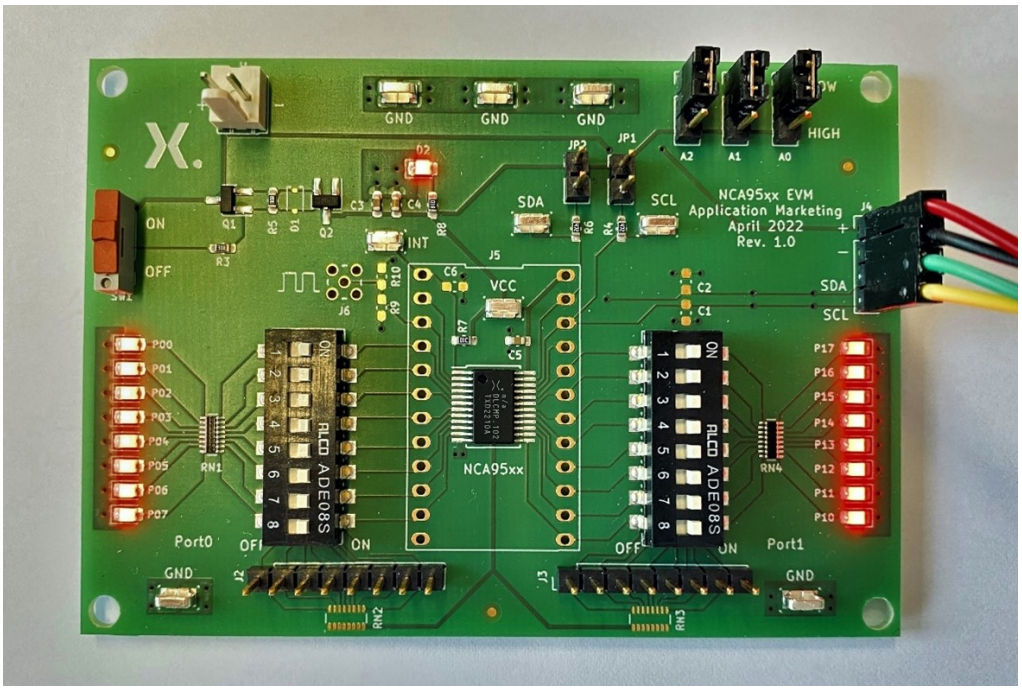

Fig. 1. NCA95xx EVB - evaluation board for GPIO expander IC NCA95xx

The list below gives a summary of the key parameters and most important features of the NCA95xx GPIO expander IC evaluation board:

- EVB name = NCA95xx EVM
- Device = NCA 95xx
- Input voltage = 1.6 V to 5.5 V
- I²C to parallel port expansion
- Number of GPIOs = 2 ports with 8 bits
- Current drive capability = ± 50 mA
- I²C interface, Fast-Mode 400 kHz
- Open-drain active-low interrupt output
- Configurable slave address via 3 selection pins (2 pins for NCA9539)
- Low-active reset input (NCA9539)
- Polarity inversion register (for read operation)

Further details about the specification and parameters of NCA9555, NCA9535 and NCA9595 can be found in the related data sheets.

1.2. Features

- Input voltage can be supplied via the connector J1. SW1 controls a back-drive protected load switch for the supply voltage. There is a green LED indicator for the on-state. Vin can range from 1.6 V to 5.5 V.
- I²C bus can be connected via connector J4. SCL and SDA have pull-up resistors R4 and R6. There are optional footprints for series resistors in the I²C bus lines as well as capacitors that can be assembled connected to ground.
- JP3 to JP5 allow up to 8 different slave addresses to be configured.
- Decoupling capacitors are connected to Vin at the input of the EVB and close to the GPIO expander IC.
- 16 red LEDs can be used as load for the outputs configured. Resistor arrays guarantee a decent LED current for the whole supply voltage range. Switches SW2 and SW3 allow the LEDs to be connected to the ports.
- For the NCA9539, pin 3 is an active-low reset input. J6 is an SMA connector for dynamic tests of reset function.
- Multiple GND connectors are provided for a convenient testing with TP5 to TP9.
- Connectors for oscilloscope probe hook tips are provided for the I²C signals SCL, SDA and the interrupt output INT.
- Digital Input signals can be connected via the pin rows J2 and J3. J2 is connected to port 0, J3 to port 1. The resistor arrays provide pull-up resistors for the port pins. NCA9555 and NCA9539 have integrated 100 kΩ pull-ups whereas the derivative NCA9535 has no such default termination.

2. Schematic diagram

Fig. 2 shows the schematic diagram of the NCA95xx EVB evaluation board. The components, solder pins, connectors and switches described in the features list can be found here.

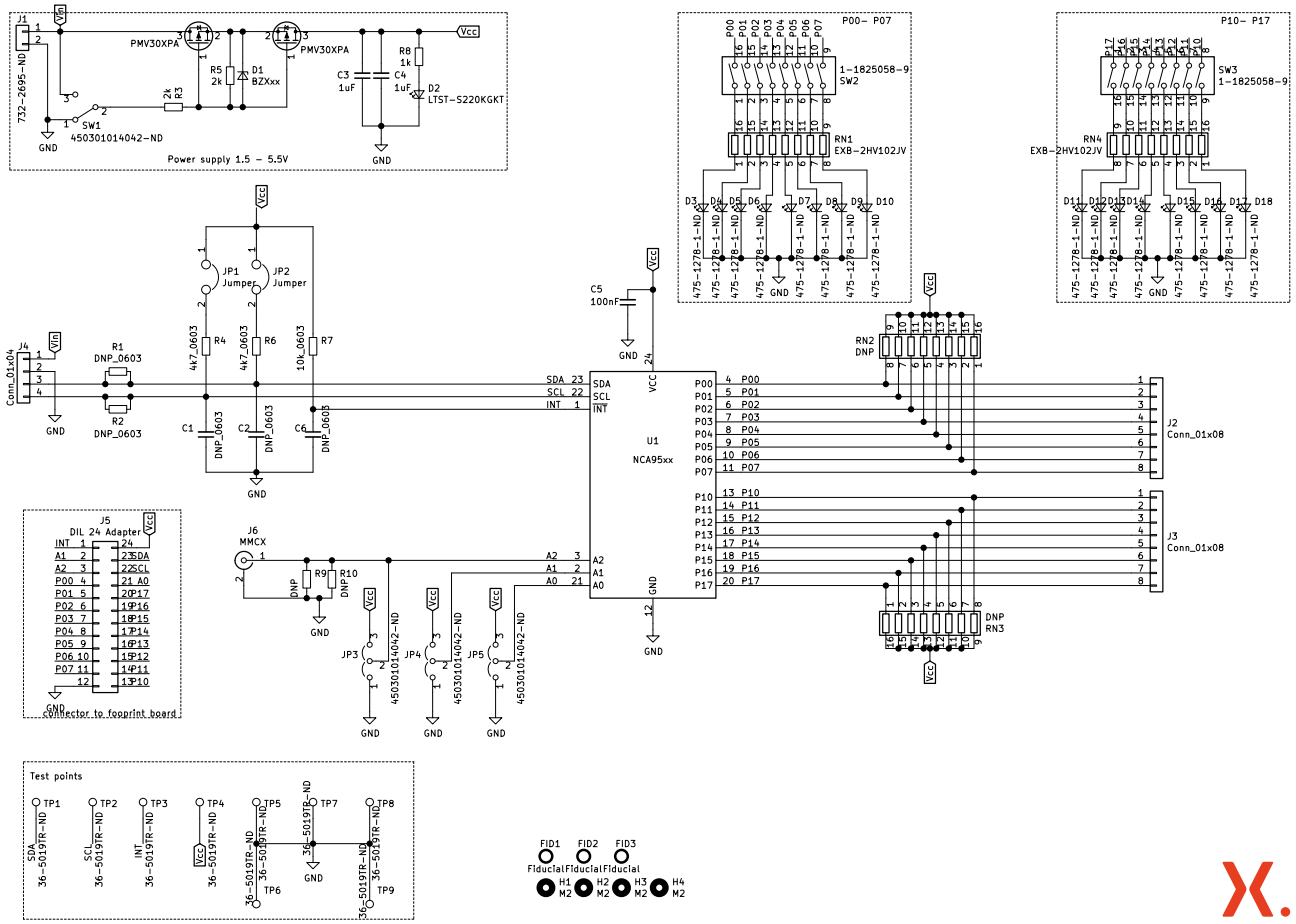

Fig. 2. NCA95xx EVB schematic diagram

3. PCB layout

Fig. 3 and Fig. 4 depicts the PCB layout of the NCA95xx EVB. The PCB has two layers, the top layer is shown in red, the bottom layer (ground plane) is shown in green.

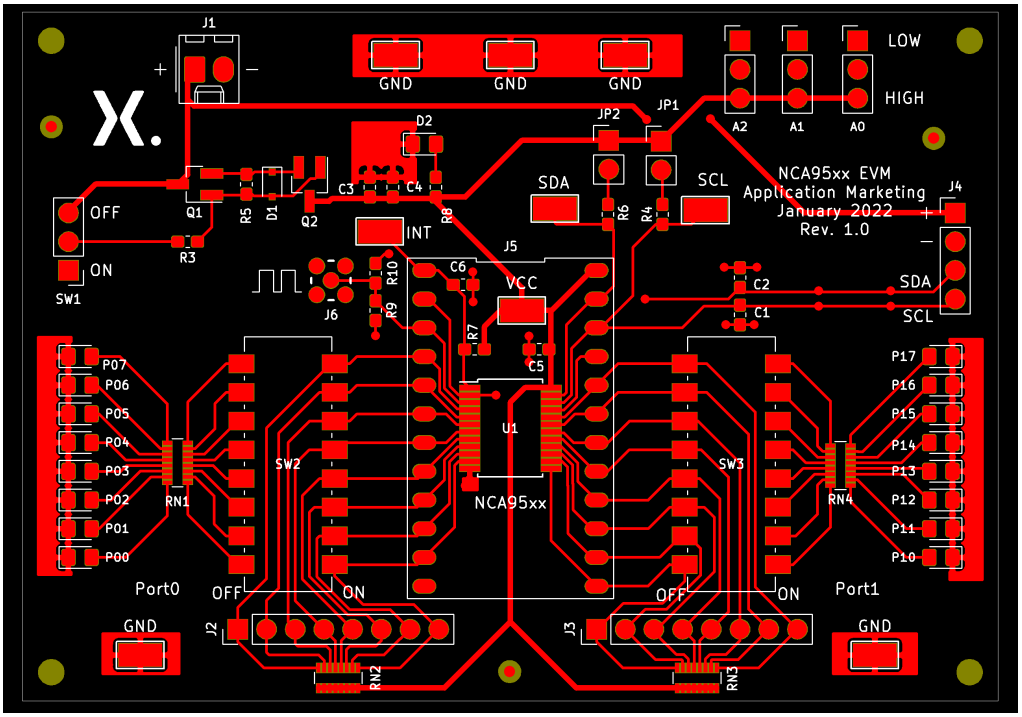

Fig. 3. NCA95xx EVB top layer PCB layout

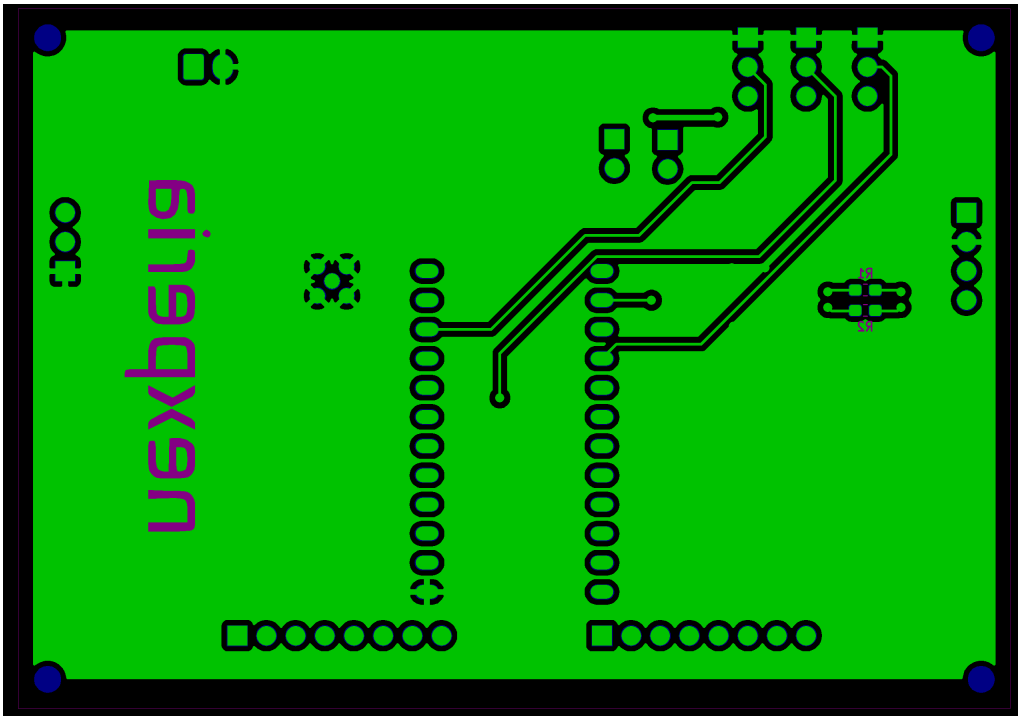

Fig. 4. NCA95xx EVB bottom layer PCB layout

4. Set up and operation

The NCA95xxEVB board is quite easy to set up and operate. This chapter gives some instructions for proper use.

4.1. Input supply

The input voltage source Vin is connected to the connector J1. The board can operate in a voltage range from 1.65 V up to 5.5 V. The EVB is turned on via the switch SW1 which controls a back-drive protected load switch realized with the back-to-back P-channel FETs Q1 and Q2. An LED indicates an activated board. Maximum current consumption is created at the maximum Vin level of 5.5 V if all LEDs attached to the two ports are activated. This is the case if all outputs are programmed to high state and all switches of SW2 and SW3 are closed.

If external loads are connected via the pin rows J2 and J3, current consumption must be calculated accordingly.

4.2. I²C Bus connectors

An I²C master device can be connected via J4 which provides connection pins for the I²C bus clock signal SCL, the data signal SDA, as well as a ground pin and a Vin pin.

Note: the board can be supplied via J4 as an alternative to the connector J1 but in this case it is important to check that the connected I²C master hardware is able to provide enough current.

TP1 (SDA) and TP2 (SCL) provide convenient eyelet connectors for oscilloscope probes.

4.3. Address selection

Via the jumpers J3, J4 and J5 an I²C address in the range from 0x20 to 0x27 can be selected for NCA4555 and NCA4535. NCA4539 provides 4 addresses from 0x20 to 0x23 only. The pin A2 is used as low active reset for this derivative.

4.4. Low active Interrupt

If the logic state of any input has changed, the open drain output INT_NOT changes from high state to low state. This signal of NCA95xx is provided at the eyelet connector TP3. It can be connected to µ-controllers as interrupt signal in order to trigger a read back of the state of the ports. With the read operation, the interrupt gets cleared.

If the ports change back to the prior state before a read operation was performed, the interrupt is cleared. The GPIO expanders have no register to store, for which port bits changes had happened.

4.5. Port connectors

The pin row J2 allows connections to port 0 whereas pin row J3 provides access to port 1. These connectors can be used to measure the voltage of the GPIO pins or for connecting of external loads. Resistor arrays RN2 and RN3 act as external pull-ups for the ports as mounting option. NCA9555 and NCA9539 have integrated pull-up resistors to prevent floating digital inputs. For The NCA9535 there is no internal termination. This is because integrated resistors create extra current if GPIOs are used as outputs and thus deteriorate power efficiency. NCA9595 provides an additional register pair for port0 and port 1 to connect or disconnect an internal pull-up resistor.

Via the switches SW2 and SW 3 red LEDs can be connected to the port pins. If the pins are configured as inputs, the LEDs get illuminated weakly via the integrated pull-up resistors. At minimum VCC the forward voltage of the LEDs cannot be reached and there is no current flow hence the LEDs will not be lit.

5. Software Control of the EVB via I²C-Bus

5.1. Device address description

Fig. 5 shows the structure of the NCA9555 slave address. The LSB is at low state for write operation and high state for read operation. The residual 7 bits define the slave address. The three last significant bits A0, A1 and A2 allow a selection from 8 options as depicted in Table 1.

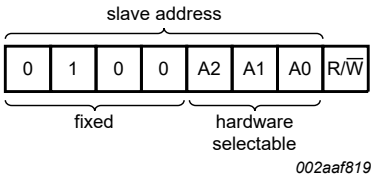

Fig. 5. NCA95xx device address

Table 1. Configuration options for NCA9555 device address

A2	A1	A0	Address (hex)
0	0	0	0x20
0	0	1	0x21
0	1	0	0x22
0	1	1	0x23
1	0	0	0x24
1	0	1	0x25
1	1	0	0x26
1	1	1	0x27

5.2. Pointer registers

In the I²C communication to the GPIO expanders first a command byte must be sent which points to 8 registers. The values 0x00 to 0x07 are used and supported only. If an illegal value is transmitted this message is not acknowledged by the NCA95xx.

Table 2. Command byte

Pointer Register bits – NCA95xx								Register	Protocol	Power-up default
B7	B6	B5	B4	B3	B2	B1	B0			
0	0	0	0	0	0	0	0	Input Port 0	Read byte	XXXX XXXX
0	0	0	0	0	0	0	1	Input Port 1	Read byte	XXXX XXXX
0	0	0	0	0	0	1	0	Output Port 0	R/W byte	1111 1111
0	0	0	0	0	0	1	1	Output Port 1	R/W byte	1111 1111
0	0	0	0	0	1	0	0	Polarity Inv 0	R/W byte	0000 0000
0	0	0	0	0	1	0	1	Polarity Inv 1	R/W byte	0000 0000
0	0	0	0	0	1	1	0	Config Port 0	R/W byte	1111 1111
0	0	0	0	0	1	1	1	Config Port 1	R/W byte	1111 1111
0	0	0	0	1	0	0	0	Pull up Res 0*	R/W byte	0000 0000
0	0	0	0	1	0	0	1	Pull up Res 1*	R/W byte	0000 0000

* registers present in NCA9595 only

Table 2 lists the valid command byte values. The registers in the NCA95xx are provided as pairs for port 0 and port 1 always. Registers 0x00 and 0x01 are read-only registers for the logic states

of the two ports. The next two registers 0x02 and 0x03 define the logic state of an output. Via the registers 0x04 and 0x05 a mask for polarity inversion of input bits can be defined. Registers 0x06 and 0x07 configure the bits of each port to an input or output. Registers 0x02 to 0x07 can be written as well as read. For NCA9595 this is the case from register 0x02 to 0x09 (see Table 2).

NCA45xx supports an auto-increment for read and write operations within a pair of registers for port 0 and port 1. If the pointer register is set to 0x02 and 2 more bytes are transmitted, the output states of port 0 and port 1 are defined. If additional bytes are sent the pointer toggles between port 0 and port 1 but does not direct to following register pairs. After writing of registers, these can be read back directly, because the pointer will still point to the prior processed register pair. If an odd number of bytes was transmitted, the next byte will be read. It is most convenient to communicate with 2 data bytes following the pointer definition to port 0 always in the I²C communication.

The NCA95xx has a power-on state with all GPIOs configured as inputs. In the right column of Table 2 the start conditions are depicted.

5.3. Input port register pair (0x00, 0x01)

The input port registers return the logic state of the related port pins regardless if a pin is configured as an input or output. With the read-back of output pins, failures in a hardware can be detected like a short circuit at an output.

Table 3. Input port 0 register (address 0x00)

Bit	7	6	5	4	3	2	1	0
Symbol	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X

The input port read registers cannot be written. Table 3 and Table 4 show the bit assignment in the two read registers. The default status X means that there is no power-on state. If a read operation is done after power on without further register changes, the actual state of all GPIOs pins which are inputs as default state can be derived.

Before starting a read operation the command byte had to be programmed to 0x00 or 0x01. After this the input port bytes can be read back

Table 4. Input port 1 register (address 0x01)

Bit	7	6	5	4	3	2	1	0
Symbol	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

5.4. Configuration register pair (0x06, 0x07)

With the configuration registers it can be defined if a GPIO pin is an input or an output. As power-on and default state the ports are defined as inputs. For the NCA9555 all the port pins start with a logic high state supported from the integrated pull-up resistors unless they are forced to low state externally. Programming a bit to 0 activates the push-pull stage at the GPIO and the port pin becomes an output. If a control bit is set to 1, the related GPIO pin works as an input.

Table 5. Configuration port 0 register (address 0x06)

Bit	7	6	5	4	3	2	1	0
Symbol	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1

Table 6. Configuration port 1 register (address 0x07)

Bit	7	6	5	4	3	2	1	0
Symbol	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

5.5. Output port register pair (0x02, 0x03)

The Output registers define the logic state of an output. The default state is high level at the output.

Table 7. Output port 0 register (address 0x02)

Bit	7	6	5	4	3	2	1	0
Symbol	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1

Table 8. Output port 1 register (address 0x03)

Bit	7	6	5	4	3	2	1	0
Symbol	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

5.6. Polarity inversion register pair (0x04, 0x05)

By means of the Polarity Inversion registers, the logic level of those pins that are defined as inputs via the Configuration registers can be inverted. The inversion does not effect pins programmed as outputs. They appear as programmed in non-inverted polarity.

Table 9. Polarity inversion port 0 register (address 0x04)

Bit	7	6	5	4	3	2	1	0
Symbol	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0

Table 10. Polarity inversion port 1 register (address 0x05)

Bit	7	6	5	4	3	2	1	0
Symbol	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

5.7. Pull Up Resistor register pair (0x08, 0x09)

The Pull Up Resistor registers allow to turn on integrated pull-up resistors in the NCA9595 derivative in the NCA95xx GPIO expander family. In default condition the input pins are not terminated internally, so the device behaves like an xCA9535 from several competitors.

If a GPIO pin is configured as an output, connected pull-up resistors create unnecessary power consumption in logic low state. If a bit in a Pull Up Resistor register is set to 1, the integrated 100 kΩ pull up resistor gets connected to the related port pin.

Table 11. Pull Up Resistors port 0 register (address 0x08)

Bit	7	6	5	4	3	2	1	0
Symbol	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0
Default	0	0	0	0	0	0	0	0

Table 12. Pull Up Resistors port 1 register (address 0x09)

Bit	7	6	5	4	3	2	1	0
Symbol	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
Default	0	0	0	0	0	0	0	0

6. I²C control software for the NCA95xx evaluation PCB

Together with the NCA95xx EVB, a control software is available from Nexperia. The software supports I²C communication with 400 kHz bus speed (FM mode) via an FTDI FT232HQ USB to serial UART interface module. The interface module is connected to a USB port of a Windows computer as shown in Fig. 6. The SCL and SDA I²C bus signals and the GND need to be connected to the evaluation module. A supply voltage of 3.3 V or 5 V is also available from the interface module.

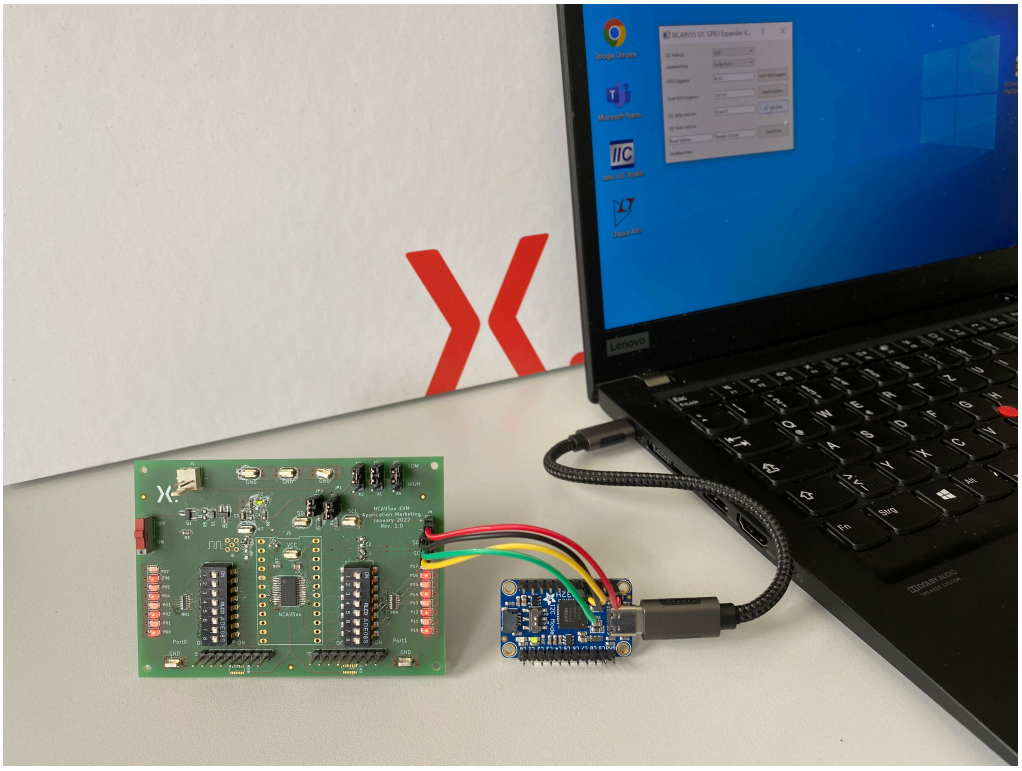

Fig. 6. NCA9555 software communicating with the EVB via a USB to serial interface

The GUI (Graphical User Interface) of the control software is shown in Fig. 7.

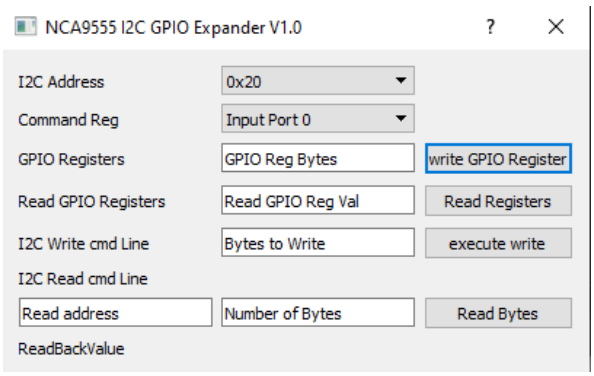

Fig. 7. NCA9555 software user interface

With the I²C address selection pull-down menu the desired device address can be chosen. For the NCA9555 this is one of the options 0x20 to 0x27 compliant to the logic levels at the selection pins A0 to A2 depicted in Table 1.

In the pull-down menu called Command Reg. the pointer register can be selected from the options listed in Table 2.

In the line edit window GPIO Registers data bytes can be defined. The hexadecimal values need to be input with a space as separator. Clicking the button “write GPIO Register” sends a write command to the GPIO expander as defined. If a write command is sent with an empty data field, the pointer is written only.

In Fig. 8 an example for programming of the configuration registers is shown. The NCA95xx handles the I²C bytes in pairs. So, if two bytes are sent the corresponding registers for both ports are updated. The pointer is never incremented to another port function. If more than 2 bytes are written, the pointer toggles between the 2 ports and data in a pair will then be rewritten.

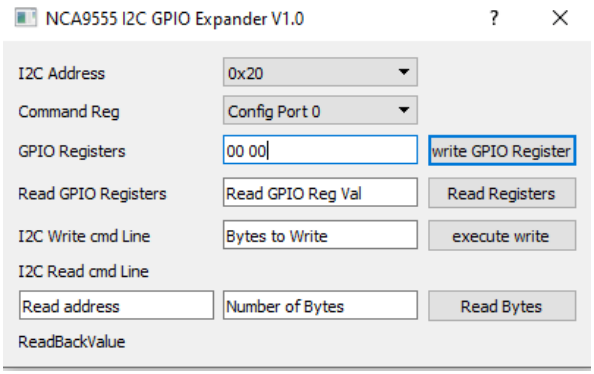

Fig. 8. Example for a write command to configuration register

The line Read GPIO Registers supports reading back a data pair for the chosen pointer register setting in line 2. Clicking the button “Read Registers” delivers 2 bytes, so the actual data value pair for the selected control registers.

In Fig. 9 an example is shown. The Configuration registers have been programmed to 0xAA for Port 0 and 0x55 for Port 1. After pushing the Read Register” button, these values are returned from the read operation.

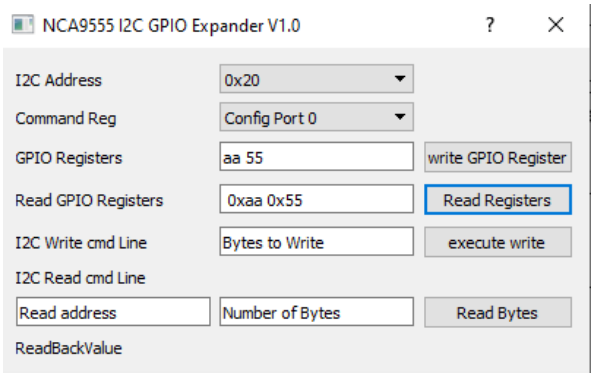

Fig. 9. Example for a write command to configuration registers and a read operation performed afterwards

Fig. 10 shows an example of reading back the Input ports. All port pins are defined as inputs, which is the power-on state. The register pointer has been set to “Input Port 0” in the selection menu. No data is written, because the registers Input Port 0 and Input Port 1 are read-only registers.

Pushing the read button returns the logic state of all port pins. For the example 1 pin, bit 0.3 of Port 0, was terminated to ground and all other port pins are at high level, terminated by the internal pull-up resistors (all 16 LED switches turned off). The read back shows the expected value 0xF7 for Port 0 and 0xFF for Port .

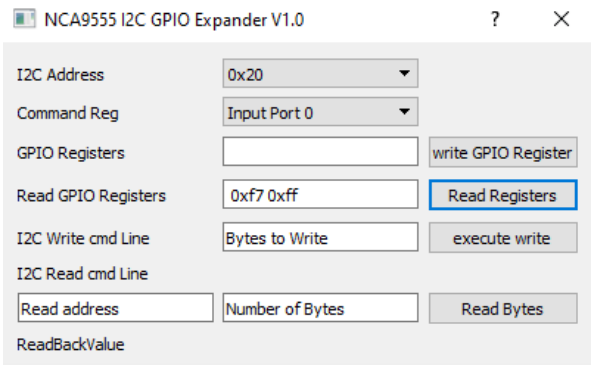

Fig. 10. Example for a read command for the port states. First the pointer was written to "Input Port 0" and read operation performed afterwards

With the I²C Write cmd Line a write command can be executed as depicted in Fig. 11. The NCA9555 has been programmed to use all GPIO pins as outputs. This means that the configuration registers have been cleared. This was done with the upper registers control section.

With the command line 0x02 0x55 0xAA, the pointer is programmed to 0x02 (Output Port 0) and the logic states of outputs of Port 0 are programmed to 0x55. Port 1 is programmed to 0xAA. If all the EVB LED switches are turned on, every second LED per port is emitting light.

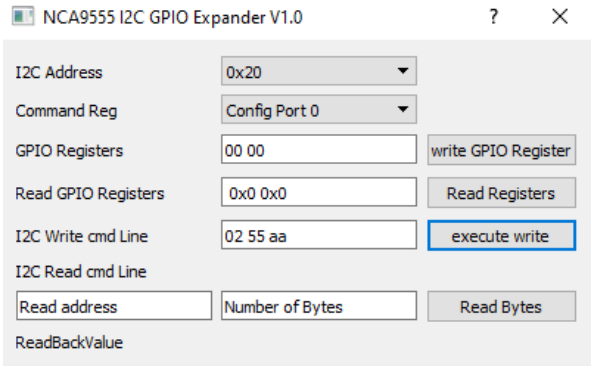

Fig. 11. Example for the usage of the write command line to program the ports output state

In Fig. 12 the above described set-up of the evaluation board is shown. For port 0 all even port pin LEDs are turned on, whereas all odd pins of port 1 are in on-state.

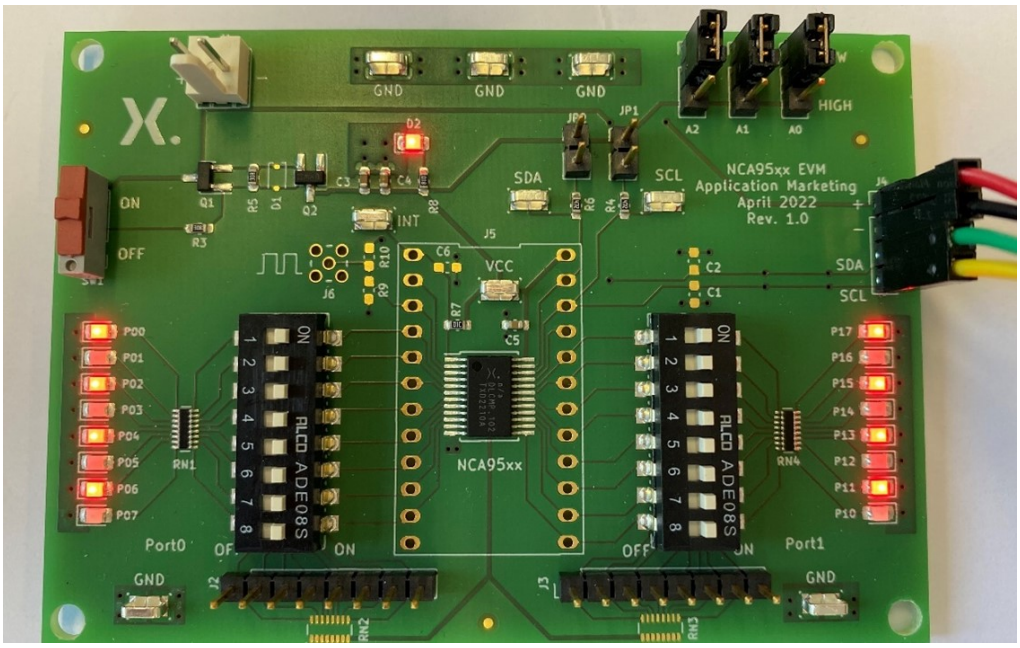

Fig. 12. EVB programmed with the I²C command sequence

In the last line of the user interface a generic “Read command Line” can be found. The pointer address has to be defined in the left input box. In the second box the number of bytes to be written is input. After pushing the “Read Bytes” button, the requested data are shown below the right box.

An example for this read operation is shown in Fig. 13 where the Input ports are read back delivering the 0x55 and 0xAA for the ports. The inputs are all high-state, means 0xFF for the ports. However the inversion register has been programmed to 0xAA for Port 0 and 0x55 for Port 1. So all odd bits get inverted, means cleared in our input condition for Port 0 resulting in 0x55 as read value for Port 0. For Port 1 all even bits get cleared which results in 0xAA as readback.

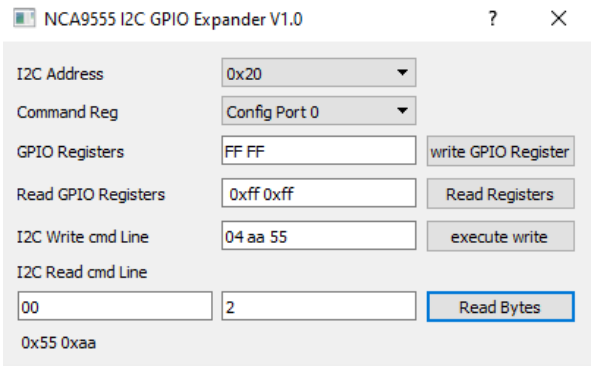

Fig. 13. Usage of the I²C Read command line (bottom line in GUI)

Installing the control software

The control software for the NCA95xx EVB is provided by Nexperia as an executable file: NCA9555_Gui.exe.

Before the software can be used, a driver for the FDTI USB-serial interface needs to be installed. The Zadig USB driver installation application can be used to install the required driver. The Zadig installation file zadig-2.7.exe is made available together with the control software executable file.

Fig. 14 shows the Zadig USB driver installation application. From the drop-down menu in the top line select the **USB Serial Converter** device. Next select the driver **libusbK (v3.0.7.0)**. Finally the "**Replace Driver**" button must be clicked to complete the installation.

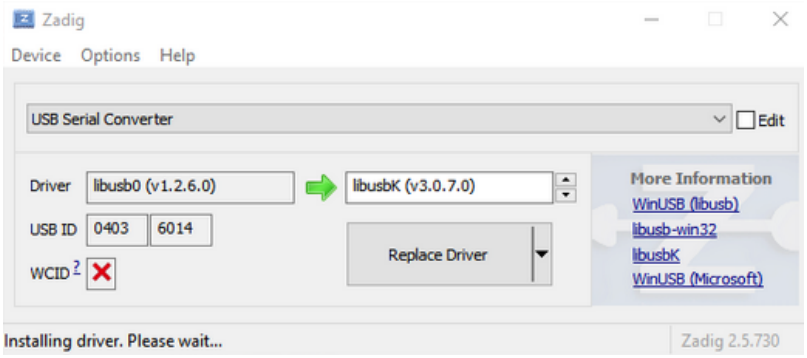

Fig. 14. Zadig USB driver installation application

7. Revision history

Table 13. Revision history

Revision number	Date	Description
1.0	2022-06-22	Initial version.

8. Legal information

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Date of release: 22 June 2022