UM90003

NXTTP4000W066: 4 kW Bridgeless Totem-pole PFC evaluation board

Rev. 1.1 — 1 February 2019 User manual

Document information

Information	Content
Keywords	GaN FET, PFC, evaluation board
Abstract	The NXTTP4000W066 evaluation board is a bridgeless totem-pole Power-Factor-Correction (PFC) circuit. Using Nexperia power GaN FETs a very high-efficiency single-phase AC-DC converter is realized by using a diode-free power GaN FET bridge.

nexperia

1. Introduction

This user guide details the NXTTP4000W066B evaluation board from Nexperia Semiconductors.

The NXTTP4000W066B evaluation board implements a bridgeless totem-pole Power-Factor-Correction (PFC) circuit, using Nexperia power GaN FETs. By using a diode-free power GaN FET bridge with low reverse-recovery charge, very-high-efficiency single-phase AC-DC conversion is realized. In this circuit, the performance and efficiency improvement, achieved by use of the GaN FETs in the fast-switching leg of the circuit, is further enhanced by the use of low resistance MOSFETs in the slow-switching leg. The evaluation board is shown in Fig. 1, Fig. 2 and Fig. 3.

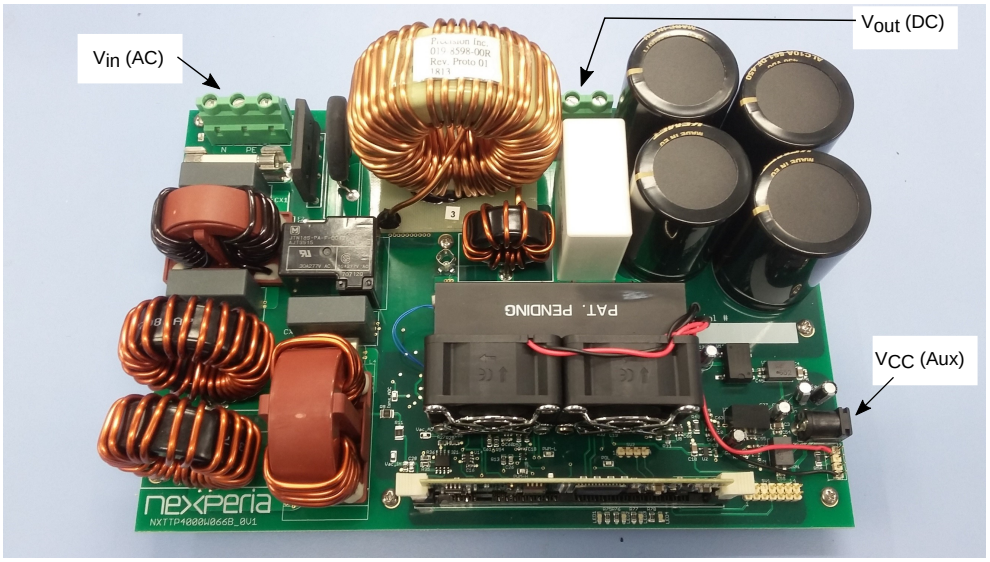


Fig. 1. 4 kW Totem-pole PFC evaluation board; top side

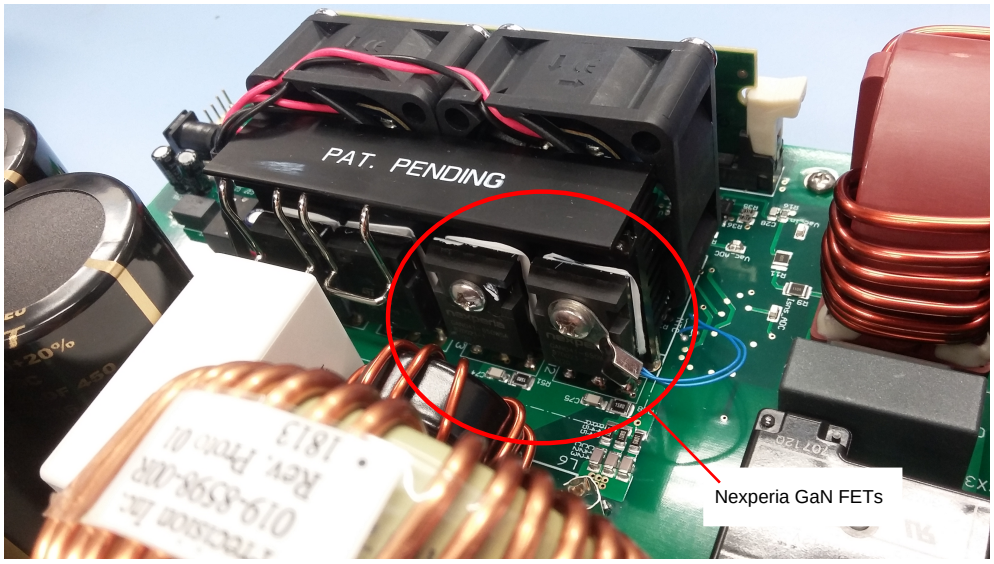


Fig. 2. 4 kW Totem-pole PFC evaluation board

Fig. 3. 4 kW Totem-pole PFC evaluation board; bottom side

1.1. Warnings

This demo board is intended to demonstrate GaN FET technology. While it provides the main features of a totem-pole PFC, it is not intended to be a finished product and does not have all the protection features found in commercial power supplies. Along with this explanation go a few warnings which should be kept in mind:

1. An isolated AC source should be used as input; an isolated lab bench grade power supply or the included AUX DC supply should also be used for the 12 VDC power supply.
2. Use a resistive load only. The totem-pole PFC kit can work at zero load with burst mode. The output voltage will be swinging between 375 V and 385 V during burst mode.
3. The demo board is not fully tested at large load steps. **DO NOT** apply a very large step in the load (>2000 W) when it is running.
4. **DO NOT** manually probe the waveforms when the demo is running. Set up probing before powering up the demo board.
5. The auxiliary VDC supply must be 12 V. The demo board will not work under, for example, 10 VDC or over 15 VDC.
6. **DO NOT** touch any part of the demo board when it is running.
7. When plugging the control cards into the socket, make sure the control cards are fully pushed down with a clicking sound.
8. If the demo circuit goes into protection mode it will work as a diode bridge by shutting down all PWM functions. Recycle the bias power supply to reset the DSP and exit protection mode.
9. **DO NOT** use a passive probe to measure control circuit signals and power circuit signals at the same time. GND1 and AGND are not the same ground.
10. To get clean V_{GS} of low side GaN FET, it is recommended not to measure the V_{DS} at the same time.
11. It is not recommended using passive voltage probe for V_{DS}, V_{GS} measurement and using differential voltage probe for V_{in} measure measurement at the same time unless the differential probe has very good dv/dt immunity.
12. **Be aware** that DC negative and AC neutral are not the same node, and that unless proper caution is taken with instrument grounding, a severe fault condition could be created.

1.2. Quick reference information

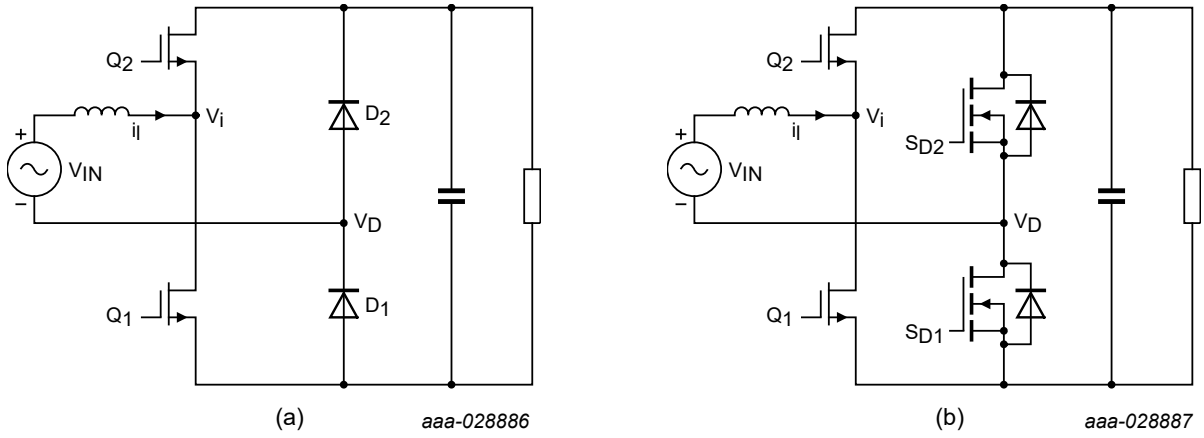
Table 1. NXTTP4000W066_0V2 Input/Output specifications

Parameter	
Input voltage	85 VAC to 265 VAC, 47 Hz to 63 Hz
Input current	18 A (RMS) : (2000 W at 115 VAC, 4000 W at 230 VAC)
10% overload short time	19.8 A (RMS) (2200 W at 115 VAC, 4400 W at 230 VAC)
Ambient temperature	< 50 °C
Output voltage	387 VDC ±5 VDC
PWM frequency	66 kHz
Auxiliary supply	12 VDC for bias voltage

Power dissipation in the GaN FET is limited by the maximum junction temperature. Refer to the GAN041-650WSA datasheet

2. Circuit description

The bridgeless totem-pole topology is shown in Fig. 4 below. As shown in Fig 4 (a), two GaN FETs and two diodes are used for the line rectification, while in Fig 4 (b), the circuit is modified and the diodes are replaced by two low resistance silicon MOSFETs to eliminate diode drops and improve the efficiency. Further information and discussion on the performance and the characteristics of bridgeless PFC circuit is provided in [1].



(a) Diode for line rectification

(b) MOSFET for line rectification

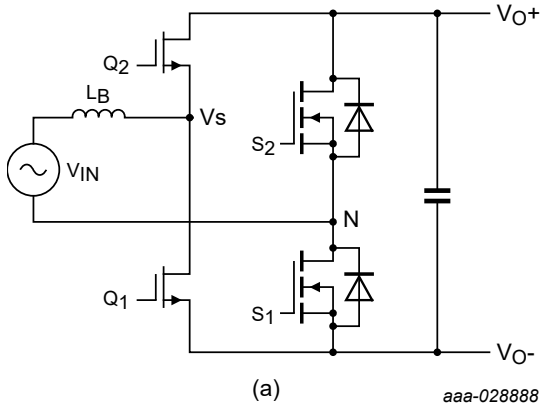
Fig. 4. Totem-pole bridgeless PFC converter based on GaN FET

The large recovery charge (Q_{rr}) of existing silicon MOSFETs makes CCM operation of a silicon totem-pole Bridgeless PFC impractical and reduces the total efficiency. Table 2 below compares a Nexperia GaN FET to an equivalent CoolMOS FET.

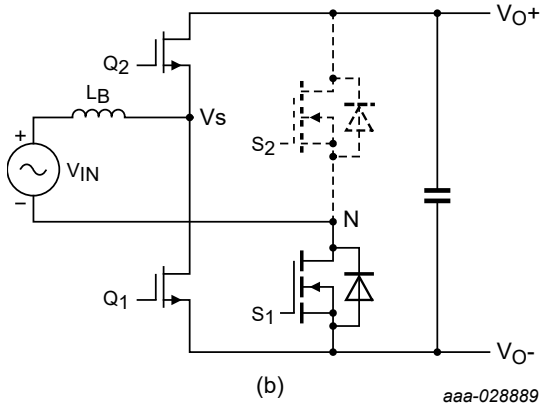
Table 2. Key parameter comparison of GAN041-650WSA to IPW65R041CFD

Parameter	GAN041-650WSA	IPW65R041CFD
$R_{DS(on)}$ max	41 mΩ	41 mΩ
I_D	50 A	68.5 A
Q_G	21 nC	300 nC
Q_r	180 nC	1.9 µC

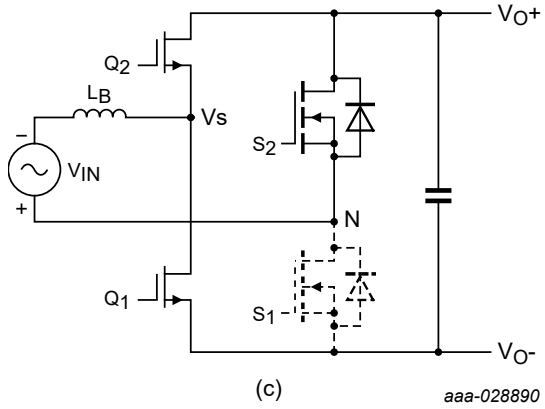
A GaN FET totem-pole PFC in Continuous Conduction Mode (CCM) focusing on minimizing conduction losses was designed. A simplified schematic is shown in Fig 5 (a). It consists of a pair of fast GaN FET switches (Q1 and Q2) operating at a high Pulse-Width-Modulation (PWM) frequency and a pair of slow, but very-low-resistance, MOSFETs (S1 and S2) operating at a much slower line frequency (50/60 Hz). The primary current path includes one fast switch and one slow switch only, with no diode drop. The function of S1 and S2 is that of a synchronized rectifier as illustrated in Fig 5 (b) and Fig 5 (c). During positive AC cycle, S1 is on and S2 is off, forcing the AC neutral line tied to the negative terminal of the DC output. The opposite applies for the negative cycle.



(a) Simplified schematic



(b) Positive AC half-cycle

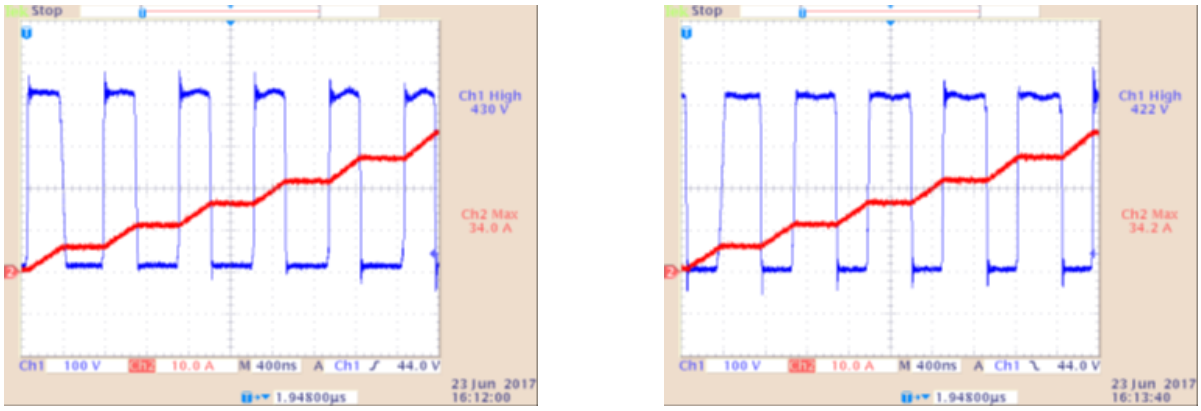


(c) Negative AC half-cycle

Fig. 5. GaN FET totem-pole bridgeless PFC converter

In either AC polarity, the two GaN FETs form a synchronized boost converter with one transistor acting as a master switch to allow energy intake by the boost inductor (L_B) and another transistor as a slave switch to release energy to the DC output. The roles of the two GaN FET devices interchange when the polarity of the AC input changes; therefore, each transistor must be able to perform both master and slave functions. To avoid shoot through, a dead time is built in between two switching events during which both transistors are momentarily off. To allow CCM operation, the body diode of the slave transistor has to function as a flyback diode for the inductor current to flow during dead time. The diode current, however, has to quickly reduce to zero and transition to the reverse blocking state once the master switch turns on. This is the critical process for a totem pole PFC which previously lead to abnormal spikes, instability and associated high switching losses due to the high Q_{rr} of the body diode in modern high-voltage Si MOSFETs. The low Q_{rr} of the GaN FET switches allows designers to overcome this barrier. As seen in Fig. 6 inductive tests at 430-V bus using either low-side or high-side GaN FET as a master switch show healthy voltage waveforms up to inductor current exceeding 35 A.

With a design goal of 4.4 kW output power in CCM mode at 230 VAC input, the required inductor current is 20 A. This test confirms a successful totem-pole power block with enough current overhead.



(a) High side as master

(b) Low side as master

Fig. 6. Hard-switched waveforms of a pair of GaN FET switches

One inherent issue in bridgeless totem-pole PFC is the operation mode transition at AC voltage zero-crossing. For instance, when the circuit operation mode changes from positive half-cycle to negative half-cycle at the zero-crossing, the duty ratio of switch Q1 changes abruptly from almost 100% to 0%, and the duty ratio of switch Q2 changes from 0% to 100%. Due to the slow reverse recovery of diodes (or body diode of MOSFET), the voltage V_D cannot jump from ground to VDC instantly; a current spike will be induced. To avoid the problem, a soft-start at every zero-crossing is implemented to gently reverse the duty ratio.

Since the NXTTP4000W066B totem-pole bridgeless PFC is designed to run in CCM, the larger inductance actually alleviates the current spike issue at zero-crossing. A soft-start time of a few switching cycles is enough to handle this problem.

3. Design details

For this evaluation board, the PFC circuit has been implemented on a 4-layer PCB. The GaN FET half-bridge is built with GAN041-650WSA devices by Nexperia. The slow Si switches are STY139N65M5 super junction MOSFETs with 0.017 Ω on-resistance. The inductor is made of a High Flux core with the inductance of 480 µH and a DU resistance of 0.025 Ω, designed to operate at 66 kHz. A simple 0.5 A rated high/low side driver IC (Si8230) with 0/12 V as on/off states directly drives each GaN FET. A 150 MHz DSP – the TMS320F28335 – handles the control algorithm.

The voltage and current loop controls are similar to conventional boost PFC converter. The feedback signals are DC output voltage (V_O), AC input potentials (VACP and VACN) and inductor current (I_L). The input voltage polarity and RMS value are determined from VACP and VACN. The outer voltage loop output multiplied by |VAC| gives a sinusoidal current reference. The current loop gives the proper duty ratio for the boost circuit. The polarity determines how PWM signal is distributed to drive Q1 and Q2. A soft-start sequence with a duty ratio ramp is employed for a short period at each AC zero-crossing for better stability.

The circuit schematic, PCB layout and bill of materials for the NXTTP4000W066 bridgeless totem-pole PFC evaluation board are shown in the next sections.

3.1. NXTTP4000W066_0V2 schematics

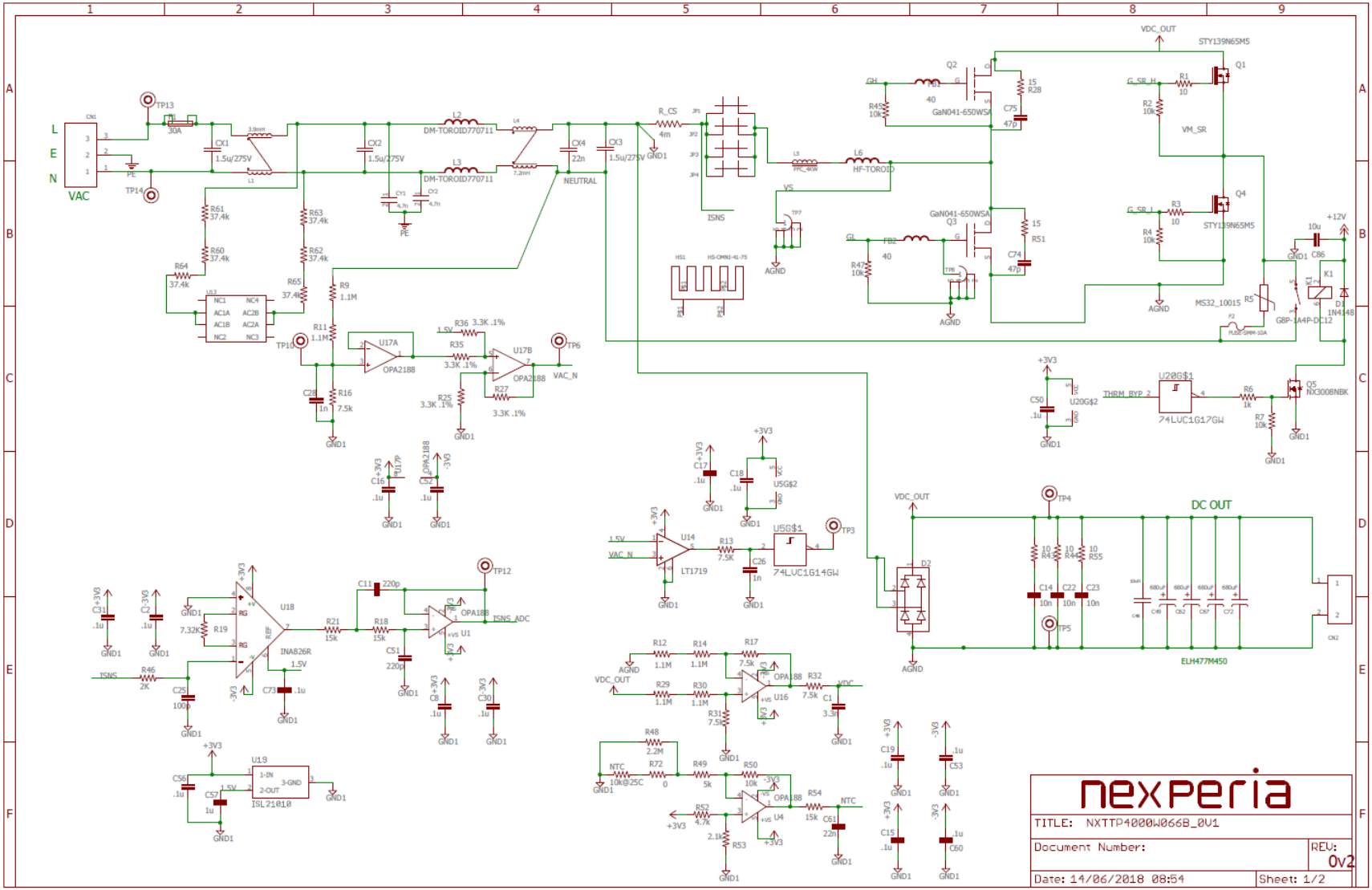


Fig. 7. Schematic sheet 1

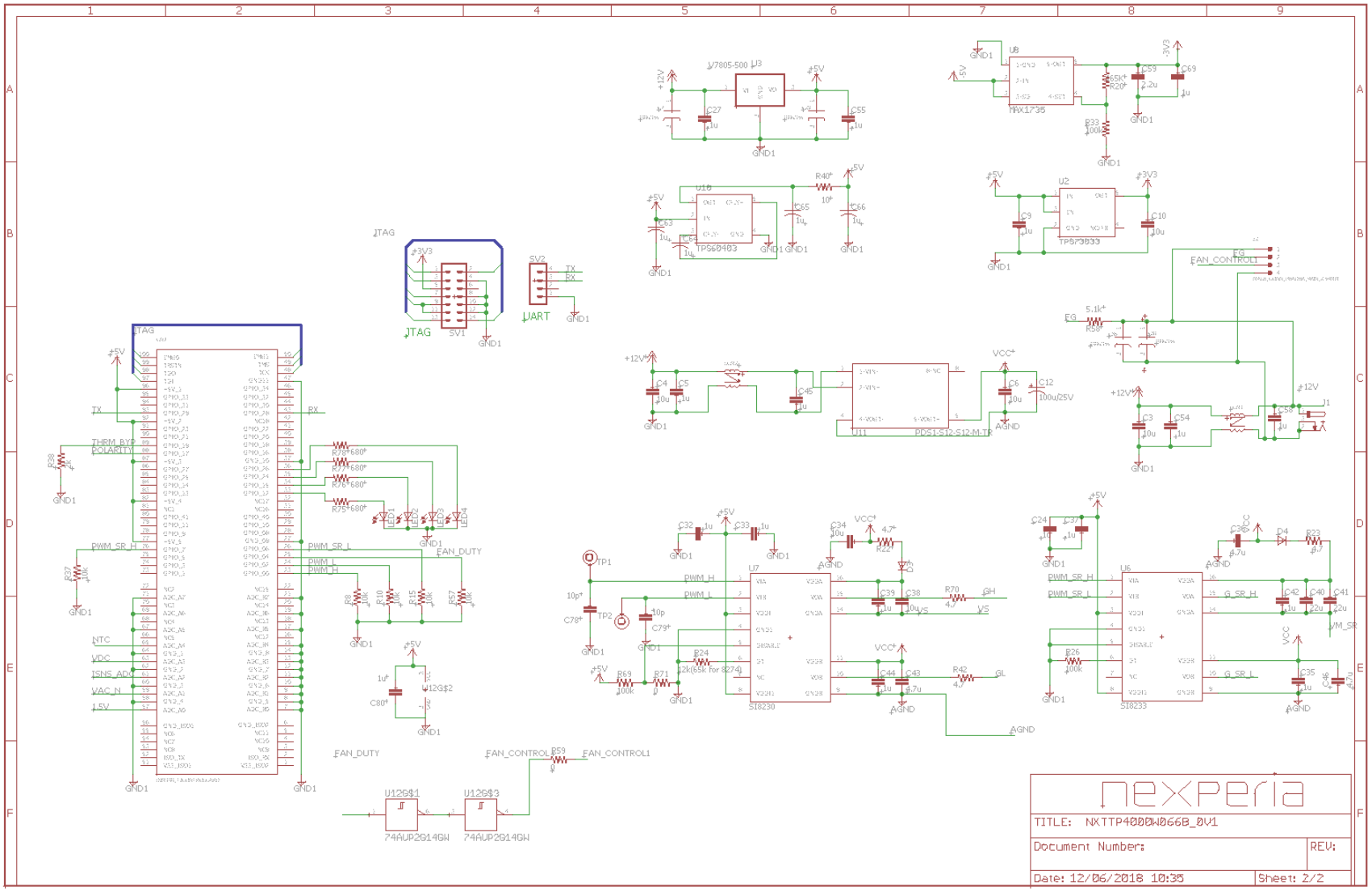


Fig. 8. Schematic sheet 2

3.2. NXTTP4000W066_0V2 PCB Layout

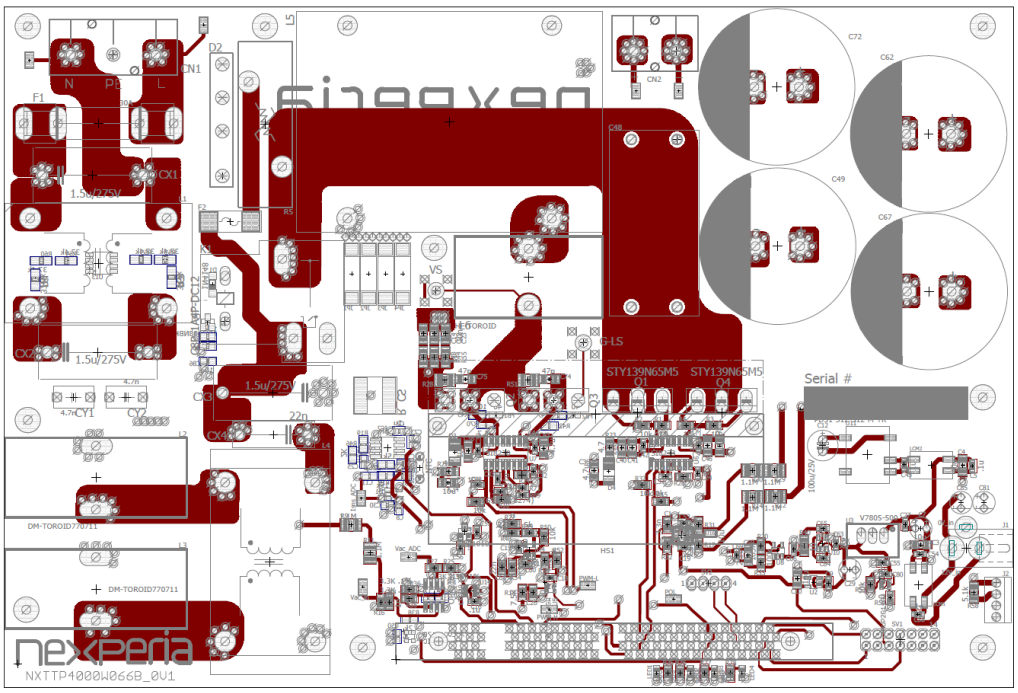


Fig. 9. PCB top layer

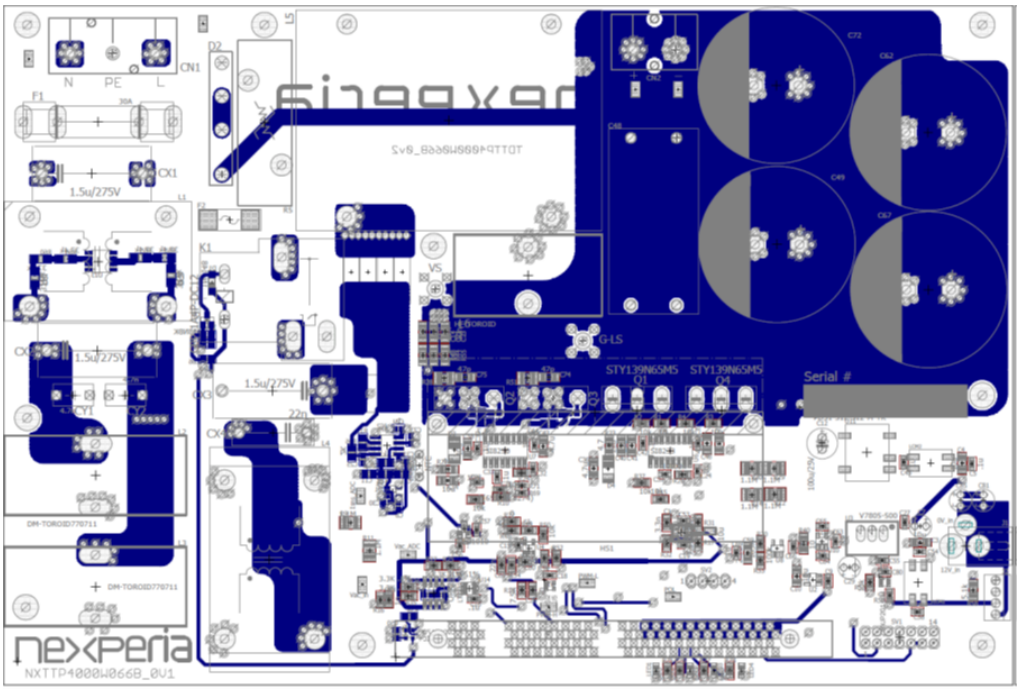


Fig. 10. PCB bottom layer

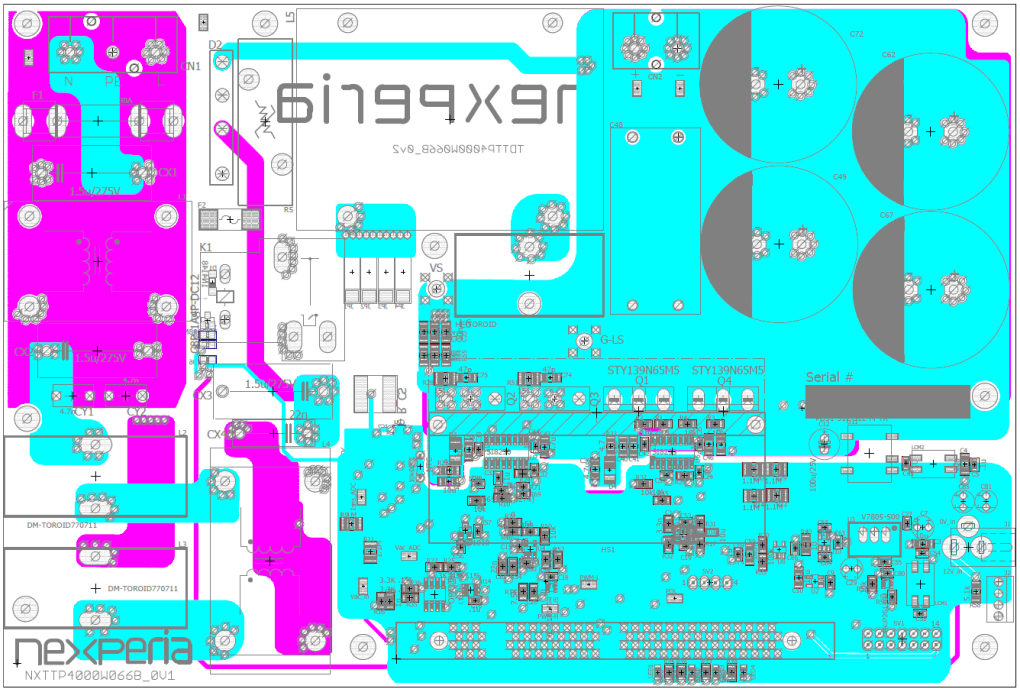


Fig. 11. PCB inner layer 2 (ground plane) and inner layer 3 (power plane)

3.3. NXTTP4000W066_0V2 Bill of Materials

Table 3. NXTTP4000W066B_0V2 evaluation board Bill of Materials (BOM)

Qty	Value	Reference designator	Manufacturer's part number	Manufacturer
2	-	D3, D4	ES1J	Micro Commercial
1	-	D2	GBJ2506-BP	Micro Commercial
4	-	LED1, LED2, LED3, LED4	SML-211UTT86	Rohm
1	-	SV2	961104-6404-AR	3M
1	-	SV1	67996-114HLF	FCI
1	-	J1	PJ-002AH	CUI
2	-	TP7, TP8	131-4353-00	Tektronix
10	-	TP1, TP2, TP3, TP4, TP5, TP6, TP10, TP12, TP13, TP14	5015	Keystone
28	0.1 µF	C2, C5, C8, C9, C15, C16, C17, C18, C19, C24, C27, C30, C31, C32, C33, C35, C37, C39, C42, C44, C50, C52, C53, C54, C55, C56, C60, C73	06033C104JAT4A	AVX
2	0 Ω	R59, R71	RC0603JR-070RL	Yageo
1	0 Ω	R72	RC0805JR-070RL	Yageo
6	1.1 MΩ	R9, R11, R12, R14, R29, R30	KTR25JZPF1104	Rohm
3	1.5 µF/275 V	CX1, CX2, CX3	155MKP275KG	Illinois Capacitor
2	10 Ω	R1, R3	RMCF0805JT10R0	Stackpole
1	10 Ω	R40	RMCF1206FT10R0	Stackpole
1	100 kΩ	R69	ESR03EZPF1003	Rohm
2	100 kΩ	R26, R33	RMCF0805FT100K	Stackpole
1	100 pF	C25	06035A101FAT2A	AVX
4	100 µF/16 V	C7, C29, C81, C85	UKL1E101KPDANA	Nichicon
1	100 µF/25 V	C12	ESK107M025AC3AA	Kemet
11	10 kΩ	R2, R4, R7, R8, R10, R15, R37, R45, R47, R50, R57	KTR10EZPF1002	Rohm
1	10 kΩ @ 25 °C	NTC	B57703M103G40	EPCOS (TDK)
3	10 nF	C14, C22, C23	C3216C0G2J103J160AA	TDK
2	10 pF	C78, C79	C0603C100K3GACTU	Kemet
1	10 µF	C86	GRM219R61E106KA12D	MuRata
6	10 µF	C3, C4, C6, C10, C34, C38	CL31A106KAHNNNE	Samsung Electro
1	10 **µH**	C48	C4ATGBW5100A3FJ	Kemet
1	12 kΩ	R24	RC0805FR-0712KL	Yageo

Qty	Value	Reference designator	Manufacturer's part number	Manufacturer
3	10 Ω	R43, R44, R55	RNCP1206FTD10R0	Stackpole
2	15 Ω	R28, R51	RMCF1210FT15R0	Stackpole
3	15 kΩ	R18, R21, R54	05FR-0715KL	Yageo
1	165 kΩ	R20	ERJ-6ENF1653V	Panasonic
1	1N4148	D1	1N4148W-E3-18	Vishay
1	1 kΩ	R6	ERJ-6ENF1001V	Panasonic
2	1 nF	C26, C28	CC0805KRX7R9BB102	Yageo
9	1 µF	C45, C57, C58, C69, C80, C63, C64, C65, C66	TMK107B7105KA-T	Taiyo Yuden
1	2.1 kΩ	R53	RC0805FR-072K1L	Yageo
1	2.2 MΩ	R48	RMCF0805JT2M20	Stackpole
1	2.2 µF	C59	CL31B225KAHNNNE	Samsung Electro
2	220 pF	C11, C51	C0805KRX7R9BB221	Yageo
1	22 nF	C61	C2012C0G1V223J060AC	TDK
1	22 nF	CX4	PME271M522MR30	Kemet
2	22 µF	C40, C41	CL31X226KAHN3NE	Samsung Electro
1	2 kΩ	R38, R46	RMCF0805FT2K00	Stackpole
1	2PIN_9.53MM	CN2	1714971	Phoenix Contact
4	3.3 kΩ 0.1%	R25, R27, R35, R36	ERA-6AEB332V	Panasonic
1	3.3 nF	C1	C0805C332K5RACTU	Kemet
1	3.9 mH	L1	T60405-R6128-X225	Vacuumschmelze
2	30 A	F1	01020078H	Little Fuse
6	37.4 kΩ	R60, R61, R62, R63, R64, R65	RC1206FR-0737K4L	Yageo
1	3PIN_9.53MM	CN1	1714984	Phoenix Contact
2	4.7 Ω	R42, R70	ESR10EZPJ4R7	Rohm
2	4.7 Ω	R22, R23	CRM1206-JW-4R7ELF	Bourns
1	4.7 kΩ	R52	RC0805FR-074K7L	Yageo
2	4.7 nF	CY1, CY2	R413F147000M1M	Kemet
3	4.7 µF	C36, C43, C46	CL31B475KBHNNNE	Samsung Electro
2	40 Ω	FB1, FB2	MMZ1608S400ATD25	TDK
2	47 pF	C74, C75	CC1206JKNPOZBN470	Yageo
1	4 m	R_CS	CSSH2728FT4L00	Stackpole
1	5.1 kΩ	R58	RC1206FR-075K1L	Yageo
1	5 kΩ	R49	RC0805FR-075K1L	Yageo
4	680 Ω	R75, R76, R77, R78	RC0805FR-07680RL	Yageo
4	680 µF	C49, C62, C67, C72	ALC10A561DF450	Kemet
1	7.2 mH	L4	T60405-R6128-X230	Vacuumschmelze
1	7.32 kΩ	R19	RC0805FR-077K32L	Yageo
1	7.5 kΩ	R13	ERJ-6ENF7501V	Panasonic

Qty	Value	Reference designator	Manufacturer's part number	Manufacturer
4	7.5 kΩ	R16, R17, R31, R32	RN73C2A7K5BTDF	Panasonic
2	CMC_WURTH_ 744229	LCM1, LCM2	744229	Würth
1	DIM100_TI CONTROL CARD	CN3	5390213-1	Texas TE Connectivity
1	FUSE- SMM-10A	F2	SMM 10	Bel Fuse
1	G8P-1A4P-DC12	K1	JTN1AS-PA-F-DC12V	Panasonic Industrial Dev
1	INA826R	U18	INA826AID	Texas Instruments
1	ISL21010	U19	ISL21010CFH315Z-TK	Intersil
4	JUMPER_ S1621-46R	JP1, JP2, JP3, JP4	S1621-46R	Harwin Inc
1	LT1719	U14	LT1719CS6#TRMPBF	Linear Technology
1	MALE_CONN_HEADER_ 4PIN_2.54MM	J2	961104-6404-AR	3M
1	MAX1735	U8	MAX1735EUK50+T	Maxim Integrated
1	MS32_10015	R5	MS32 10015-B	Ametherm
1	NCP4810	U13	CAP200DG	Power Integrations
3	OPA188	U1, U4, U16	OPA188AIDBVT	Texas Instruments
1	OPA2188	U17	OPA2188AIDR	Texas Instruments
1	PDS1-S12-S12-M-TR	U11	PDS1-S12-S12-M-TR	CUI
1	SI8230/8274	U7	SI8230BB-D-IS1	Silicon Labs
1	SI8233	U6	SI8233BB-D-IS1	Silicon Labs
1	TPS60403	U10	TPS60403DBVR	Texas Instruments
1	TPS73033	U2	TPS73033DBVR	Texas Instruments
1	V7805-500	U3	V7805-500	CUI
9	stand off (nylon 1/2)	9	1902C	
1	HS-OMNI-41-75	HS1	OMNI-UNI-41-75	Wakefield-Vette
1	74AUP2G14GW	U12	74AUP2G14GW	Nexperia
1	74LVC1G14GW	U5	74LVC1G14GW	Nexperia
1	74LVC1G17GW	U20	74LVC1G17GW	Nexperia
1	NX3008NBK	Q5	NX3008NBK	Nexperia
2	DM-TOROID770711	L2, L3	CWS-1SN-12606	Coil Winding Specialists
1	10uH HF-TOROID	L6	CWS-1SN-12554	Coil Winding Specialists
1	442uH min	L5	019-8598-00R	Precision Inc
2	STY139N65M5	Q1, Q4	STY139N65M5	ST Microelectronics
2	GAN041-650WSA	Q2, Q3	GAN041-650WSA	Nexperia
1	control card	control card	TMS320F28335	Texas Instruments
2	FAN	MB40201VX-000U-A99	MB40201VX-000U-A99	Sunon
2	FAN GAURDS	G40-2	G40-2	Orion Fans
1	THERMAL TAPE	BP100-0.011 -00-1010	BP100-0.011 -00-1010	Bergquist
2	Thermal HEAT PAD	4180G	4180G	Aavid

Qty	Value	Reference designator	Manufacturer's part number	Manufacturer
2	Thermal pad for Q2, Q3		4169G	Aavid
	DEVICE SCREWS - 6-32 x 7/16 PAN		wcb1630501	(globalindustrial.com)
	Fan mount screws - 1" #4 SELF TAPPING SCREWS		wcb1628443	(globalindustrial.com)
9	machine screw (ss 1/2)	machine screw (ss 1/2)	9902	-
2	screws for FETs to HS (Q2, Q3)	screws for FETs to HS (Q2, Q3)	6/32	-

4. Using the board

The board can be used for evaluation of Nexperia GAN041-650WSA GaN FETs in a bridgeless totem-pole PFC circuit. It is not a complete circuit, but rather a building block.

4.1. Turn on Sequence:

1. Connect an Electronic / resistive load to the corresponding marking (CN2).
   The requirement for the resistive load:
   - At 115 VAC input: 0 W and ≤ 2200 W
   - At 230 VAC input: 0 W and ≤ 4400 W
2. Connect the 12 VDC auxiliary supply to the demo-board (included in the demo-kit package).
   - Verify auxiliary LED is on.
   - Verify both FANS attached to heatsink are running
3. With the HV power turned off, connect the high-voltage AC power input to the corresponding marking (CN1) on the PCB.
   - N and L (PE: potential ground)
4. Turn on the AC power input (85 VAC to 265 VAC; 50 – 60 Hz)
   - Minimum power load for turn-on sequence is 350 W.
     Note the minimum load at start-up is required by the control algorithm implemented. It is not an inherent requirement of the bridgeless totem-pole topology. Full-load and no-load start-up are possible with more optimized control.
   - Monitor CN2 output voltage with VDC meter to verify 385 V ±5 V is generated.
   - The electronic/resistive load can be increased while the AC supply is ON and the board is functional.

4.2. Turn off Sequence:

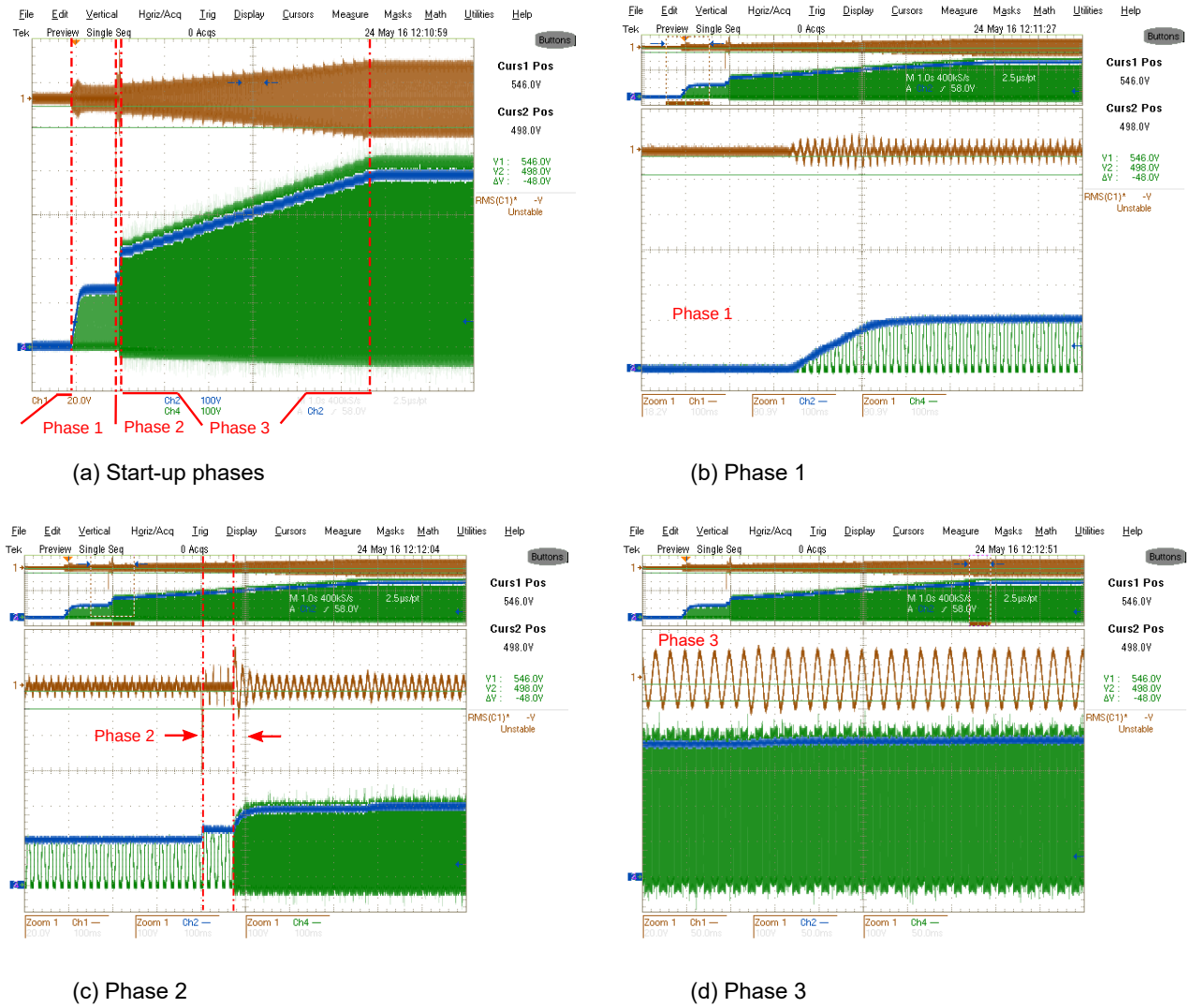
1. Switch off the high-voltage AC power input; .
2. Power off the DC bias.

5. Operational waveforms

Fig. 12 below shows the converter start-up procedure: CH1 shows the DC input current; CH2 is the DC bus voltage waveform and CH3 is the voltage waveform of fast leg switching node. For the start-up, there are three phases to charge the DC bus to a reference voltage.

Initially the relay K1 is open and DC bus capacitors are charged by input voltage through NTC R5 and the diode bridge. When the VDC is over 100 V, the relay K1 is closed to bypass the NTC, and the VDC increase to the peak of the input voltage.

After 100 ms, the GaN FETs **leg** is engaged in closed-loop voltage control, in which the DC bus voltage reference slowly increases to the rated voltage of 385 V. The NTC and diode bridge are applied in this circuit to avoid high inrush current flow through the GaN FETs.



(a) Start-up phases

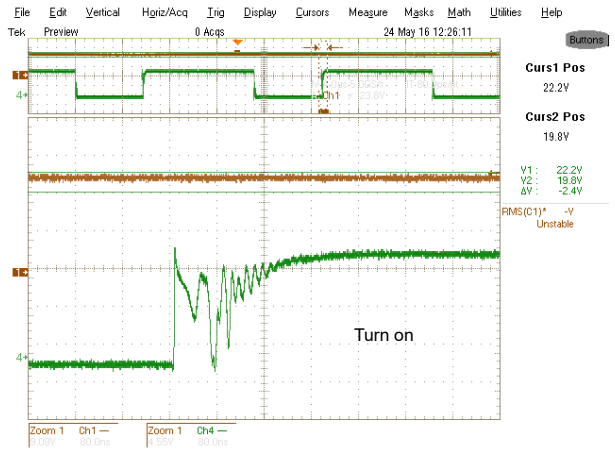
(b) Phase 1

(c) Phase 2

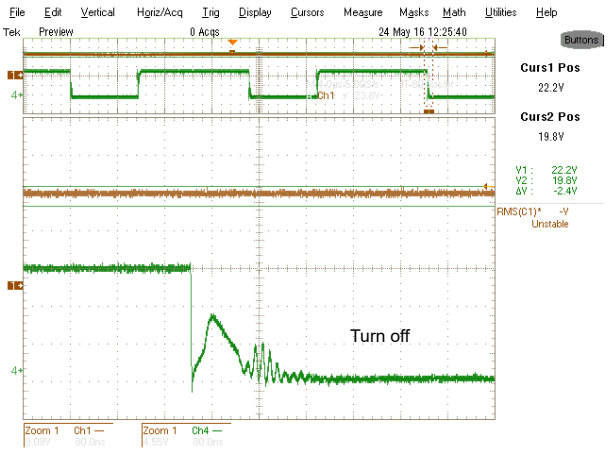
(d) Phase 3

Fig. 12. Start-up of the bridgeless totem-pole PFC (CH1: I_{in}, Ch2: V_O, CH3: V_{DS}) with 1.2 kW load

Fig. 13 below shows the turn on and turn off V_{GS} waveforms at I_L = 23 A. There is no voltage overshoot at turn-on. Turn-off voltage bump is caused by the total effective gate impedance.



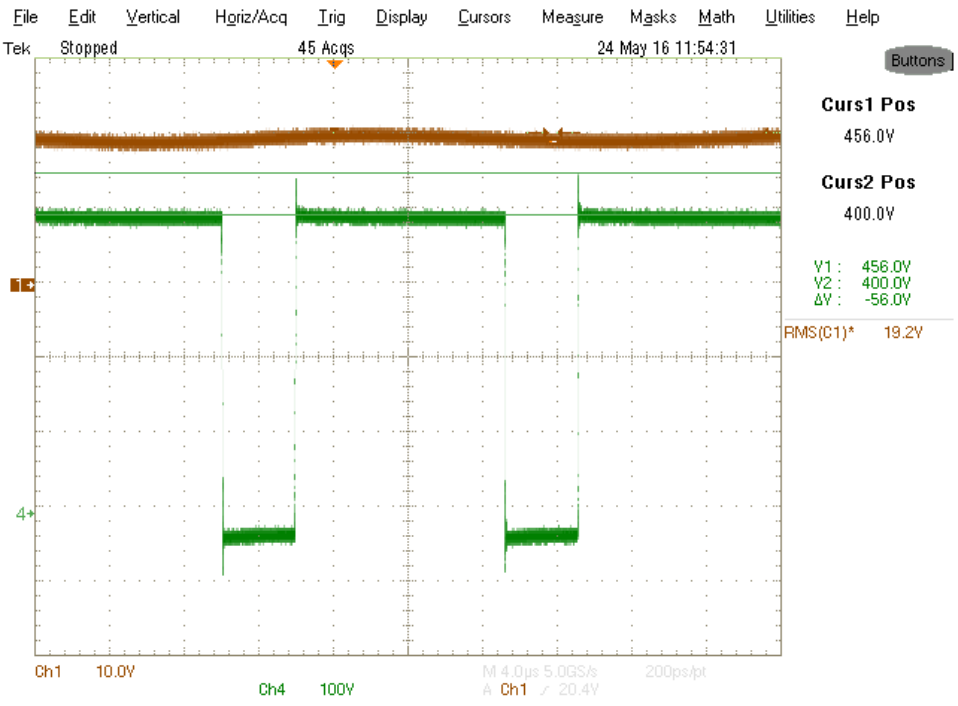
(a) Turn on, CH1: input current I_{IN} (10 A/div); CH4: V_{GS} of Q2 (5 V/div)



(b) Turn off, CH1: input current I_{IN} (10 A/div); CH4: V_{GS} of Q2 (5 V/div)

Fig. 13. Waveforms of I_{IN} and Q2 V_{GS} at I_L = 23 A

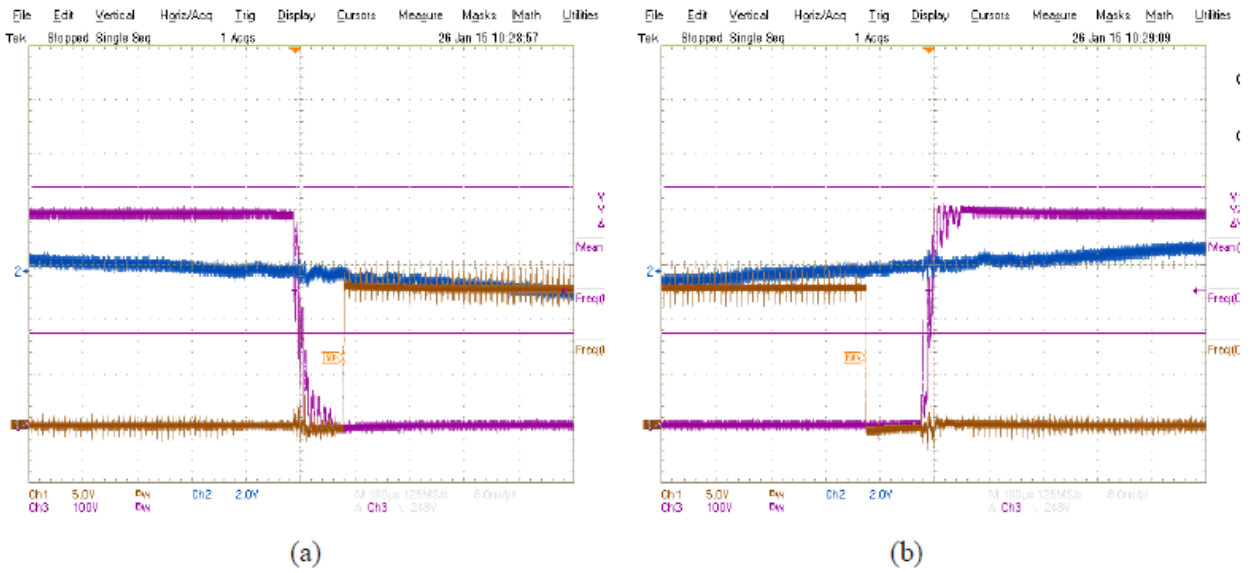
Fig. 14 below shows the V_{DS} of Q2 at 3.5 kV. It can be seen that the voltage spike is 56 V at I_L = 20 A. In this circuit, the RC snubber and R_G help to reduce voltage spikes.



CH1: input current I_{in} (10 A/div); CH4: V_{DS} (100 V/div)

Fig. 14. Waveforms of I_{IN} and V_{DS} of Q2 at I_L = 20 A

Fig. 15 below shows the transition between two half cycles. In (a) the AC line enters the negative half-cycle. Soft-start gradually increases voltage V_D from 0 V to 385 V. While in (b), V_D decreases from 385 V to 0 V.



(a) from negative to positive half-cycle (b) from positive to negative half-cycle: CH1: PW <Gate Signal for SD2; CH2: I_L waveform; CH3: V_D waveform

Fig. 15. Zero-crossing transitional waveform

6. Dead time control

The required form of the gate-drive signals is shown in Fig. 16. The times marked A are the dead times when neither transistor is driven on. The dead time must be greater than zero to avoid shoot-through currents. The Si8230 gate drive chip ensures a minimum dead time based on the value of resistor R24, connected to the DT input. The dead time in ns is equal to the resistance in kΩ x 10, so the default value of 12 kΩ corresponds to 120 ns. This will add to any dead time already present in the input signals

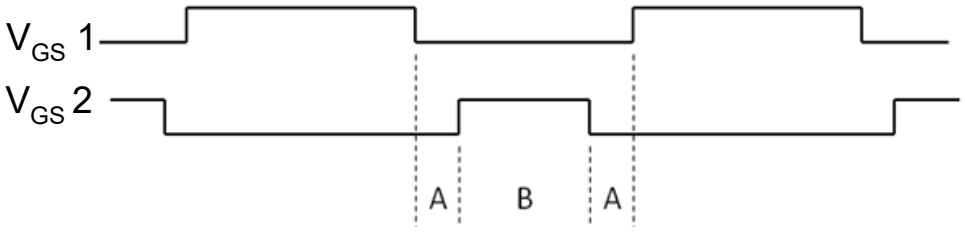


Fig. 16. Non-overlapping gate pulses

Nexperia GaN FETs can switch at dV/dt of 50 V/ns or higher to enable the lowest possible switching loss. At this level of operation, even the layout becomes a significant contributor to performance. As shown in Fig 7, the recommended layout keeps a minimum gate drive loop; it also keeps the traces between the switching nodes very short, with the shortest practical return trace to the power bus and ground. As the power ground plane provides a large cross-sectional area to achieve an even ground potential throughout the circuit. The layout carefully separates the power ground and the IC (small signal) ground.

Note that the Nexperia GaN FETs in TO247 package has pin-out configured as G-S-D, instead of traditional MOSFET's G-D-S arrangement. The configuration is designed with thorough consideration to minimize the Gate-Source driving loop to reduce parasitic inductance as well as to separate the driving loop (Gate-Source) and power loop (Drain-Source) to minimize noise. For further information, different layers of NXTTP4000W066B design are shown in Section 3.2.

7. Probing

As shown in Fig. 17 below, in the demo board, there are four probing sockets to allow measurement of V_{GS} and V_{DS} of the low-side GaN FET and MOSFET. By removing the jumpers and using a short wire to clamp the current probe, the PFC inductor can also be measured.

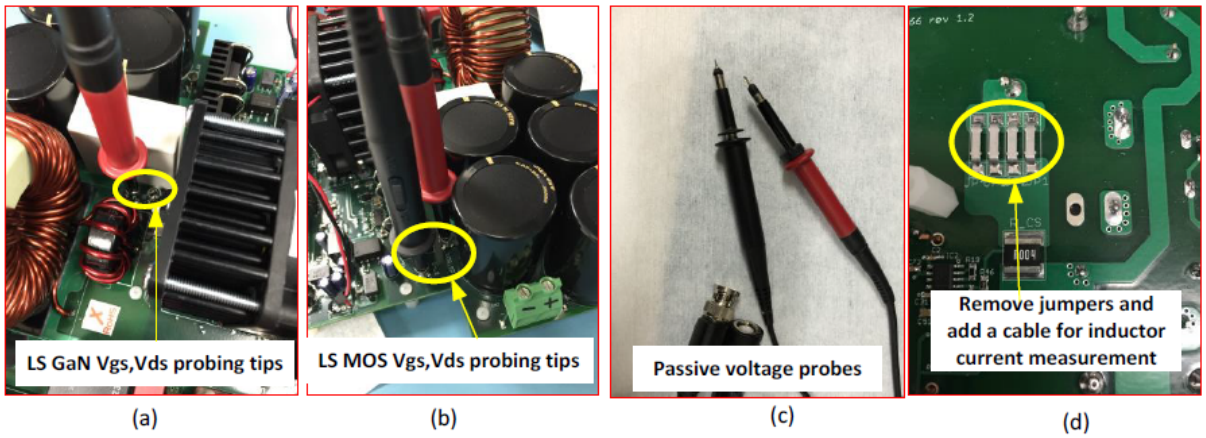


Fig. 17. V_{GS} and V_{DS} of low side GaN FET and MOSFET measurement socket tips, and PFC inductor current measuring position

8. Efficiency sweep and EMI

For the efficiency calculation, the input/output voltage and current are measured using a power analyzer to obtain the input/output power values. Efficiency has been measured at 120 VAC or 230 VAC input and 400 VDC output using the WT1800 precision power analyzer from Yokogawa. The efficiency results for this totem-Pole PFC board are shown in Fig. 18.

The extremely high efficiency of 99% at 230 VAC input, and > 98% at 115 VAC input is the highest among PFC designs with similar PWM frequency; this high efficiency will enable customers to reach peak system efficiency to meet and exceed Titanium standards.

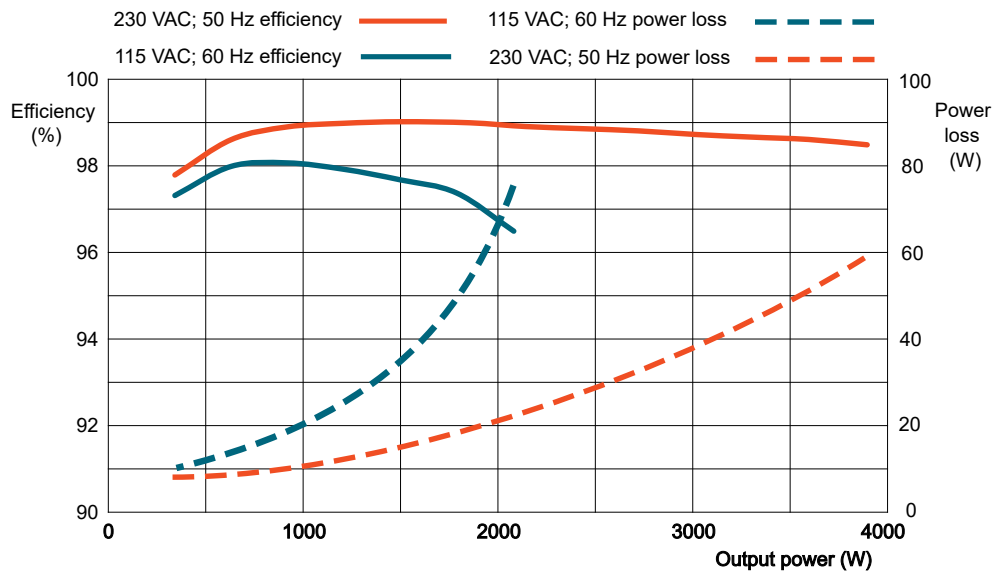


Fig. 18. Efficiency as a function of output power for bridgeless totem-pole PFC Evaluation Board

EMI

Conducted emissions have also been measured for this board using an LIN-115A LISN by Com-Power. The results compared to EN55022A limits are shown in Fig. 19. It should be noted that the EMI test was done by using the lab-use power supply for auxiliary 12 V source. **Do not use wall AC-DC adaptor for EMI test.**

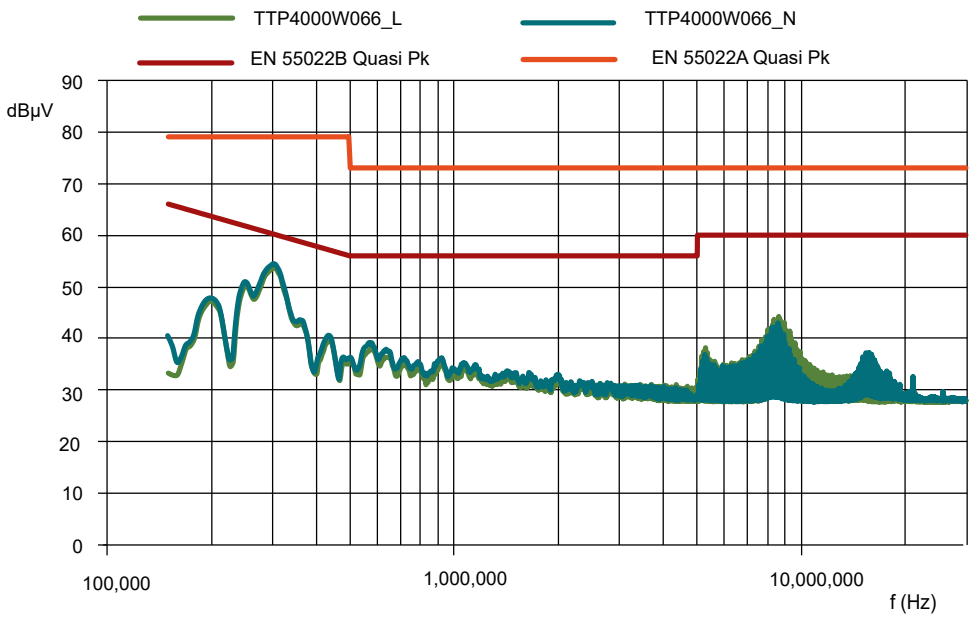


Fig. 19. Conducted emissions @ 115 V, 1150 W

The THDi is measured using WT1800 at the condition of input THDv 3.8%. As shown in Fig. 20 below, it meets the standard of IEC61000-3-12.

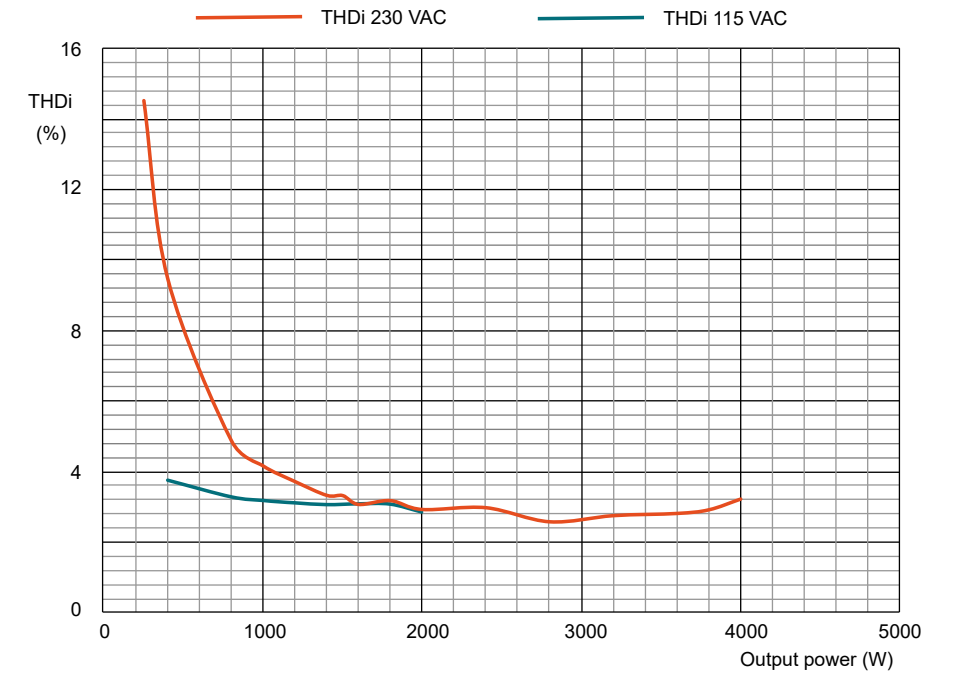


Fig. 20. THDi meets IEC61000-3-12 (>16 A)

9. Maximum load limit

The NXTTP4000W066 Bridgeless totem-pole PFC eval board is allowed to run overload in a short time. The rated input current for < 230 VAC input is 18 A, and the 10% overload current can be 19.8 A. The input OCP will be triggered when the current is over 21 A.

10. References

1. Liang Zhou, Yi-Feng Wu and Umesh Mishra, “True Bridgeless Totem-pole PFC based on GaN FETs”, PCIM Europe 2013, 14-16 May, 2013, pp.1017-1022.
2. L. Huber, Y. Jang, and M. M. Jovanovic, “Performance evaluation of Bridgeless PFC boost rectifiers,” IEEE Transactions on Power Electronics, Vol. 23, No. 3, pp. 1381-1390, May 2008.

11. Revision history

Table 4. Revision history

Revision number	Date	Description
1.1	2019-02-01	Type number GAN041-650WSA corrected
1.0	2018-10-16	Initial version of the document

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