TN90007

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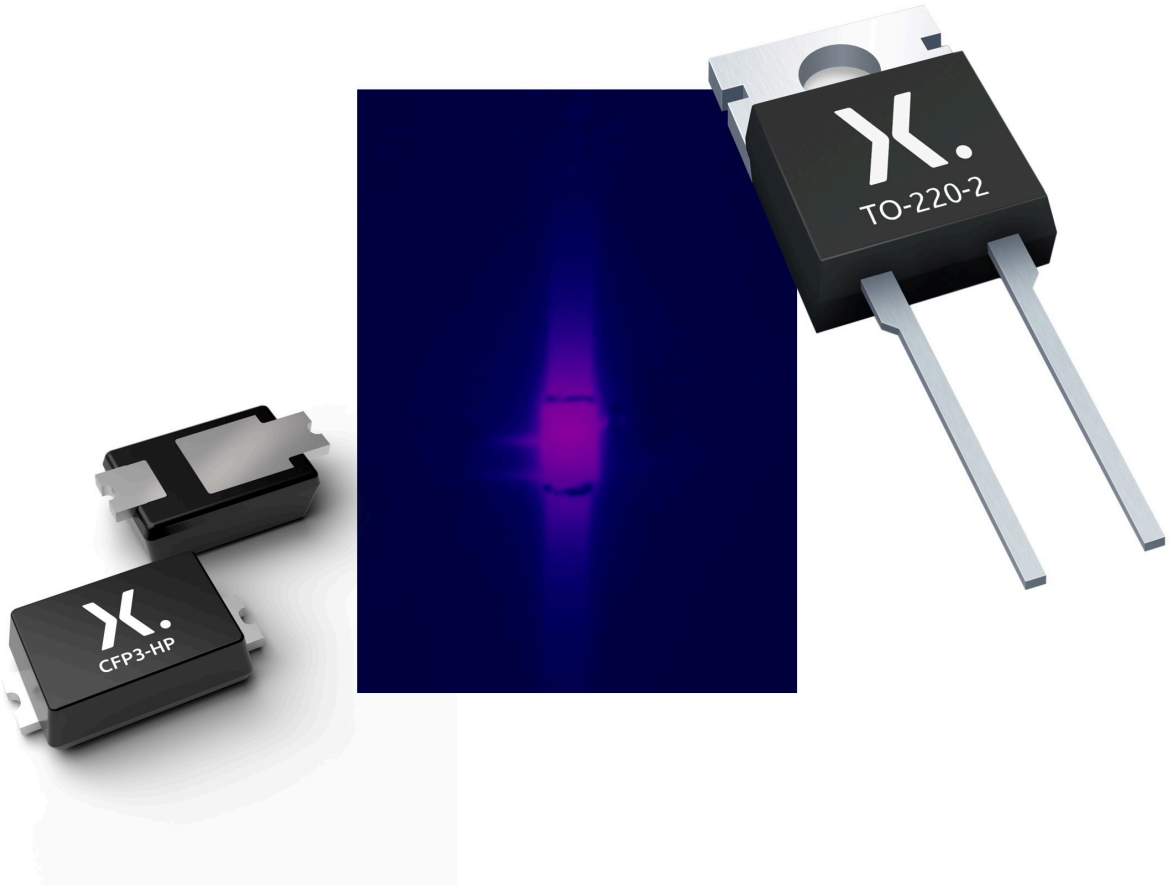
Technical note

Evaluation of junction temperature and thermal stacks using the virtual junction



Abstract: This application note is going to introduce the Virtual Junction Temperature (VJT) measurement method, which provides a nondestructive way to calculate the junction temperature as well as the thermal resistance of a thermal stack.

Keywords: Junction temperature measurement method

nexperia

1. Introduction

Measuring the junction temperature and the thermal impedance of semiconductors has been a challenge and has gone through multiple iterations in standardization. From MIL-STD-883E to JESD51-1 the measurement standard to measure the junction temperature and calculate the thermal impedance of a device has changed significantly. With the current Transient Dual Interface Measurement (TDIM) the standard is clearly defined to measure the thermal impedance of a device which is widely used in the industry.

This application note is going to introduce the Virtual Junction Temperature (VJT) measurement method, which provides a nondestructive way to calculate the junction temperature as well as the thermal resistance of a thermal stack. The measurement method is an easy and fast alternative to TDIM to evaluate the performance of a device. As the measurement method is closely linked to the application in which the device is used, the performance in the final design can be estimated from it.

As this measurement method can also be used to evaluate different parts of the complete thermal stack, the performance of certain thermal interface materials and their effect on an application will be discussed.

For this application note Nexperia's PSC1065K Silicon Carbide (SiC) diodes and rectifiers in Clip-bonded Flat Power (CFP) packages are going to be used as a reference.

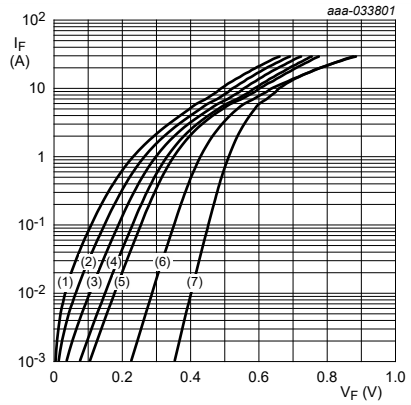
2. Measurement method

Measuring the junction temperature of a device has always been a problem as the semiconductors are usually embedded in mold compound. Therefore, it is not possible to reach the junction with an infrared camera or a thermocouple. The MIL-STD-883E standard used destructive procedures to reach the junction with a thermocouple or an infrared camera. As this is not always wanted and also not applicable in applications, herein the measurement method of virtual junction temperature shall be introduced which does not harm the device and is providing a close approximation of the performance in the application.

2.1. Temperature sensitive parameter

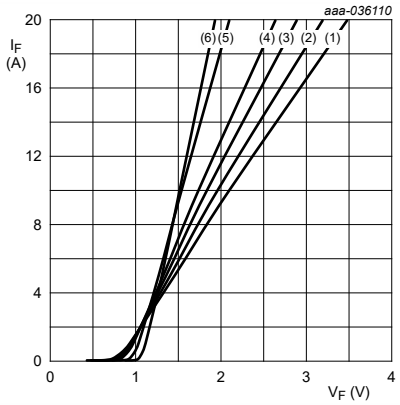
To determine the junction temperature, a Temperature Sensitive Parameter (TSP) is needed. A temperature sensitive parameter describes a physical quantity which shows a distinct shift against temperature variation. If this parameter is clearly quantified by measurement, it can be used to back trace the temperature. This temperature dependency can be used as an indicator to calculate the junction temperature in steady state.

Examples of temperature sensitive parameters are the voltage drop of a diode in forward bias or the Drain-Source on-Resistance (R_{DSon}) of a MOSFET. Figure 1 displays the forward voltage drop of a Schottky diode from Nexperia. The voltage drop decreases for the same forward current with higher temperatures. Due to this behavior these kinds of characteristics are described with Negative Temperature Coefficient (NTC). It can also be the other way around if for example a SiC rectifier is used. The characteristic of a SiC rectifier is shown in Figure 2 where it is visible that the voltage drop increases with rising temperature at a fixed current. This characteristic is described with Positive Temperature Coefficients (PTC).



pulsed condition
(1) T_j = 175 °C
(2) T_j = 150 °C
(3) T_j = 125 °C
(4) T_j = 100 °C
(5) T_j = 85 °C
(6) T_j = 25 °C
(7) T_j = -40 °C

Fig. 1. PMEG100T200ELPE I-V: Forward current as a function of forward voltage; typical values



pulsed condition
(1) T_j = 175 °C
(2) T_j = 150 °C
(3) T_j = 125 °C
(4) T_j = 100 °C
(5) T_j = 25 °C
(6) T_j = -55 °C

Fig. 2. PSC1065K I-V: Forward current as a function of forward voltage; typical values

Regardless of PTC or NTC behavior as long as the quantity shows a distinct temperature behavior, it can be used as a TSP to evaluate the junction temperature. Rectifiers and their TSP will be used in the proceedings.

To make use of a TSP it is important that the bigger the temperature shift of the physical quantity the better for distinguishing between measurement points. Using rectifiers there are two ways to make use of their temperature dependency. Either by applying a fixed current and measuring the voltage drop or by applying a fixed voltage and measuring the current going through the device. To display the temperature shift of the physical quantity the forward I-V curve of the PSC1065K can be used (Figure 2). Extracting the forward current of different temperatures at a specific voltage yields the temperature shift of the devices forward current. In Figure 3 the forward current for 1 V, 2 V and 3 V forward voltage are shown for junction temperatures ranging from -55 °C to 175 °C.

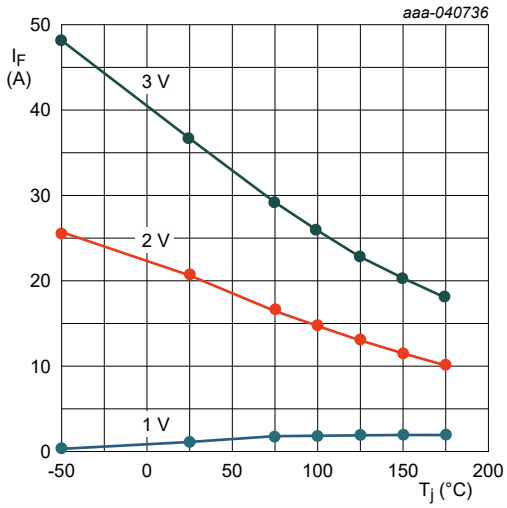


Fig. 3. PSC1065K: Forward currents over junction temperatures at different forward voltages

Putting the device under a fixed voltage like 2 V or 3 V shows a clear temperature shift of the forward current. At the same time, it is also visible that 1 V would not be a suitable fixed voltage as it is only showing a small temperature shift of the forward current. A device specific problem can be the power loss and consequently the heat dissipation that would result from a constant voltage applied to the rectifier. Taking the constant 3 V as an example: At 0 °C of junction temperature the current of the diode would be at 40 A of forward current. Having this as a constant current and voltage through the device would lead to a power level that would be challenging to dissipate and could lead to destruction of the device. Additionally, it would be above the usually operational current level of the device and also very challenging to keep the junction at the defined target temperature.

Looking at constant forward current applied to the diode shows a different picture. As shown in Figure 4 the constant currents 10 A, 12.5 A and 15 A create a comparable shape of voltage drop in the given range of junction temperatures. The difference in voltage drop between the junction temperatures for the different fixed currents indicate a measurable shift of the physical quantity over temperature. At a constant 3 A the curve shows two changes of slopes of the curve, indicating a change from NTC to PTC and thereby going through the Zero-Temperature Coefficient (ZTC) regime. In the ZTC regime there is no change in the temperature of the physical quantity. Looking at Figure 2 it is visible that all lines of the I-V curve go through roughly the same voltage and current point for all temperatures. ZTC regimes are typical for SiC rectifiers as they change from NTC to PTC behavior at low currents.

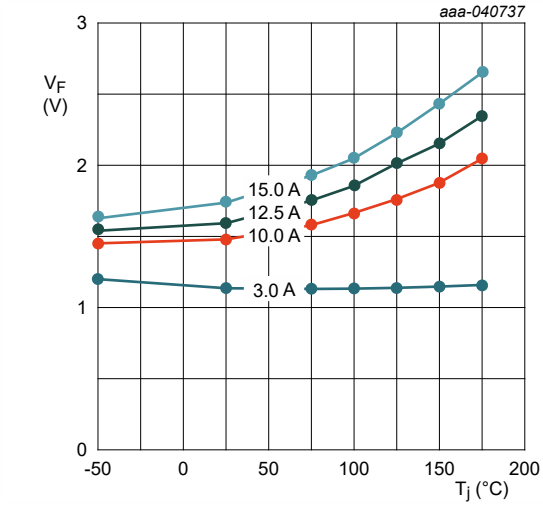


Fig. 4. PSC1065K: Forward voltages over junction temperatures at different forward currents

As a conclusion, it is favorable to have a big shift over temperature of the physical quantity (forward voltage and forward current). The device's characteristics must be kept in mind as a big shift in the physical quantity over temperature can lead to an increase of power which the device may not be able to handle. Also, the changes in the temperature coefficients have to be kept in mind as points of ZTC do not show any shift over temperature of the physical quantity.

2.2. Virtual junction temperature measurement method

The first step of the procedure and to make use of the TSP in a measurement method the forward I-V curves of one specific rectifier have to be obtained. Typically the I-V curves are measured in a climate-controlled chamber with a curve tracer. In this climate-controlled chamber, the goal is to reach thermal equilibrium between junction and ambient temeprature. Having the junction and the ambient at the same temperature is crucial as only by this way it is possible to know the junction temperature of the device. Typical temperatures of the I-V curves are between room temperature of 25 °C and maximum temperature of the junction, which are usually at 150 °C or 175 °C. During the measurement of the I-V curves it has to be ensured that the pulse width used to determine the forward voltage drop needs to be as short as possible to minimize self heating of the device during the coduction phase. To avoid cumulative increase of the junction temeperature caused by repetitive I-V curve measurement stess a suitable pause between the pulses should also be used to let the device reach the ambient temperature of the chamberagain before the next I-V curve measurement is initiated. The principle time-dependent junction temperature rise of a device during the I-V curve measurement phase is shown in Figure 5. The measurement of the forward voltage drop should be taken in the early phase of the input pulse as there is some heat up in the device taking place. When the input pulse is over the device is still taking time to cool down. The pause between the first and second pulse therefore should be as long as possible to let the device cool down to ambient temperature again.

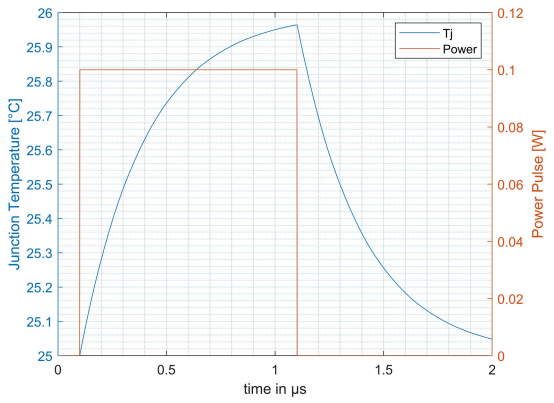


Fig. 5. Exemplary heat up of a device during conduction phase

Measurements conducted for this document used a pulse length of 300 µs while the measurement was taken in a 10 µs window and a pause between the pulses of 1 s. Note that it is relevant to obtain these curves for every Device Under Test (DUT) as this increases the accuracy of the measurement method and mitigates the risk of device tolerances to each other and to the datasheet.

After obtaining the forward I-V curves the device is ready to be tested. Before the start of the next measurement the device needs to be mounted on a Printed-Curciut Board (PCB) where the DUT can be stressed with a constant current. At the same time it has to made sure that it is also possible to measure the voltage drop of the device while it is under load.

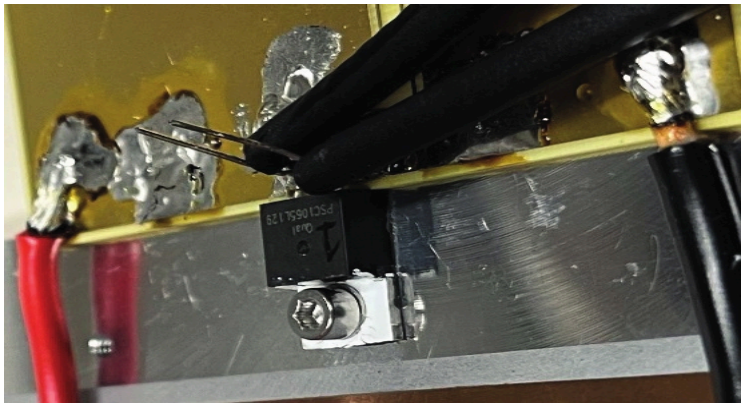


Fig. 6. Mounted TO-220 device on heatsink and wired with measurement and power wires.

Measuring the voltage drop of the device is crucial as this is the parameter from which the junction temperature can be calculated. It is recommended to measure the voltage drop as close to the DUT as possible to mitigate the influence of connections and wires.

To start the measurement a fixed current has to be applied to the DUT. As soon as a steady state of the voltage drop is reached the voltage drop of the DUT is to be measured. A constant voltage drop can be achieved more easily if the DUT is cooled via a heatsink like in Figure 6. As this voltage drop is an idicator of the junction temperature a steady voltage drop corresponds to a steady temperature in the junction. With this voltage drop the junction temperature can be estimated from the I-V curves.

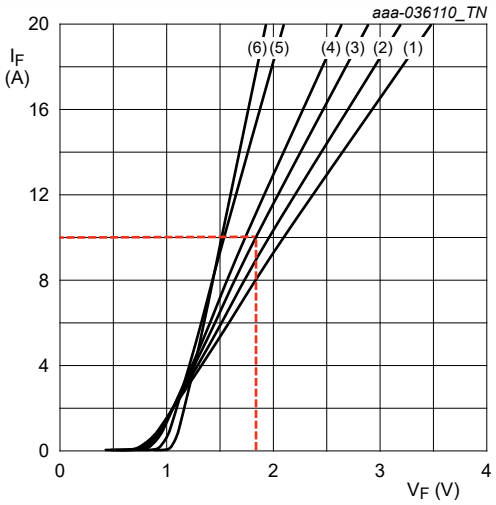


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Fig. 7. PSC1065K I-V curve

Printing the voltage drop of the device and the load current of 10 A into the I-V curves shows the estimated temperature in the junction. As an example Figure 7 shows the forward I-V curve of the PSC1065K. In this example a forward voltage drop of 1.78 V at 10 A forward current was measured. As the resulting point of the horizontal forward current line and the vertical forward voltage line is on the 125 °C I-V curve the junction temperature can be estimated to 125 °C

The evaluated temperature is called Virtual Junction Temperature (VJT). It is called this way as it is not a direct measurement of the junction temperature but indirect calculation through a TSP.

3. Measuring thermal stacks using VJT measurement method

In the following sections it is explained how the VJT measurement method can be used to obtain the thermal resistance and the total dissipated power of a given thermal stack.

3.1. Thermal stack

The described VJT measurement method can be used to evaluate the junction temperature. This virtual junction temperature is needed to evaluate a complete thermal stack. A thermal stack is here described by the path the heat needs to flow from the junction to ambient.

Heat and its path can be described as an equivalent electric circuit via an analogy as shown in the following table.

Table 1. Analogy for electric circuit

Electric	Thermal
Potential difference (V)	Temperature difference (K)
Electrical resistance (Ω)	Thermal resistance (K/W)
Electrical power (I)	Power / Heat flow (W)
Electrical capacitance (F)	Thermal capacitance (J/K)

The junction would be the source and the ambient would be the sink. The different connections of layers or materials can be reflected as resistances which are measured in K/W.

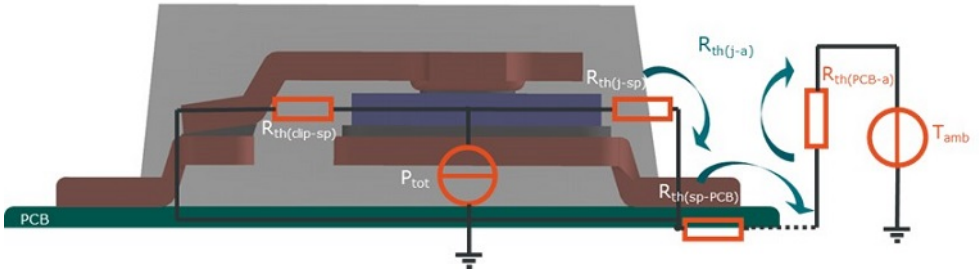

Fig. 8. Equivalent circuit of CFP package

For Nexperia's CFP package the thermal equivalent circuit is given in Figure 8. The heat is generated in the die which is positioned in the middle of the package highlighted in blue. From there, the heat can flow either through the clip at the top of the die to the solder point on the left side or through the bottom lead frame to the solder point on the right side. Both heat flows end in the PCB from where the heat can dissipate to ambient. All of these interconnections and heat paths can be used in calculations as thermal resistances. The source of the heat would be the die itself with a certain power P_{tot}. The ambient most of the times is at a certain temperature like 25 °C which is why another source is put into the equivalent circuit to implement the temperature level.

The resulting total thermal resistance for the CFP package mounted on the PCB is defined by the following.

$$R_{th,tot} = \left(R_{th(clip-sp)} \,||\, R_{th(j-sp)}\right) + R_{th(sp-PCB)} + R_{th(PCB-a)} \quad (1)$$

From equation 1 it is visible that there are four thermal resistances. Two thermal resistances show the heat path from the junction to the solder point of the package. The equation describes that the additional heat dissipation path, caused by the clip, leads to a parallel connection effectively lowering the overall thermal resistance. This additional heat path is a great benefit of the CFP package compared to wire bonded devices as the wire bond is less effective in transferring heat. From the solder points the thermal resistance to the PCB is defined and another thermal resistance from the PCB to air.

Parts of this total thermal resistance are defined in the datasheet of a respective product. Looking exemplarily at the PMEG060V030EPE by Nexperia, junction to ambient and junction to solder point thermal resistances are given.

Table 2. Thermal resistances of PMEG060V030EPE

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	90	K/W
			[2]	-	-	70	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		[2]	-	-	3	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for cathode 1 cm^2.

The thermal resistance from the junction to the solder point for the PMEG060V030EPE is 3 K/W. For this specific value the solder point is the one of the cathode tab. This thermal resistance can also be found in the equivalent circuit in Figure 8. The total thermal resistance from junction to ambient is also given but at the same time it shows that it is mostly defined by the different PCB designs expressed in the footnotes.

It has to be noted that these thermal resistances are measured using the JESD 51-2 (JEDEC 51-14) standard making use of the TDIM.

Key takeaways for the thermal stack are that the thermal resistance junction to solder point is part of the total thermal resistance and the thermal resistance junction to ambient is PCB design and therefore cooling specific.

3.2. Thermal stack evaluation of surface mounted devices on PCB

To evaluate different thermal stacks of surface mounted devices the VJT measurement method can be used. The total thermal stack for a CFP package on a PCB is defined by equation 1.

Not all of the parameters in the formula are given as they are device, package and PCB specific. This is where the VJT measurement method comes into play.

The thermal resistance can be calculated from this formula:

$$\Delta T = R_{\mathrm{th,tot}} \cdot P_{\mathrm{tot}} \tag{2}$$

By dividing the temperature difference ΔT by the total power put through the device P_{tot} the total thermal resistance is gained. From the temperature and current dependend voltage over and the current throught the device the total power can be calculated.

$$R_{\mathrm{th,tot}} = \frac{P_{\mathrm{tot}}}{\Delta \mathrm{T}} \tag{3}$$

The temperature difference ΔT is defined as the difference between the start and the end point of the thermal path. In this case, the temperature difference is defined from junction to ambient.

To calculate the total thermal resistance of the PCB with the mounted device the PCB needs to be put on a heatsink that is set to ambient temperature as it is shown in Table 2.

Putting the heatsink to the same temperature as the ambient reduces equation 1 by the thermal resistance from heatsink to ambient.

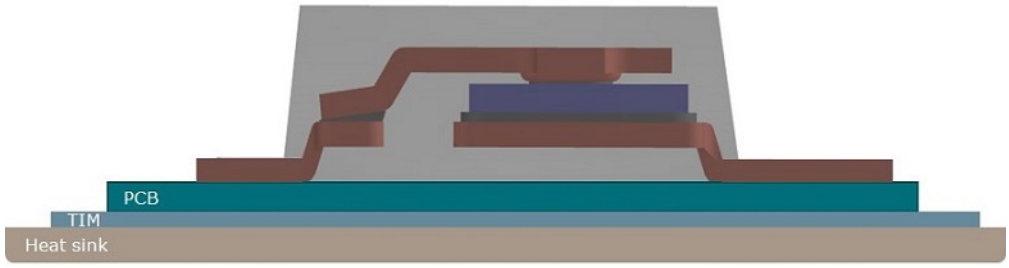

Fig. 9. Configuration of SMD package evaluation.

In between the PCB and the heatsink a Thermal Interface Material (TIM) needs to be placed to create a low resistive heat path from the PCB to the heatsink. Using a TIM reduces the thermal resistance from the PCB to ambient. Using this configuration results in a new thermal resistances. The new thermal resistance is defined from the PCB to the heatsink and is influenced by the TIM and the thermal characteristics of the PCB. The total thermal resistance for the new thermal stack is calculated using the following equation:

$$R_{th,tot} = \left(R_{th(clip-sp)} \,||\, R_{th(j-sp)}\right) + R_{th(sp-PCB)} + R_{th(PCB-hs)} \quad (4)$$

Using the VJT measurement method, multiple measurement points should be taken at different power levels while storing the value of power put through the device as well as recording the voltage drop as this is used to estimate the junction temperature. Using the stored data the temperature difference ΔT can be calculated as subtracting the heatsink temperature from the virtual junction temperature would yield the temperature difference ΔT. The total thermal resistance can be calculated using equation 4 .

If the device's thermal resistance and the TIM thermal resistance is known, the PCB can be evaluated in terms of thermal characteristics. By subtracting the device specific thermal resistance as well as the thermal resistance of the TIM from the total resistance the thermal resistance of the PCB is left.

$$R_{th(sp-PCB)} + R_{th(PCB-hs)} = R_{th,tot} - \left(R_{th(clip-sp)} \,||\, R_{th(j-sp)}\right) - R_{th,\ TIM} \quad (5)$$

Improvements to the PCB design – changing from two to four layers and adding exposed copper areas or vias – can improve the total thermal resistance of the complete thermal stack.

With this way of working different PCB designs and layouts can be tested and evaluated in terms of thermal performance. Additionally, the thermal performance of different packages can be evaluated for the same kind of PCB which can be used as an in-application test.

3.3. Evaluation of thermal interface material

Another way of using VJT is to evaluate thermal interface materials. A device with an electrically conductive metal tap like a PSC1065K in TO-220-2 R2P needs to be used. The device needs to be soldered on an evaluation PCB where the device is on the edge of the PCB. This device should then be attached to a heatsink with a repeatable mounting torque and a TIM in between. The setup used is shown in Figure 9. This configuration would lead to a total thermal resistance of:

$$R_{th,\,tot} = R_{th\,(j\text{–}c)} + R_{th\,(c\text{–}hs)} + R_{th\,(hs\text{–}a)} \quad (6)$$

A figure of the thermal stack and its resistances is given below.

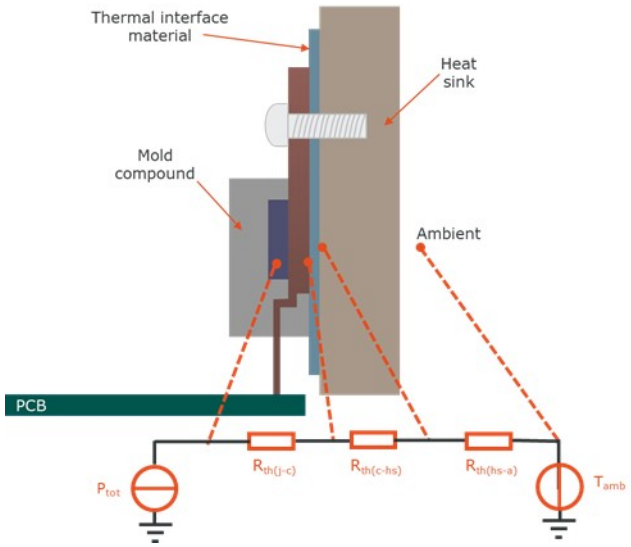

Fig. 10. Thermal interface material evaluation configuration.

The thermal path from the leads to the PCB is neglected in this case as the main heat path is through the metal tab at the bottom side of the device. The thermal resistance of the leads is very high compared to the thermal resistance through the bottom side into the heat sink.

To evaluate the influence of the TIM in the complete thermal stack the $R_{th(j\text{-}c)}$ and $R_{th(hs\text{-}a)}$ are needed. From the datasheet the thermal resistance from junction to the case bottom side can be used. If the heatsink temperature can be kept at ambient temperature (usually 25 °C) $R_{th(hs\text{-}a)}$ can be neglected. Then the only unknown thermal resistance would be $R_{th(c\text{-}hs)}$ which is the thermal resistance of the thermal interface material.

From here the same procedure as for the evaluation of the thermal stack should be used. Measuring the total power put through the device as well as the voltage drop of the device are needed to evaluate the junction temperature and therefore the temperature difference ΔT.

Using equation 3 will result in the total thermal resistance of the stack. Subtracting the thermal resistance $R_{th(j\text{-}c)}$ from the total thermal resistance and neglecting the thermal resistance $R_{th(hs\text{-}a)}$ from the heatsink to ambient the thermal resistance of the thermal interface material is obtained. Remember that this only holds true if the heatsink is attached and kept at room temperature.

Using the explained method different thermal interface materials were investigated. The different TIMs used in this investigation can be put into three categories: Thermal pads, ceramic plates and phase change materials. Thermal pads can be an ideal solution as they offer great thermal conduction while being electrically isolating, depending on the thickness of the pad. Ceramic plates are even better isolators but need additional thermal paste to offer good thermal conduction. Phase change materials are, as their name suggests, hard at a certain temperature and soften with increasing temperature. Therefore, the phase change material can improve its thermal conductivity with higher temperatures as it will fill smaller gaps when getting softer. To evaluate the performance of the thermal interface materials, Nexperia's PSC1065K SiC rectifier was used and mounted with a screw and a torque of 1 Nm to a heatsink with interchangeable TIMs in between. The maximum

power was measured until the device hit a virtual junction temperature of 175 °C. The results of this investigation are given in Figure 11 .

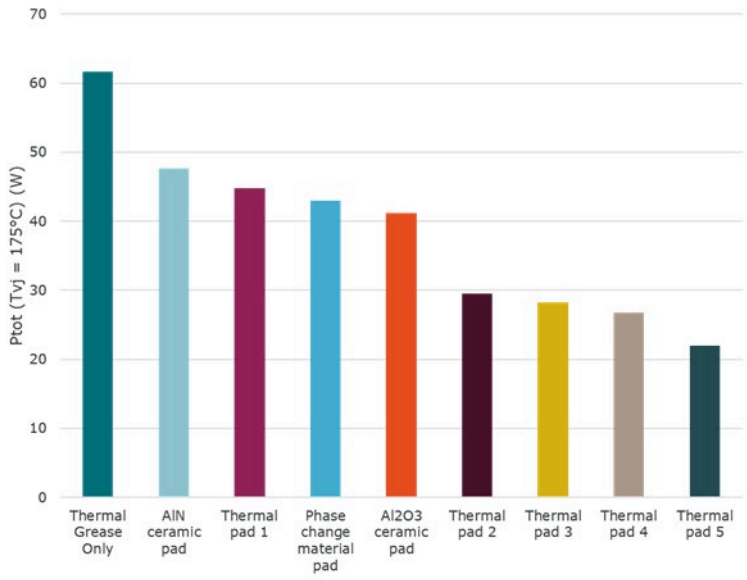

Fig. 11. Overview of maximum power throughput of PSC1065K with different thermal interface materials.

The results show that the thermal resistance of the used thermal interface material can have a bigger influence on the performance of the thermals stack than the thermal resistance of the used device. The PSC1065K can dissipate up to 65 W of power if the bottom side of the case can be kept at 25 °C. Using thermal pads 2-5 can reduce this capability by over 50 %. This reduction in performance can have a huge impact on the performance of the complete application as the increased heat in the device would also lead to a higher voltage drop across the device while in conduction phase. In a switching topology like a buck converter this decrease in total power dissipation would result in less switching speed or lower output current capability as the device could not perform to its maximum.

4. Thermal resistance instead of thermal impedance

This application note focused heavily on the thermal resistance of a device or a thermal stack and not on the thermal impedance. In fact, the thermal resistance can be sufficient enough to estimate the performance of a device even in a switching application.

As an example, a buck converter at room temperature with Nexperia's PSC1065K is to be evaluated.

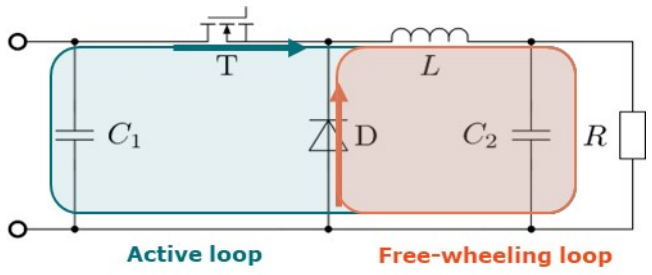

Fig. 12. Current flow in buck converter.

The buck converter is driven at a switching frequency of f_s = 100 kHz and a duty cycle D = 0.5. This leads to a conduction phase of the diode of t_p = 5 µs. In this example during the conduction phase of the diode a power of 20 W needs to be dissipated. With these data points the thermal impedance of the device can be taken from the datasheet graph:

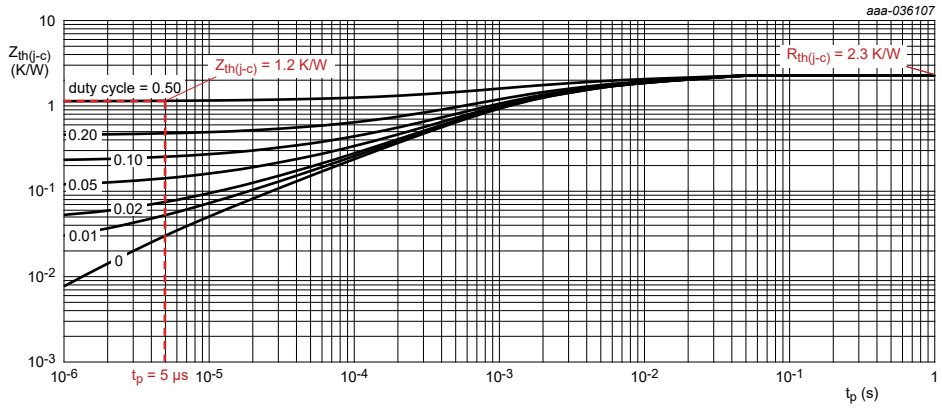

Fig. 13. Thermal resistance and impedance of PSC1065K

The evaluation from the datasheet graph results in a $Z_{th(j-c)}$ = 1.2 K/W and an $R_{th(j-c)}$ = 2.3 K/W. With these thermal parameters it is possible to calculate the junction temperature for a given power load.

With the given 20 W of peak power in the diode the junction temperature can be estimated. Using the thermal impedance gives the following formula:

$$R_{j(max)} = Z_{th(j-c)} \cdot P_{D(max)} + T_c \quad (7)$$

Using the data points given in the example results in a junction temperature of $T_{j(max)}$ = 49 °C.

If the thermal resistance of the diode is used the average power through the diode needs to be used. With a duty cycle of D = 0.5 the average power through the diode is $P_{D(avg)}$ = 10 W. The described data and the value for the thermal resistance from Figure 14 can be used to calculate the junction temperature.

(8) $$R_{j\,(max)} = Z_{th\,(j-c)} \cdot P_{D\,(max)} + T_c$$

The resulting calculated average junction temperature is $T_{j(avg)}$ = 48 °C. This is an error of 2 % compared to the results using Z_{th}.

An approximation of the heat process inside the device can be seen in Figure 14.

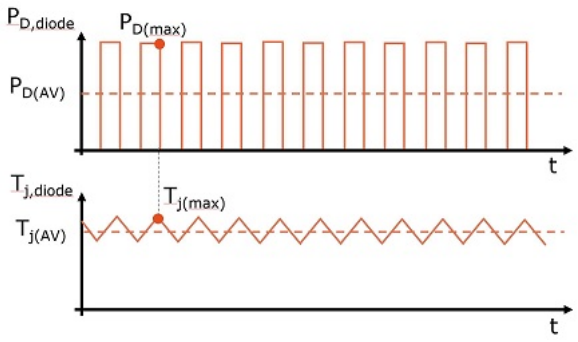

Fig. 14. Approximated heat generation in PSC1065K in a buck converter

These calculations indicate that the thermal resistance can be accurate enough to estimate the thermal performance of a thermal stack or a device in an application. In the shown example it holds true but with varying switching frequencies and device characteristics the results can differ more heavily.

5. Conclusion

The explained measurement method of the virtual junction temperature has its presented upsides. Comparing it against the established TDIM results in advantages and disadvantages of the VJT measurement method as shown in the following table.

+ Advantages	- Disadvantages
• Non-destructive method • Direct measurement method • Reliable and repeatable • Reasonably accurate estimate of P_{tot} and T_{vj} when compared to TDIM measurements • Good estimate of the thermal resistance for a given thermal stack • Measurement can be adopted for PTC (e.g. SiC Schottky) and NTC (e.g. Si Schottky) rectifiers, as well as MOSFETs and bipolar junction transistors • With enough access the test method can be adopted in the final application	• Device specific measurements • Static measurement method, hence transient thermal analysis is not possible but for high frequency power applications the steady state thermal resistance can play an important role • Inaccuracies in measurements can occur when the IV curves for different temperatures overlap, especially during transitions from the NTC to the PTC regime or the zero temperature coefficient regime

The described VJT measurement method can be used to evaluate thermal stacks. Especially if an SMD device is mounted on a PCB the thermal connection of the device to the PCB and its heat sink capabilities can be evaluated. This can be an ideal opportunity to observe the performance of different packages on the same PCB layout to see the limitations of the device used and upsides of packages to which the original device is compared to. Specially the performance of Nexperia's CFP against commonly used SMA, SMB and SMC packages can be evaluated and the performance benefits of CFP packages can be highlighted.

This measurement method is not restricted to SMD packages, it can also be used for through hole technologies and others. Also thermal interface materials, which are used with through hole devices like TO-220-2 R2P, can be characterized with this method. The presented measurements even indicate that the choice of a TIM can highly influence the performance of the complete application.

Key takeaways for the thermal stack are that the thermal resistance junction to solder point is part of the total thermal resistance and the thermal resistance junction to ambient is PCB design and therefore cooling specific.

6. Revision history

Table 3. Revision history

Revision number	Date	Description
1.0	20240902	Initial version

7. Legal information

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