TN90002

H-bridge motor controller design using Nexperia discrete semiconductors and logic ICs

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Document information

Information	Content
Keywords	H-bridge, MOSFET, motor controller
Abstract	An example of a H-bridge motor controller designed with Nexperia discrete and Nexperia logic IC components.

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1. Introduction

This technical note demonstrates a H-bridge motor controller PCB, built using Nexperia discrete semiconductors and logic ICs.

The H-bridge circuit is a full bridge DC-to-DC converter allowing operation of a brushed DC motor (48 V max, 12 V min, 5 A max). The key feature of this design is that all electronic functions are designed with Nexperia discrete and logic IC components (low cost, no micro-controller or software needed).

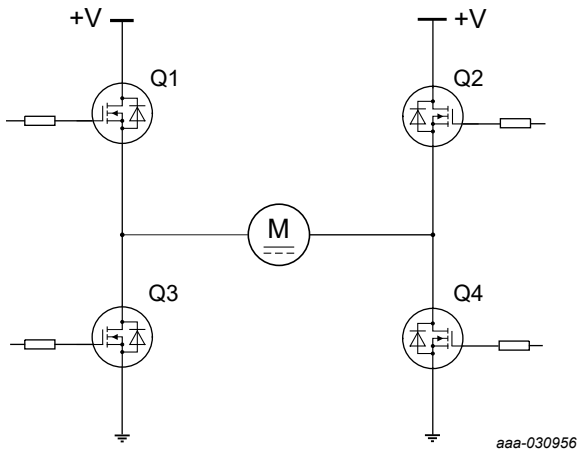


Fig. 1. Simplified MOSFET H-bridge motor control

The left MOSFETs of the full bridge (Q1 and Q3 in the simplified diagram above) are the switching MOSFETs (see the PCB top view in Fig. 26), the right MOSFETs (Q2 and Q4 in the simplified diagram above) select the motor rotation direction:

- right high side MOSFET fully ON = Forward
- right low side MOSFET fully ON = Reverse

A switch selects the motor rotation direction.

Jumpers select one of 3 switching frequencies: 7.8 kHz, 15.6 kHz or 31.3 kHz.

Two tactile push buttons allow the duty cycle (motor speed) to be increased or decreased. There are 8 steps from 0 to 100% duty cycle. A current limitation protection avoids over current in the motor and MOSFETs (set at approximately 6.5 A).

This H-bridge motor controller PCB allows the user to choose between 3 Nexperia MOSFET packages (LFPAK33, LFPAK56D or LFPAK56), jumpers are used to connect the MOSFETs chosen by the user.

This technical note describes each of the main functions used in the design.

2. Block diagram and system functionality

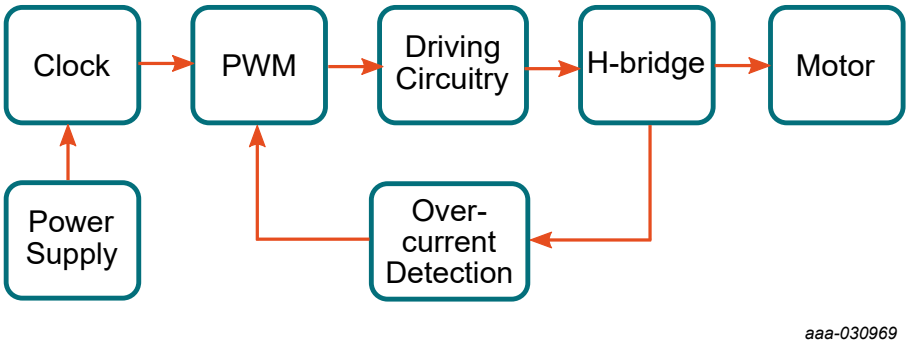


Fig. 2. H-bridge motor controller block diagram

2.1. Subsystems overview

1. Power Supply
   - Accepts 12 V to 48 V DC input
   - Transient overvoltage protection
   - Reverse polarity protection
   - Buck converter (12 V)
   - Linear regulator (5 V) for logic devices
2. Clock and duty cycle generator
   - 4 MHz crystal oscillator and frequency divider to create 3 different switching frequencies
   - Duty cycle sets by push button inputs to select the duty cycle (0% to 100%)
   - 62.5 kHz output is used to supply the charge pump on the driving circuitry block
3. PWM
   - Reset function to activate other function when V_{CC} 5 V supply is stable
   - Dead-time function and PWM enable (over current protection disabling)
   - Level shifter
   - Direction selection
4. Driver circuit
   - High-side and low-side drivers to drive 4 MOSFETs of the full bridge
   - Charge pump to supply the high-side MOSFETs
5. H-bridge
   - Reservoir and decoupling capacitors
   - Snubber on the left MOSFETs (switching MOSFETs)
   - Jumper to connect the selected MOSFETs
   - Gate drive resistors
   - Low-side current measurement
6. Overcurrent detection
   - Comparator, with voltage reference setting current limit
   - PWM reset function reactivating PWM if fault disappears

3. Subsystem descriptions

3.1. Power supply

The H-bridge motor controller power supply circuit comprises of:

- DC input stage with transient overvoltage and reverse voltage protection
- 12 V output DC-to-DC buck converter stage
- 5 V output linear regulator (for logic ICs) with status LED

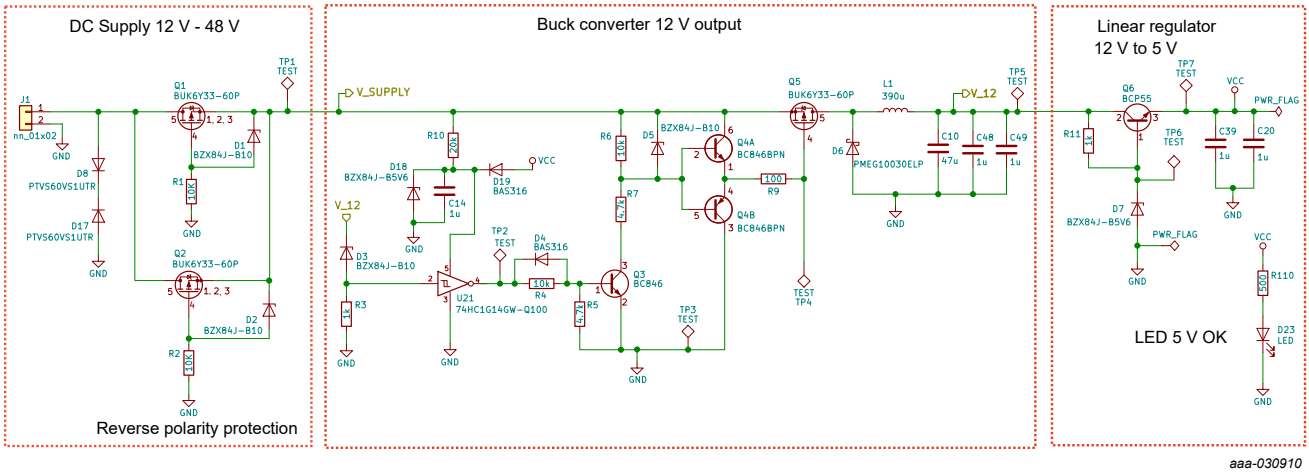


Fig. 3. Power supply circuit

Transient overvoltage protection

D8 and D17 (PTVS60VS1UTR) are transient voltage suppressor diodes, rated at 60 V, 400 W for a 10/1000 µs current pulse waveform. They protect against positive and negative transients.

Note: These TVS diodes provide protection for transient overvoltage only - not for DC overvoltage.

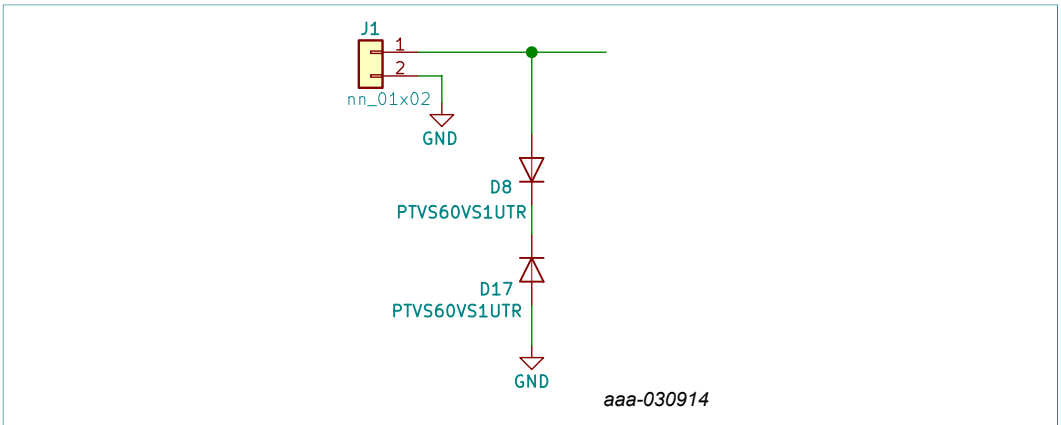


Fig. 4. Transient overvoltage protection

Reverse polarity protection

Two parallel P-channel MOSFETs Q1 and Q2 (BUK6Y33-60P) form the reverse polarity protection.

Q1 and Q2 are biased on through D1 and D2 (BZX84J-B10) respectively when the supply polarity is positive (V_{GS}= -10 V). Q1 and Q2 are off when the supply is negative (V_{GS} = V_F = 0.7 V), current cannot flow because the MOSFET body diodes are reverse biased.

This means that if the supply is inverted, no current will flow into the circuit and potentially cause damage.

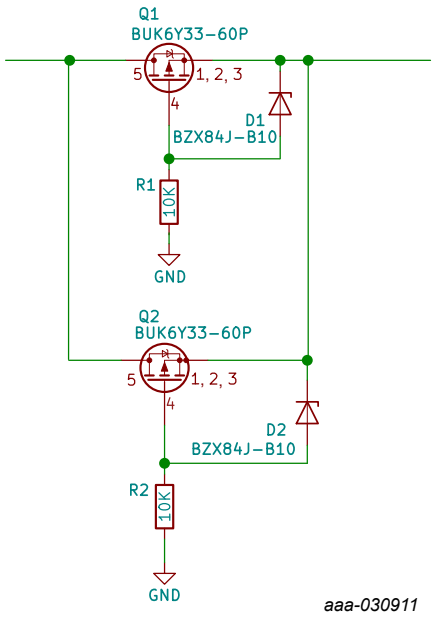


Fig. 5. Reverse polarity protection

Buck converter (12 V)

The next stage is a switching regulator that outputs 12 V. To start the switching regulator a start-up circuit is used consisting of: Zener diode D18 (BZX84J-B5V6), R10, and C14. This provides a 5 V supply for inverting Schmitt trigger U21 (74HC1G14) before V_{CC} (5 V) is available through D19 (BAS316). U21 can then start the switching regulation.

The buck converter consists of: Q5 (BUK6Y33-60P), Schottky diode D6 (PMEG10030ELP) and inductor L1. The output of the buck converter supplies the 12 V rail.

When the output of U21 is high it turns on Q5 via the NPN transistor Q3 (BC846) and the NPN/PNP dual transistor pair Q4 (BC846BPN). The voltage on node “V_12” will then increase. When “V_12” reaches 12 V, D3 (BZX84J-B10) is conducting and there is enough voltage on U21 input to force U21 output low. Then Q5 is switched off and the voltage at “V_12” decreases until U21 input is low enough to restart a new cycle.

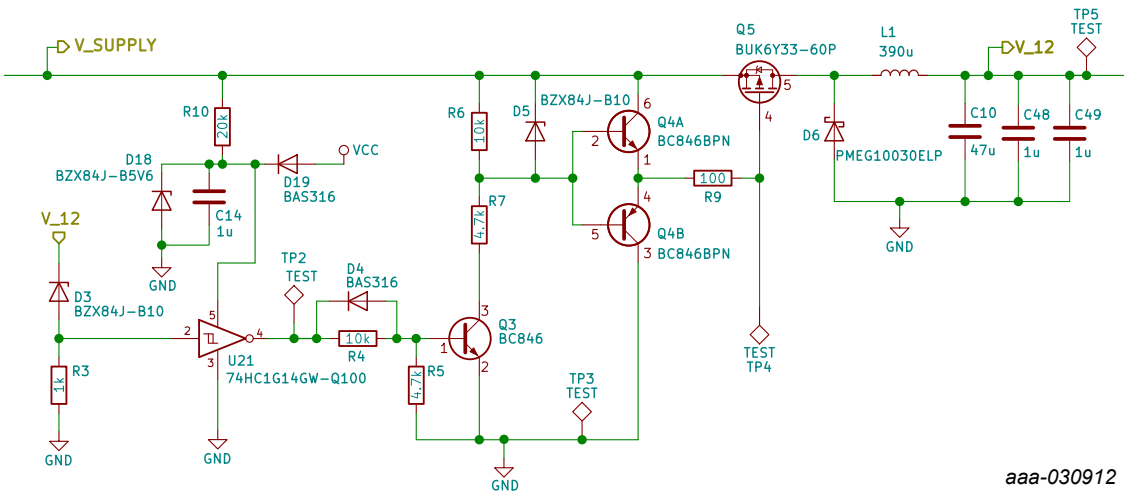


Fig. 6. Buck converter

Linear regulator (5 V) for logic ICs

A linear regulator comprising NPN transistor Q6 (BCP55), Zener diode D7 (BZX84J-B5V6) and R11 provides a regulated V_{CC} (5 V) rail for the logic ICs.

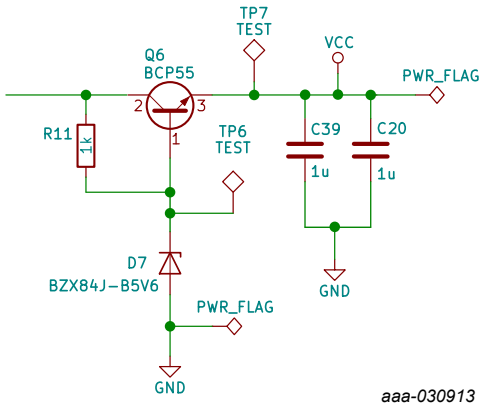


Fig. 7. Linear regulator

3.2. Clock and duty cycle generator

The Clock circuit comprises of:

- Crystal oscillator and frequency divider
- Duty cycle generator
- Frequency selection jumpers

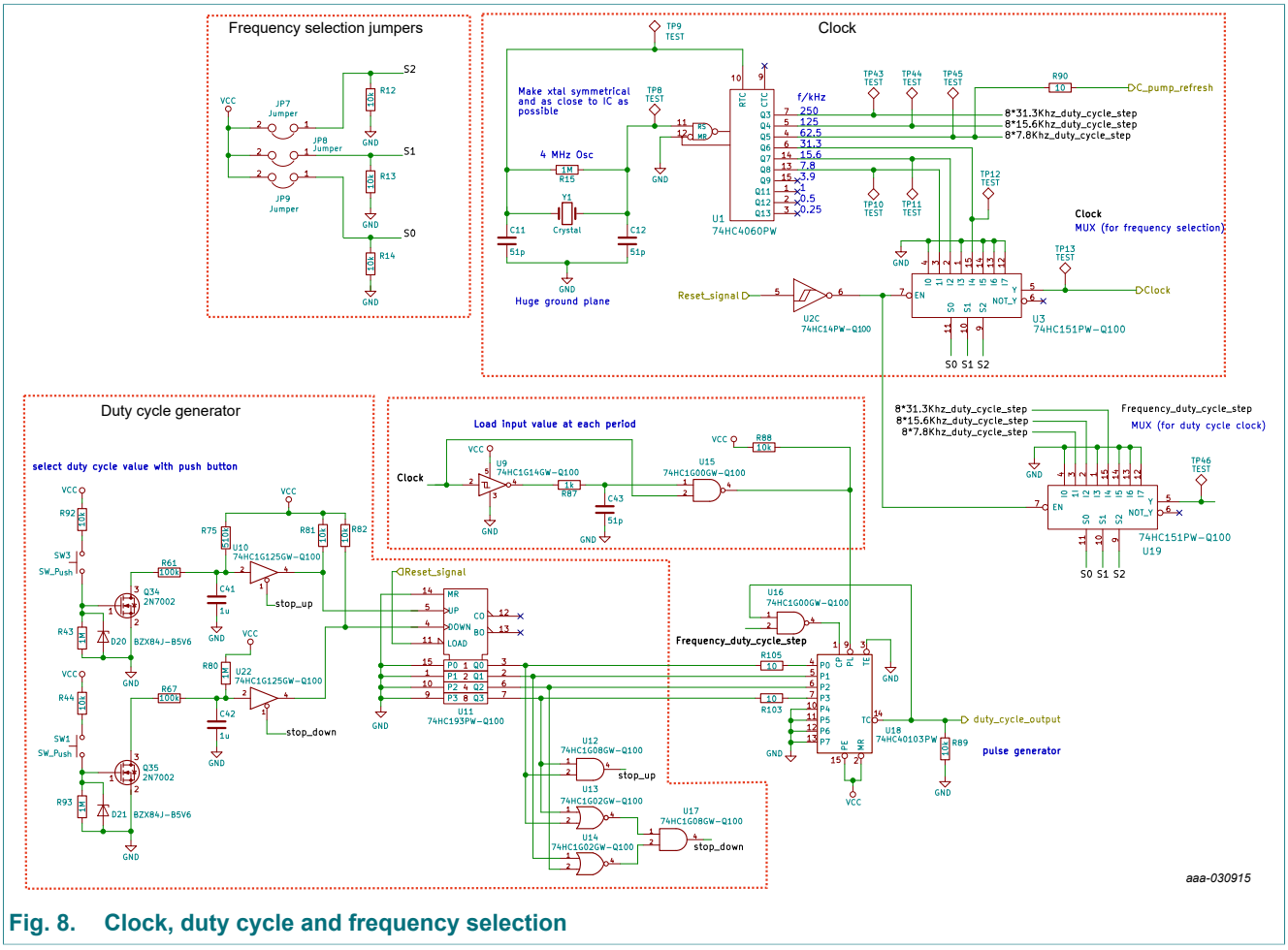


Fig. 8. Clock, duty cycle and frequency selection

Crystal oscillator and frequency divider

A crystal oscillator is used for accuracy and stability. The oscillator frequency is 4 MHz.

U1 (74HCT4060) is a frequency divider, used to obtain different frequencies from the 4 MHz. It provides outputs at:

- 62.5 kHz to drive the charge pump circuit (see Fig. 19)
- 31.3 kHz, 15.6 kHz and 7.8 kHz for the switching frequency (user selectable)

The switching frequency is selected by the multiplexer U3 (74HCT151) according to the jumper settings of JP7, JP8 and JP9.

Note: Only one jumper should be fitted at the same time.

The switching frequency output is labeled “Clock”.

A reset signal enables both multiplexer U3 and U19 (see next section for U19 explanation) when V_{CC} is 5 V.

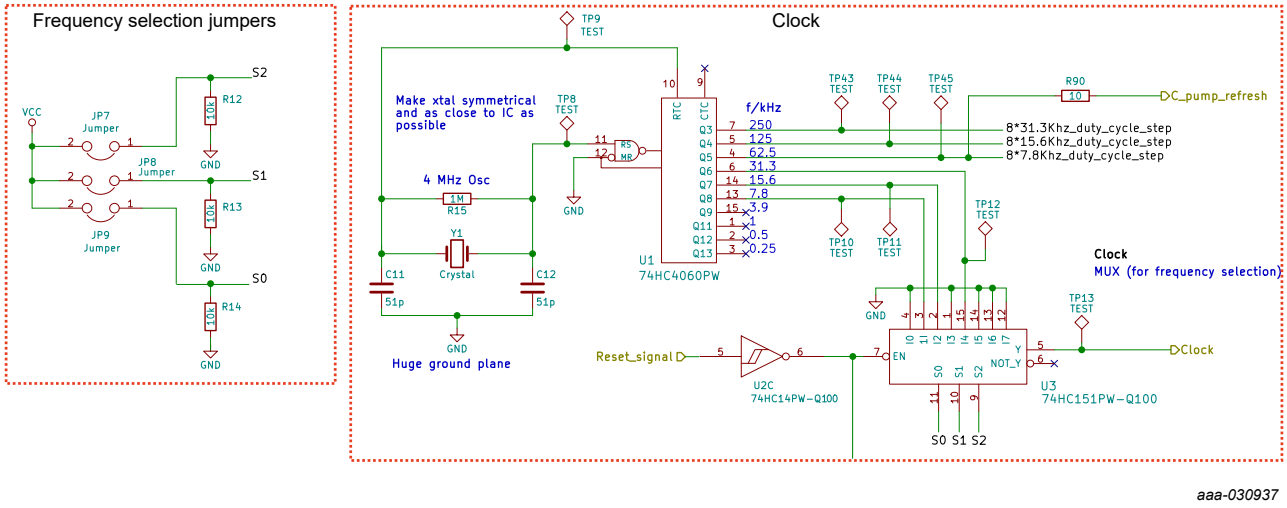


Fig. 9. Oscillator and frequency divider

Duty cycle generator

Signals with a frequency 8 times higher than the required final switching frequencies are fed to 3 of the inputs of an 8-bit multiplexer IC, U19 (74HCT151). These are labeled “8*Frequency_duty_cycle step”.

Jumpers JP7, JP8, JP9 select both the switching frequency “Clock” and at the same time, “Frequency_duty_cycle step” which is a multiple (x8) of the switching frequency.

This higher frequency is used to create 8 duty cycle steps.

“Frequency_duty_cycle step” goes into the clock input of programmable timer U18 (74HC40103PW). U18 uses "Frequency_duty_cycle step” as a clock.

U18 output produce a duty cycle time in “duty_cycle_output” equals to the value read in input (P0 to P3) multiplied by the clock period.

"duty_cycle_output” is the general output of the Clock circuit.

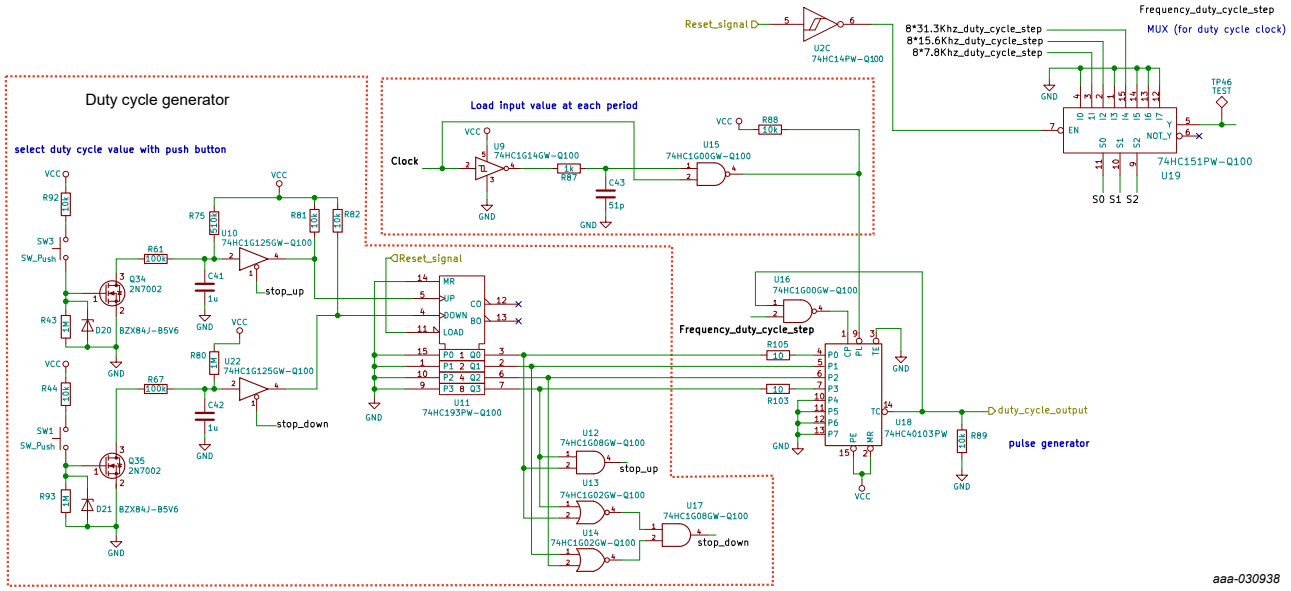


Fig. 10. Duty cycle

Table 1. Duty cycle selection

P0 (1)	P1 (2)	P2 (4)	P3 (8)	Duty Cycle
0	0	0	0	0%
1	0	0	0	12.5%
0	1	0	0	25%
1	1	0	0	37.5%
-	-	-	-	-
1	1	1	0	87.5%
0	0	0	1	100%

The signal “Clock” from U3 resets U18 at each new switching period. When reset, U18 will read inputs P0 to P3 and output a duty cycle in “duty_cycle_output” proportional to the settings.

The outputs of a 4-bit synchronous binary up/down counter U11 (74HC193) set the duty cycle value, it is the input of U18. Each time a rising edge appears on the UP input, the output value (Q0 to Q3) increases by 1, each time a rising edge appears on the DOWN input, output value (Q0 to Q3) decreases by 1.

The push buttons SW3 and SW1 with U10 and U22 (74HC1G125) create the rising edges on UP or DOWN input of U11, when the user releases the push button.

When U11 output reaches a maximum count of 9 (8 to 9 transition), (Q0 and Q3 =1), the “stop_up” output of U12 (74HC1G08) is set to 1 and U10 (74HC1G125) is deactivated (high impedance), any further impulses on SW3 can’t produce a rising edge on UP input (U11) and the duty cycle reaches a maximum.

When U11 output reaches a minimum of 0 (Q0 to Q3 = 0), U17 (74HC1G08) “stop_down” output is set to 1 and U22 (74HC1G125) is deactivated (high impedance), any further impulses on SW1 can’t produce a rising edge on DOWN input (U11) and the duty cycle reaches a minimum (after 0 the next counter value is 15, we need to stop the counter from setting duty cycle to a maximum).

3.3. Pulse Width Modulation

The PWM circuit consists of:

- PWM enable and reset
- Dead-time control
- Level shifting stage
- Direction selection

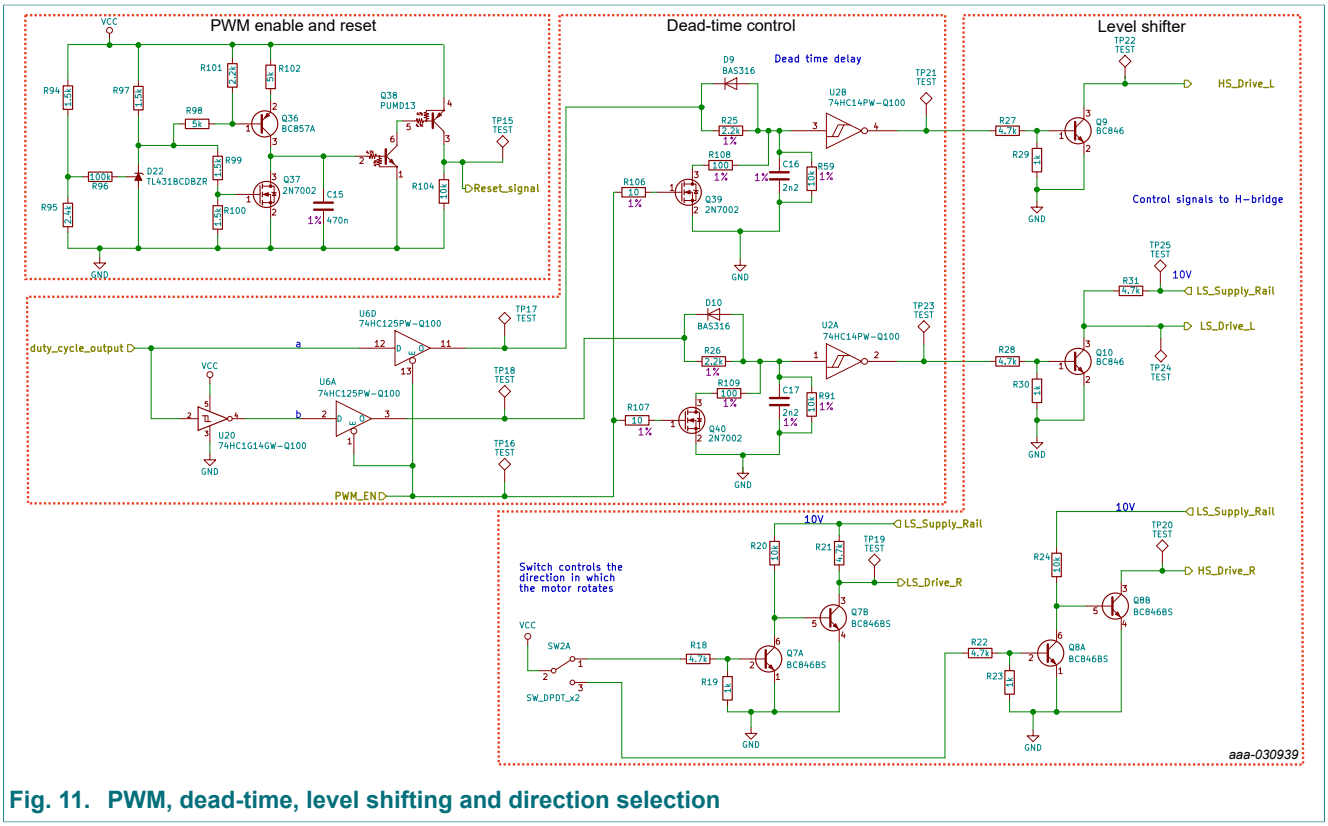


Fig. 11. PWM, dead-time, level shifting and direction selection

Reset function

The reset function to activate other function when the V_{CC} (5 V) supply is stable.

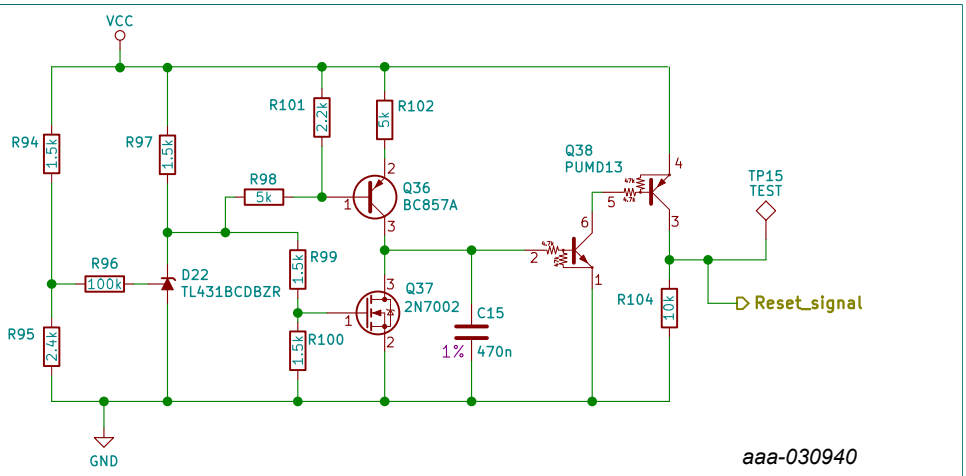


Fig. 12. Reset circuit

When V_{CC} (5 V) reaches approximately 4 V, “Reset_signal” will go high after a delay set by C15. This validates all functions enabled by this signal. This ensures that all logic ICs will start with a clean V_{CC} (5 V).

Adjustable precision shunt regulator D22 (TL431BCDBZR) acts like a comparator. PNP transistor Q36 (BC857A) is a current source charging C15 when the threshold is reached.

MOSFET Q37 (2N7002) discharge C15 when V_{CC} (5 V) is no longer present.

The dual NPN/PNP resistor-equipped transistor Q38 (PUMD13) switches “Reset_signal” high when the voltage on C15 (delay setting) reaches a value high enough to turn on the NPN transistor (input, pin 2).

Dead-time function and PWM enable (over current protection disabling)

“duty_cycle_output” is the high side command (α) and “duty_cycle_output" is inverted by U20 (74HC1G14) to create the low side command (1-α).

The duty cycle command is disabled by U6 (74HC125) through its input “PWM_EN” equal to 1 (over current protection switch U6 output in high impedance).

A dead time is controlled by U2 (74HC14) and RC filter. Q39, Q40 (2N7002) force the duty cycle to 0 when “PWM_EN” is 1.

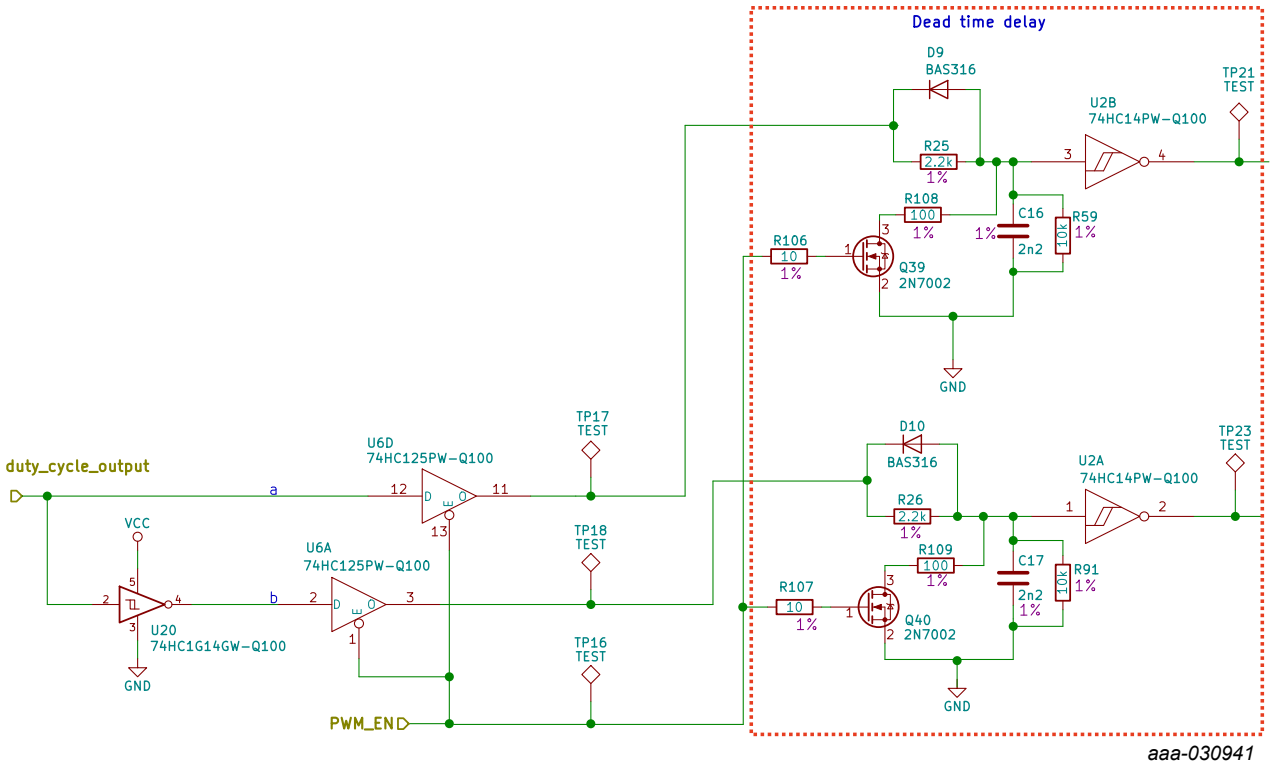


Fig. 13. Dead-time function and PWM enable

Level shifter

Transistors Q9 and Q10 (BC846) interface the 5 V duty cycle signal to the high side and low side drivers (see Section 3.4).

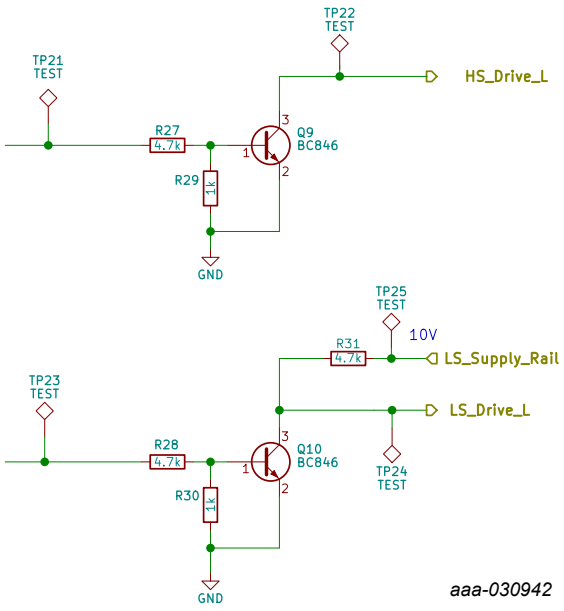


Fig. 14. Level shifter

Direction selection

Switch SW2 selects the motor direction by activating either Q7 or Q8 (BC846BS).

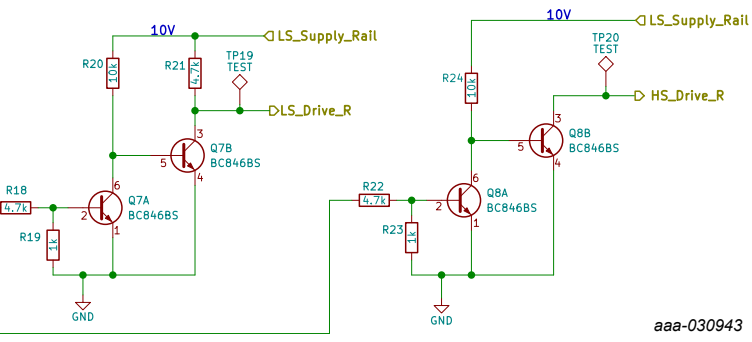


Fig. 15. Direction selection

Q7 or Q8 are fully ON and activate one of the right MOSFETs: high side fully ON or low side fully ON.

3.4. Drive circuit

The drive circuit comprises of high-side and low-side drivers to drive the 4 power MOSFETs that form the full bridge.

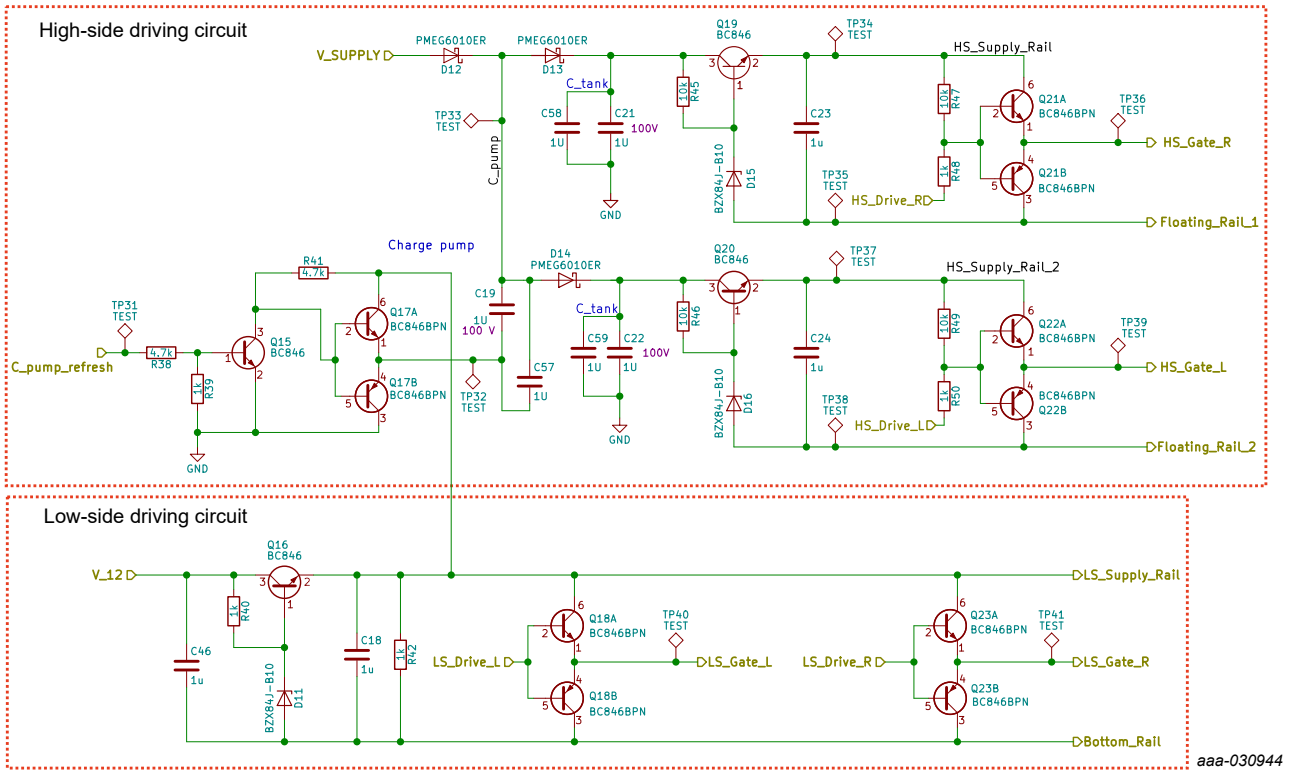


Fig. 16. Driver circuit

High-side and low-side drivers

Two high side drivers supplied by the charge pump function and regulated at 9 V:

- Q19 (BC846), D15 (BZX84J-B10), C23, R45, Q21(BC846BPN) driven by “HS_Drive_R” for the right high side
- Q20 (BC846), D16(BZX84J-B10), C24, R46, Q22(BC846BPN) driven by “HS_Drive_L” for the left high side

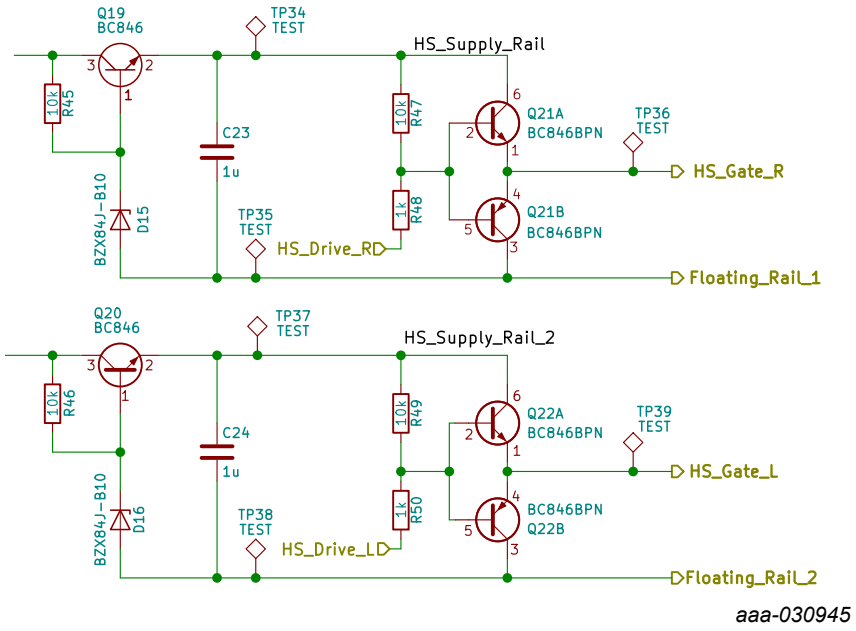


Fig. 17. High side driver circuit

Two Low side drivers supplied by the 12 V from the buck converter and regulated at 9 V

- Q16 (BC846), D11(BZX84J-B10), C18, R40 for the supply:
- Q18(BC846BPN) driven by “LS_Drive_L” for the left low side
- Q23 (BC846BPN) driven by “LS_Drive_R” for the right low side

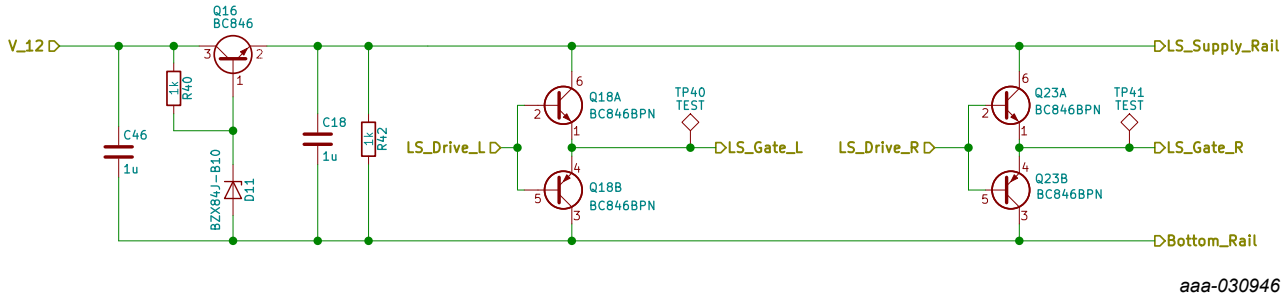


Fig. 18. Low side driver circuit

Charge pump to supply high side MOSFETs

A simple bootstrap function could be used to supply the high side MOSFETs but due to the fact the duty cycle could be 100% there is no time in this configuration to recharge the bootstrap capacitor if the high side MOSFET is fully ON (100% duty cycle) and the low side MOSFET is fully OFF.

The solution is to use a charge pump to supply the high side MOSFETs in every duty cycle configuration.

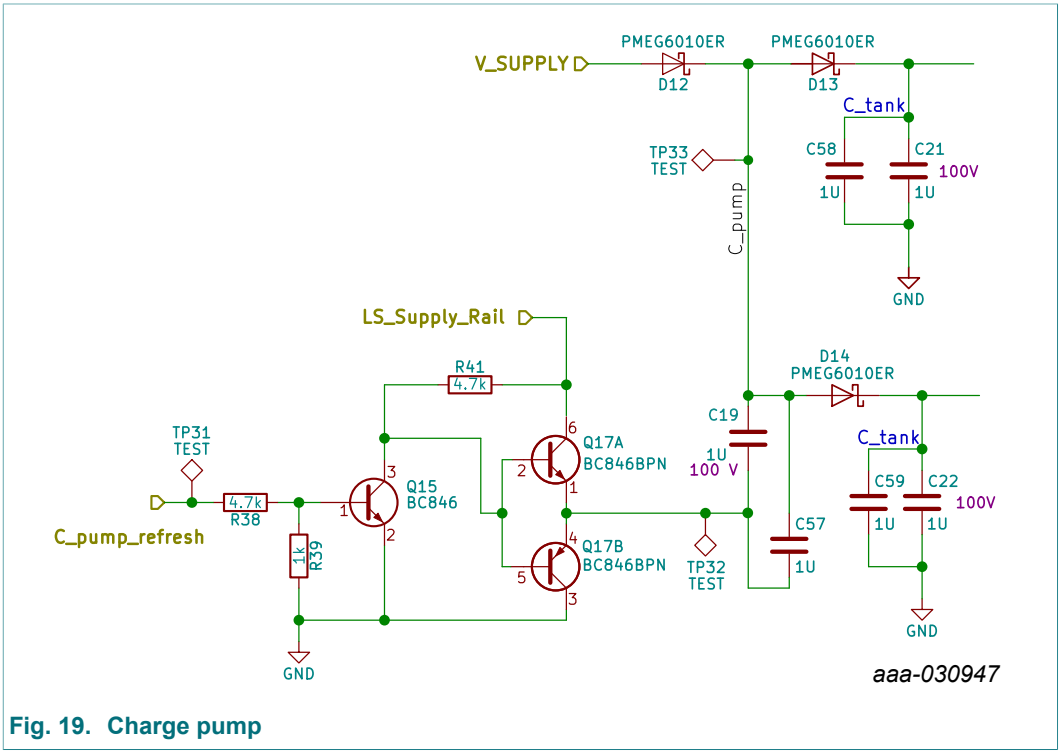


Fig. 19. Charge pump

"C_pump_refresh" from the clock function (see section Section 3.2) controls Q15 (BC846), Q17 (BC846BPN) with a frequency of 62.5 kHz, 50% duty cycle. The 9 V regulated from "LS_Supply_Rail" is applied on C19 bottom pin at 62.5 kHz, during 50% of the time, and 0 V during other 50% of the time.

Due to the fact, there is no fast voltage variation across a capacitor, there is always a voltage equals to "V_SUPPLY" across C19 ("V_SUPPLY" is the supply voltage of the H-bridge).

- When the bottom pin of C19 is 0 V, voltage across C19 is "V_SUPPLY".
- When the bottom pin of C19 is 9 V, voltage across C19 is "V_SUPPLY" +9 V.

C21 and C22 are the filtering capacitor for the driver input voltage.

3.5. H-bridge

The H-bridge circuit comprises of:

- Power MOSFETs
- Reservoir and decoupling capacitors
- Snubber components
- Low side current measurement

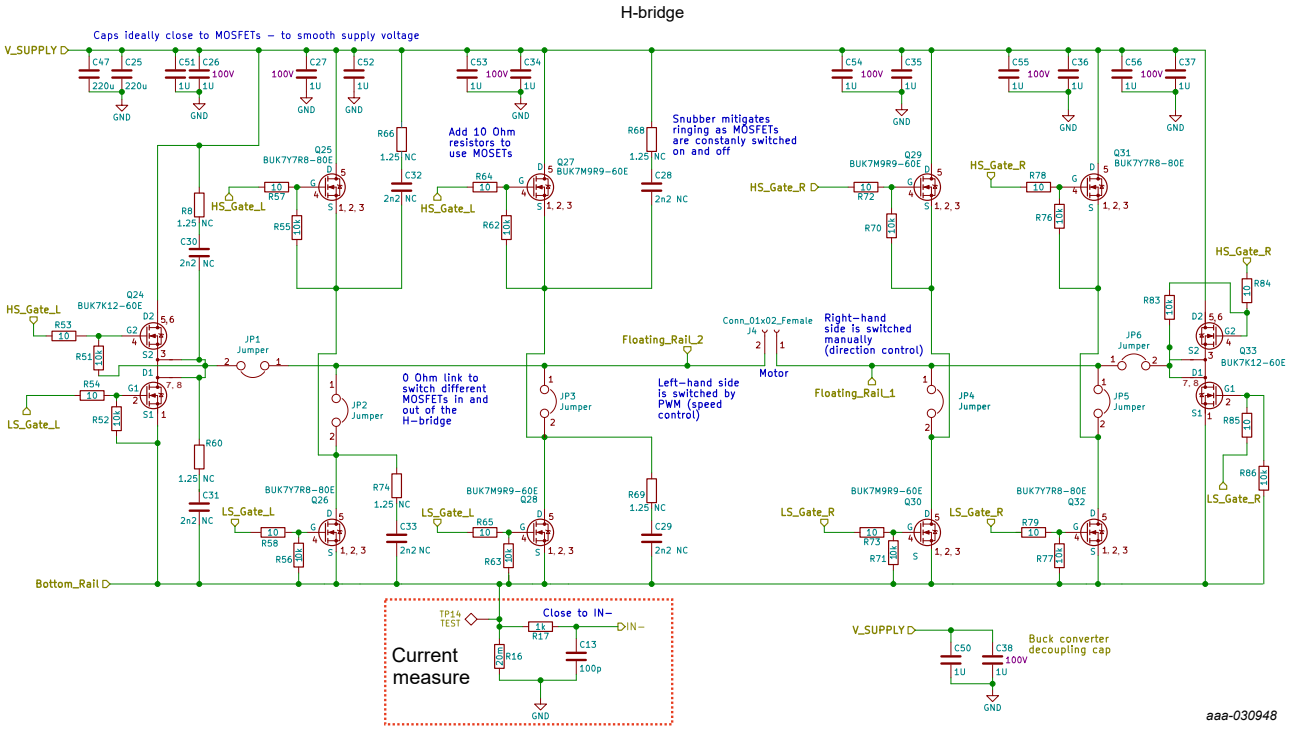


Fig. 20. H-bridge

Reservoir and decoupling capacitors

Decoupling capacitor (1 µF) and reservoir capacitor (220 µF) are used to filter the “V_SUPPLY”.

Snubber on the left MOSFETs (switching MOSFETs)

RC Snubber footprint are implemented on the switching MOSFETs.

An additional RC snubber may be added to further reduce ringing, application note *AN11160* gives an explanation about snubber calculation.

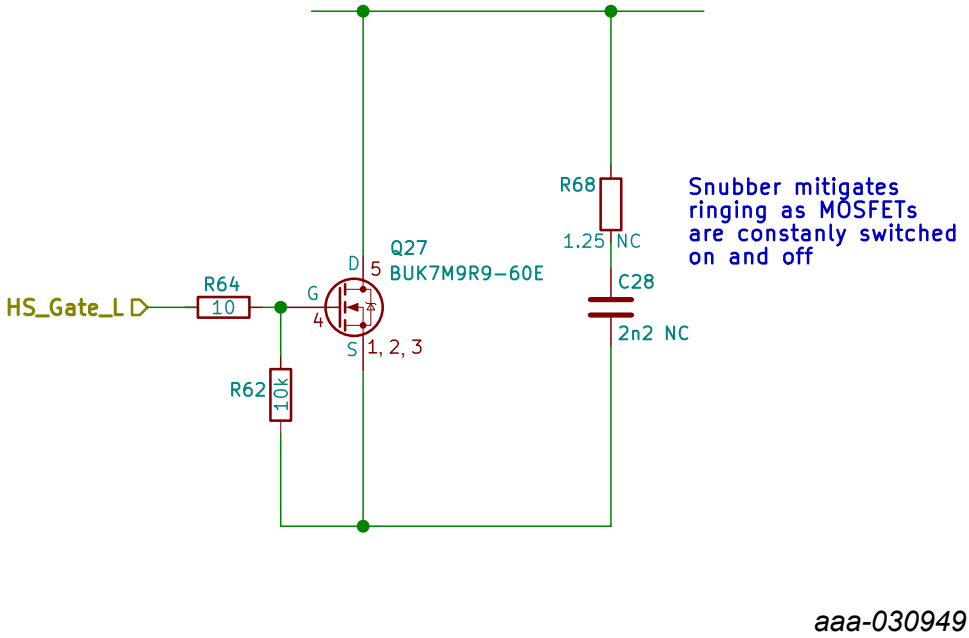


Fig. 21. Snubber circuit

Jumper to connect the required MOSFETs

Each MOSFET package is selected by soldering the following jumpers:

- LFPAK33: JP3, JP4
- LFPAK56D: JP1, JP6
- LFPAK56: JP2, JP5

Note: Solder only the jumpers needed to avoid incorrect operation!

Gate drive resistors

To avoid conflict between the switching MOSFETs gate resistors should be desoldered for those MOSFETs not in use.

Adjust the value of the gate resistor to reduce ringing or modify the switching time.

A resistor between gate and source of each MOSFET keeps the MOSFET off when there is no gate voltage applied.

Low side current measurement

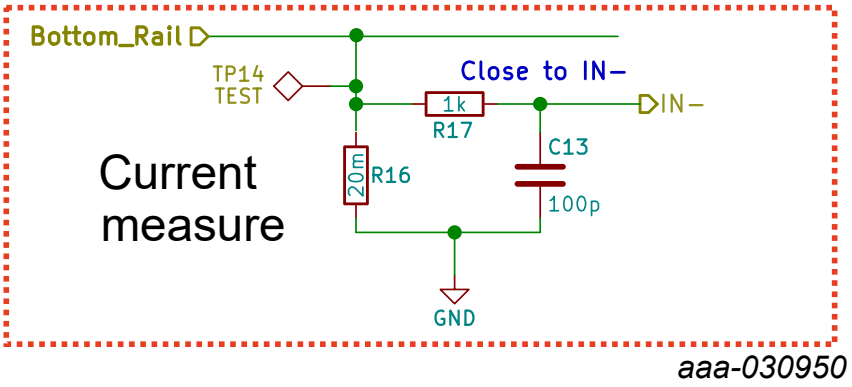


Fig. 22. Current measurement

A shunt resistor R16 (20 mΩ) measures the current in the H-bridge and provide a voltage proportional to the current to the over current protection input ”IN-“. A low pass filter R17, C13 filters the signal to avoid false triggering of the current limit circuit due to the noise spike.

3.6. Overcurrent detection

Overcurrent in the motor drive MOSFETs is prevented by comparing the current sense voltage with a reference voltage. In the case of overcurrent the PWM function is reset. The PWM function will be reactivated if the fault disappears.

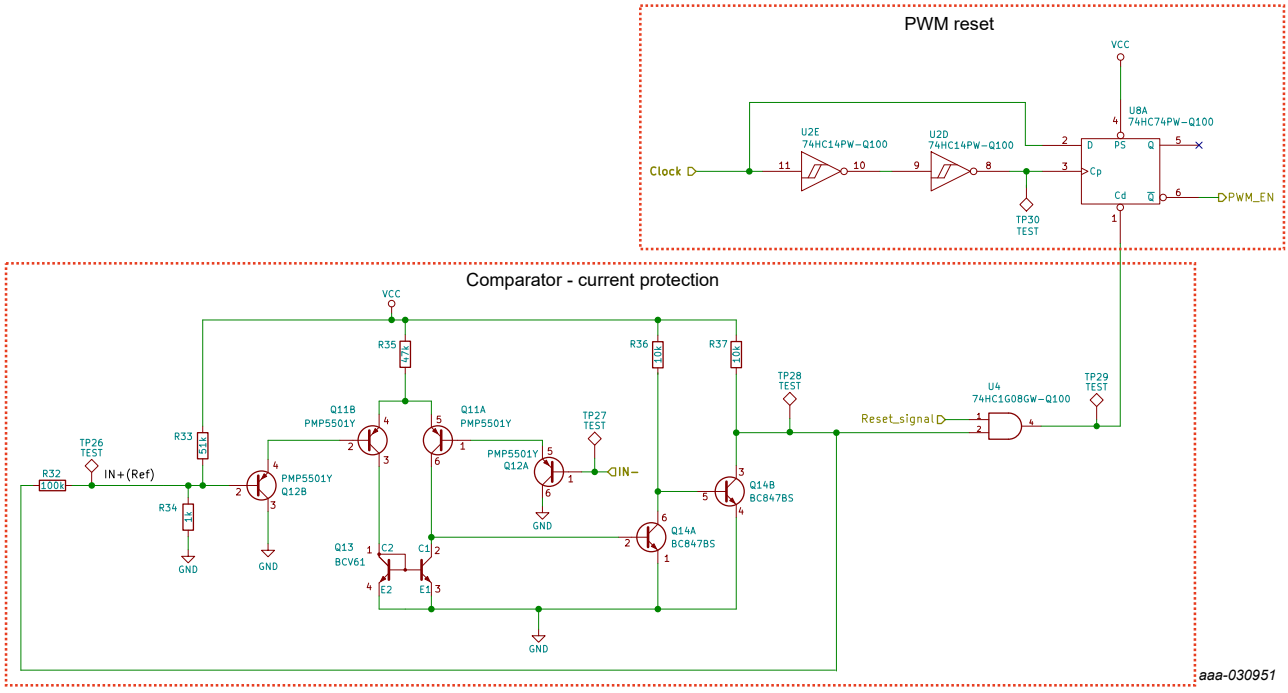


Fig. 23. Overcurrent detection

Comparator, with voltage reference setting current limit

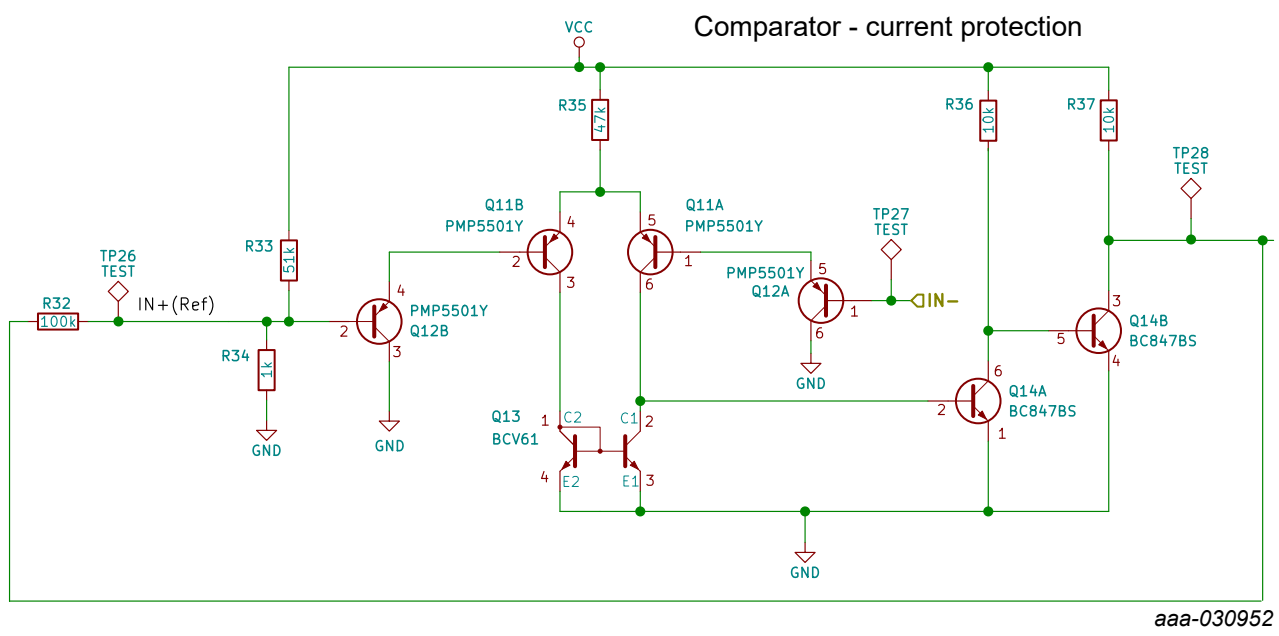


Fig. 24. Comparator, with voltage reference

"IN+" is the maximum current setting input. "IN-" is the current measurement input reference.

R35 is a rudimentary current source for the comparator circuit.

Q13 (BCV61) is a current mirror, this means that the polarisation current from R35 is shared equally between the two current paths.

Q11 and Q12 (PMP5501Y) are configured as Darlington pairs to increase the gain to improve the sensitivity of the comparator.

Q11 is a differential pair.

- When IN+ > IN- the output (TP28) is high (no overcurrent)
- When IN+ < IN- the output (TP28) is low (overcurrent)

R33 and R34 set the current limitation, R32 adds hysteresis to avoid transitions due to the noise.

PWM reset

The PWM reset function reactivating the PWM circuit if fault disappears.

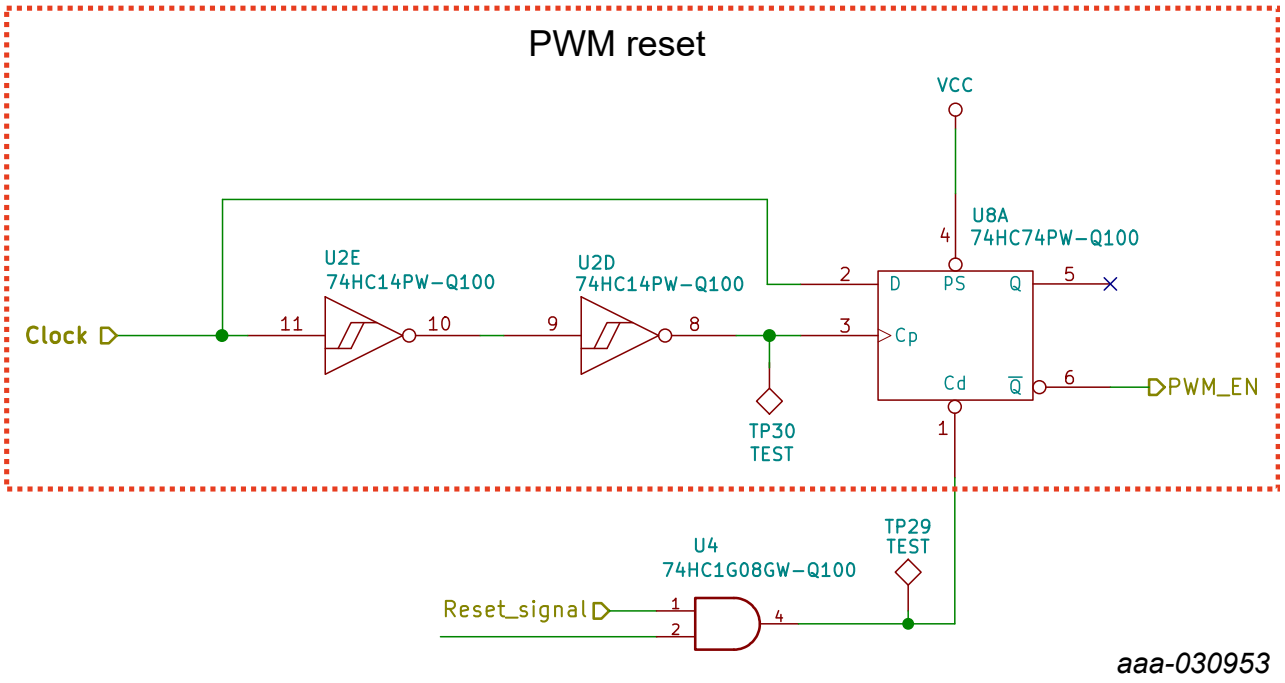


Fig. 25. PWM reset

When there is no overcurrent TP28 is high. “Reset_signal” is high since the V_{CC} (5 V) is supplying the circuit. The output of AND gate U4 (74HC1G08) is high.

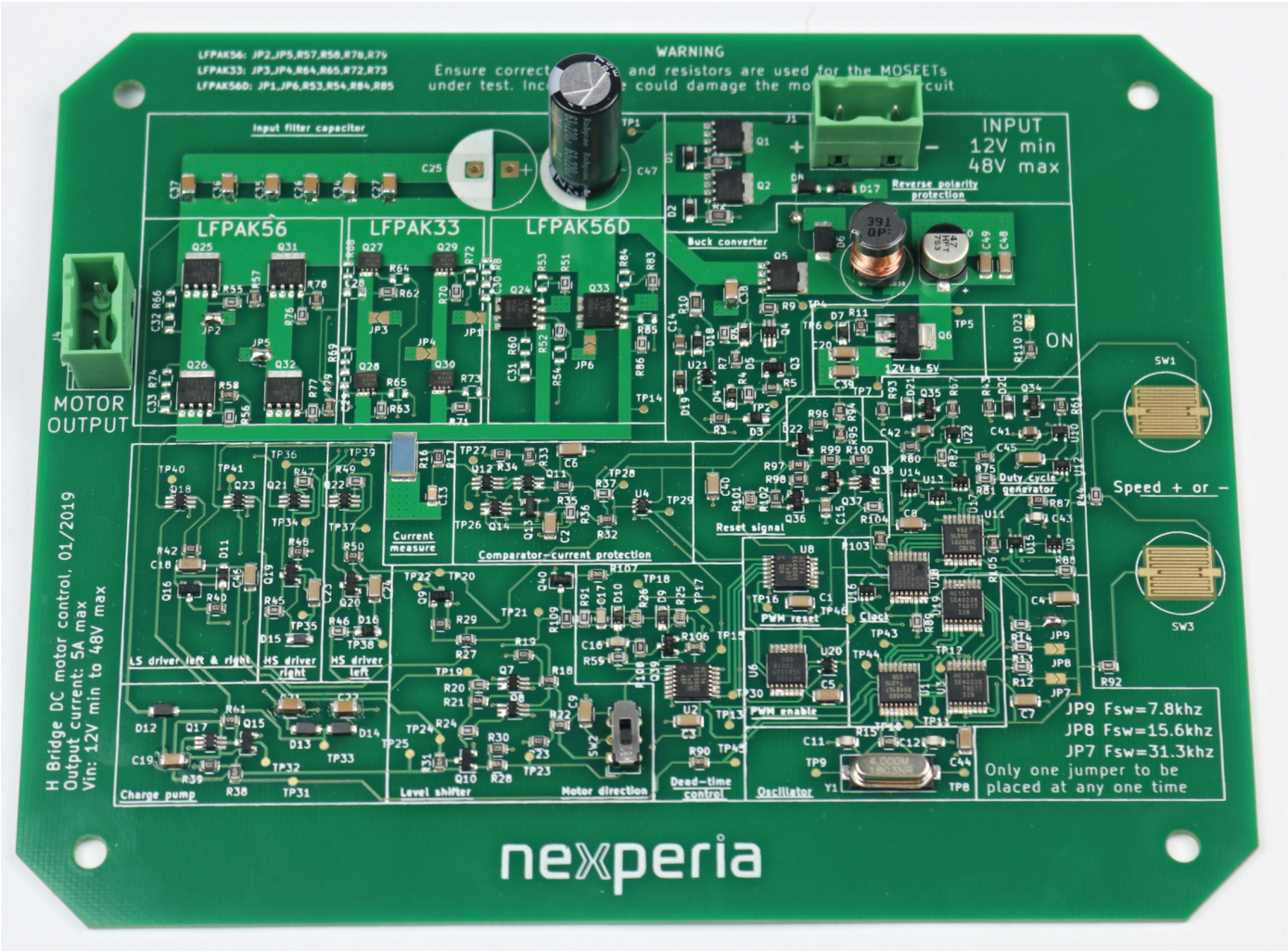
The signal “Clock” makes “PWM_EN” output from U8 (74HC74) switch to 0 at the first rising edge and stay at 0. U2 (74HC14) create a delay to have D input high before the rising edge on Cp).

If an overcurrent is detected by the comparator TP28 will switch to 0, TP29 will also switch to 0. Instantaneously “PWM_EN” will switch to 1 and force the duty cycle to be 0 (see section Dead-time function).

When the overcurrent disappears, TP28 and TP29 switch back to 1 and the next rising edge of “Clock” makes “PWM_EN” switch to 0 and the duty cycle is re-enabled.

This allows a cycle by cycle current limit behaviour from the circuit.

4. PCB top view



note: gate resistors R57,R58, R78, R79 and jumpers JP2, JP5 are fitted, selecting the MOSFETs in LFPAK56 package

Fig. 26. H-bridge motor controller PCB top-view

5. Schematics

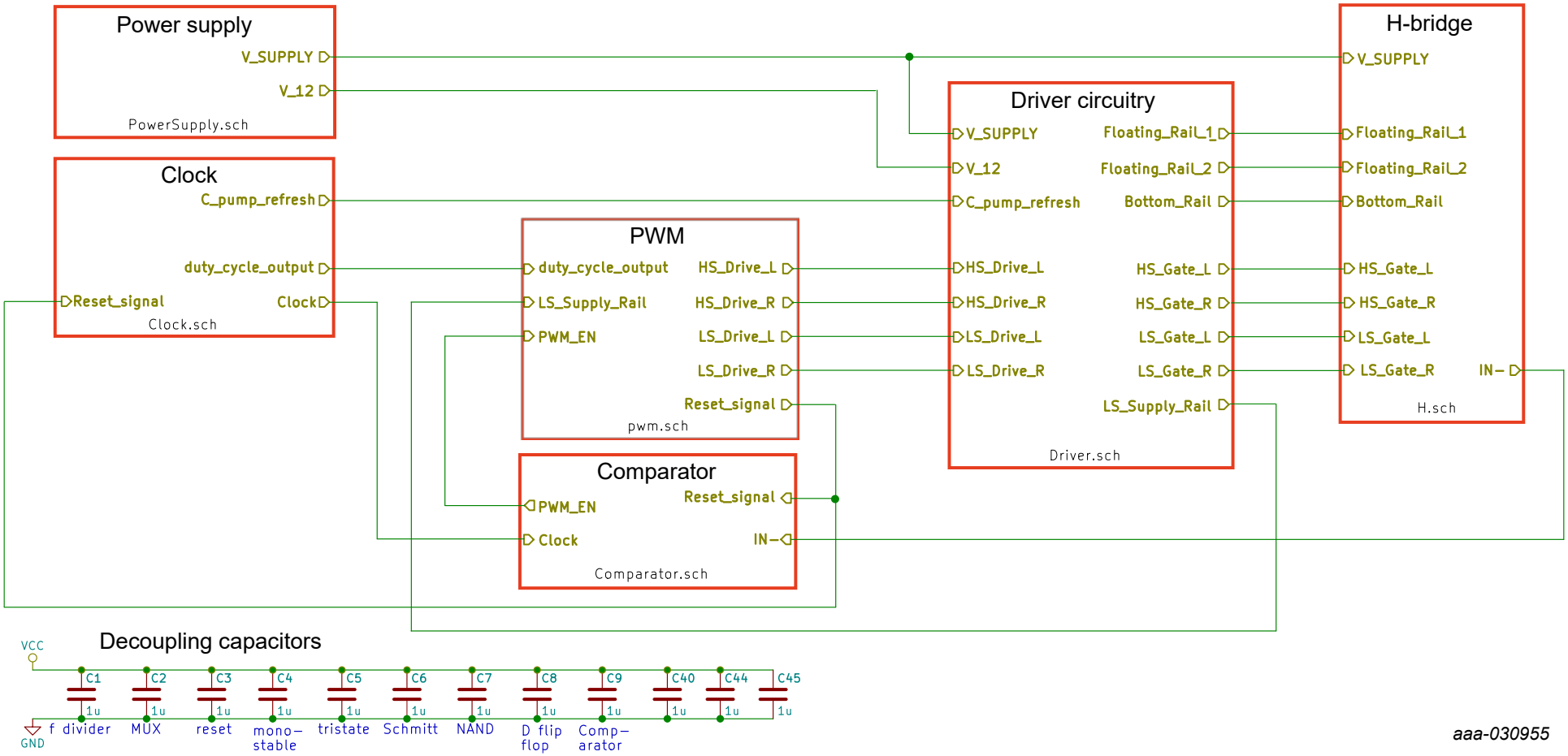


Fig. 27. Schematics overview

5.1. Power supply

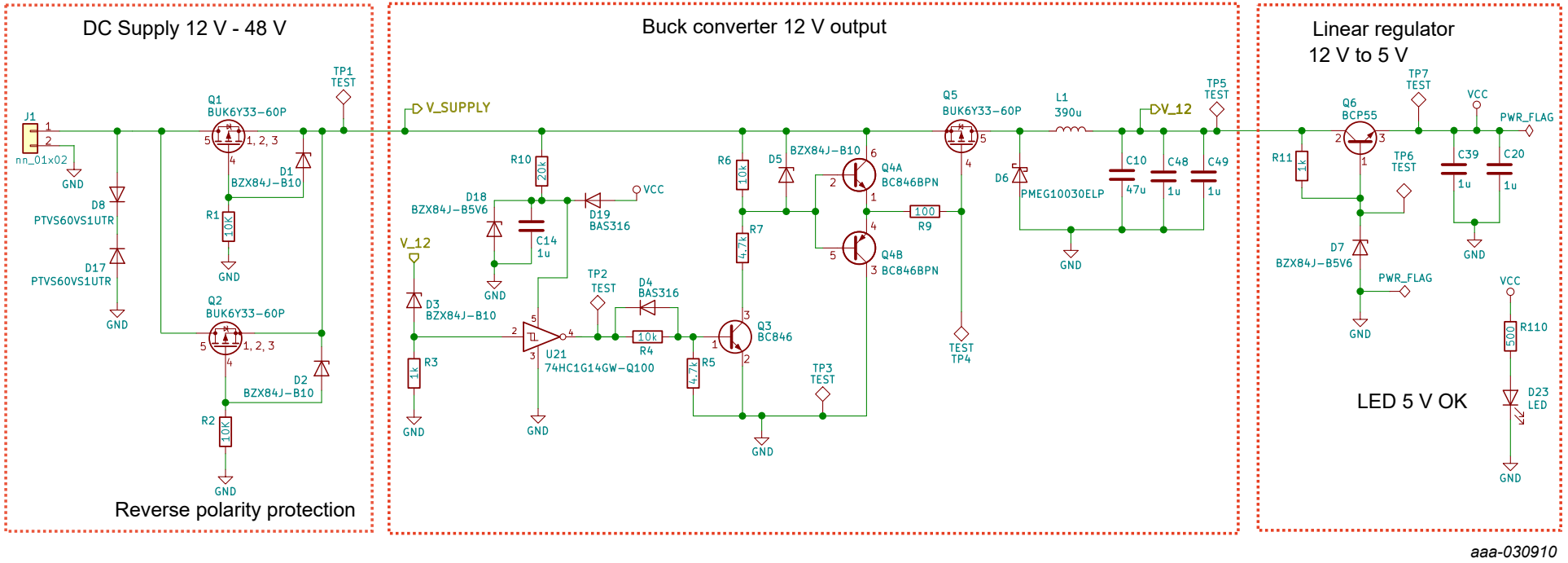


Fig. 28. Power supply schematic

5.2. Clock

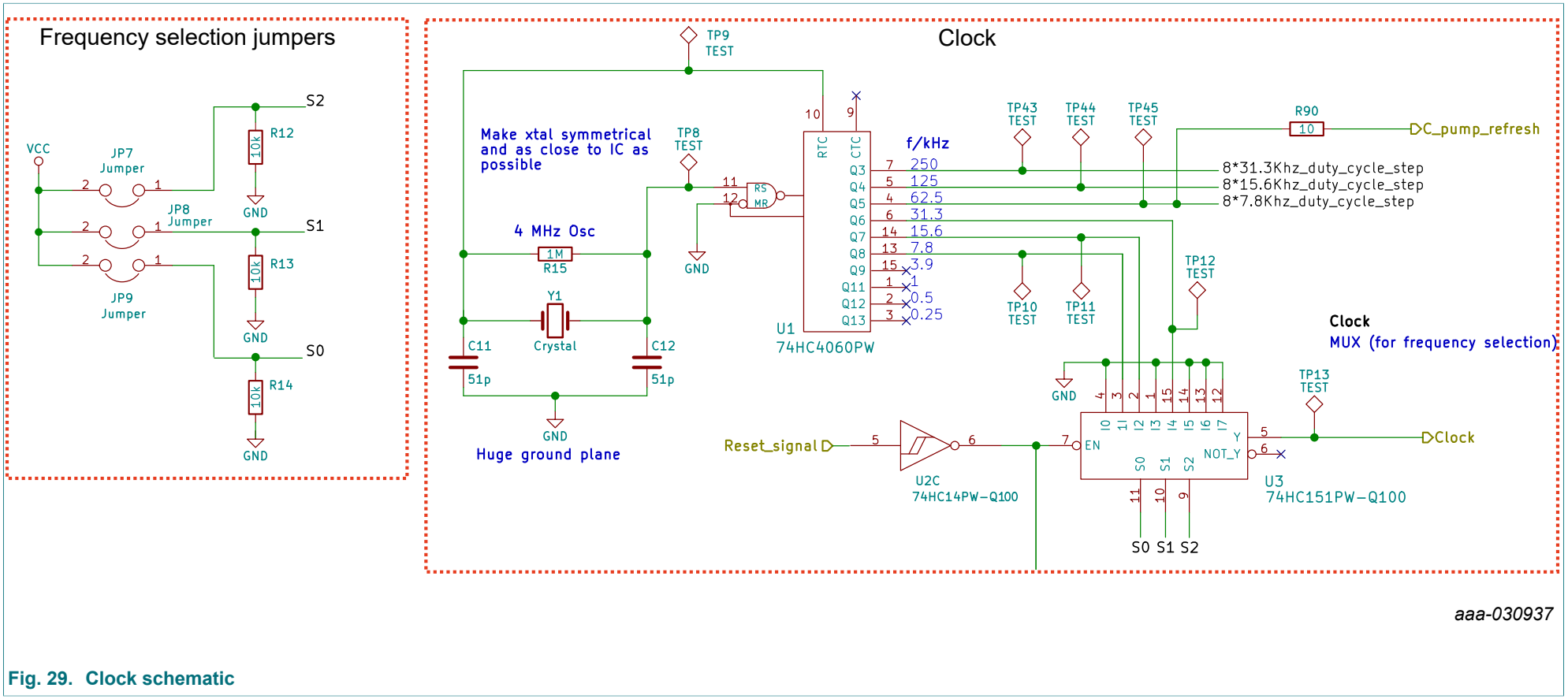


Fig. 29. Clock schematic

5.3. Duty cycle

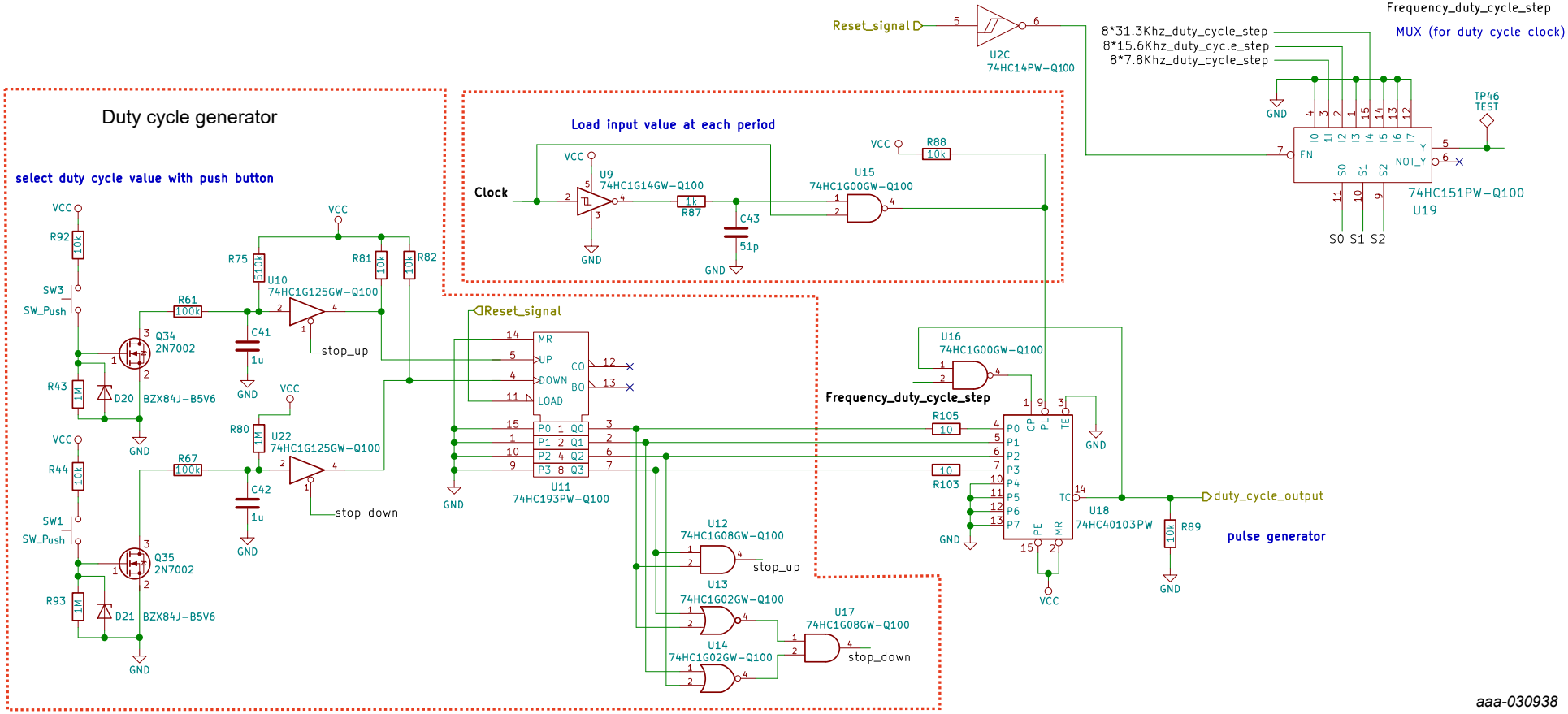


Fig. 30. Duty cycle schematic

5.4. PWM

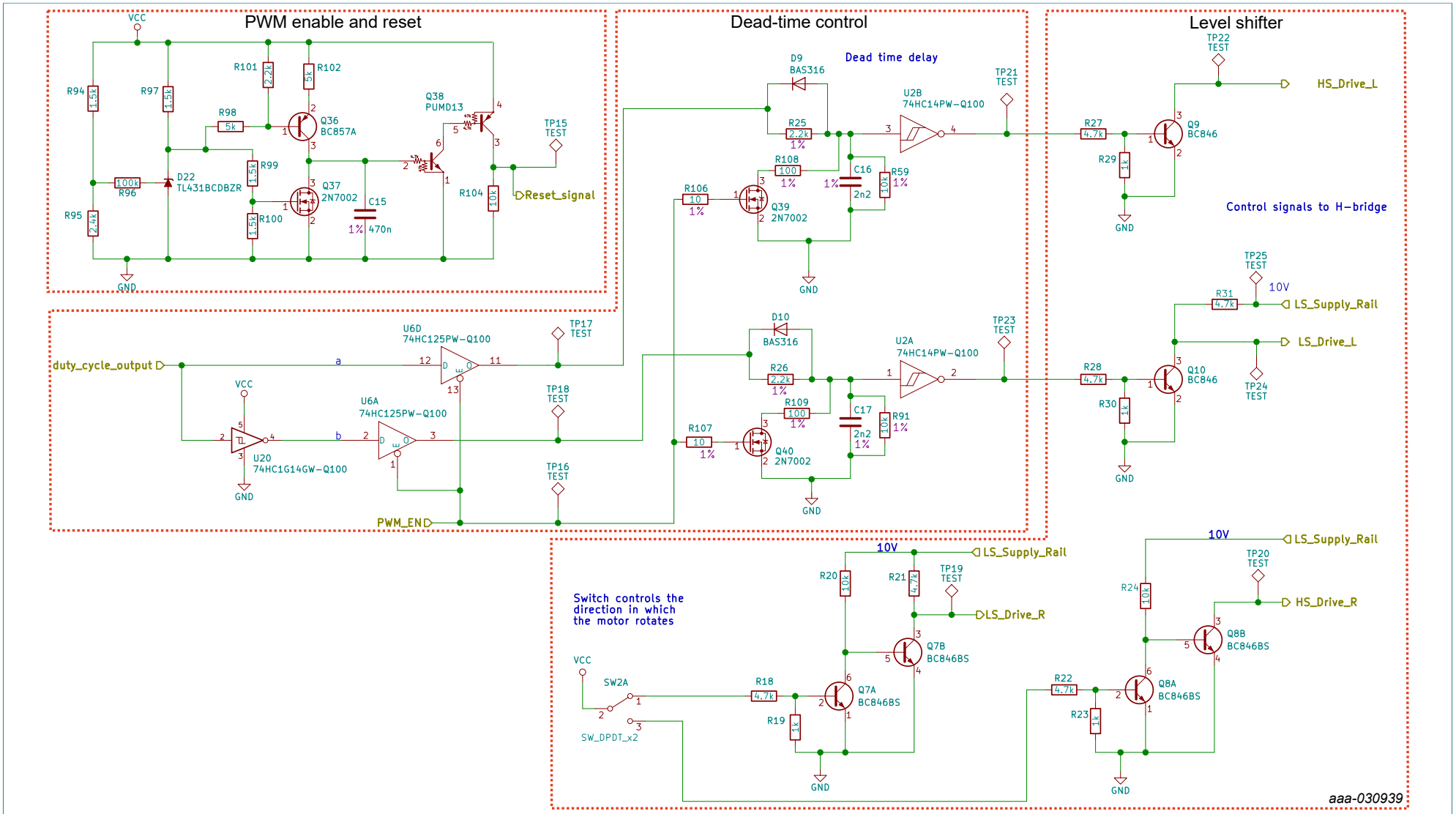


Fig. 31. PWM schematic

5.5. Overcurrent detection

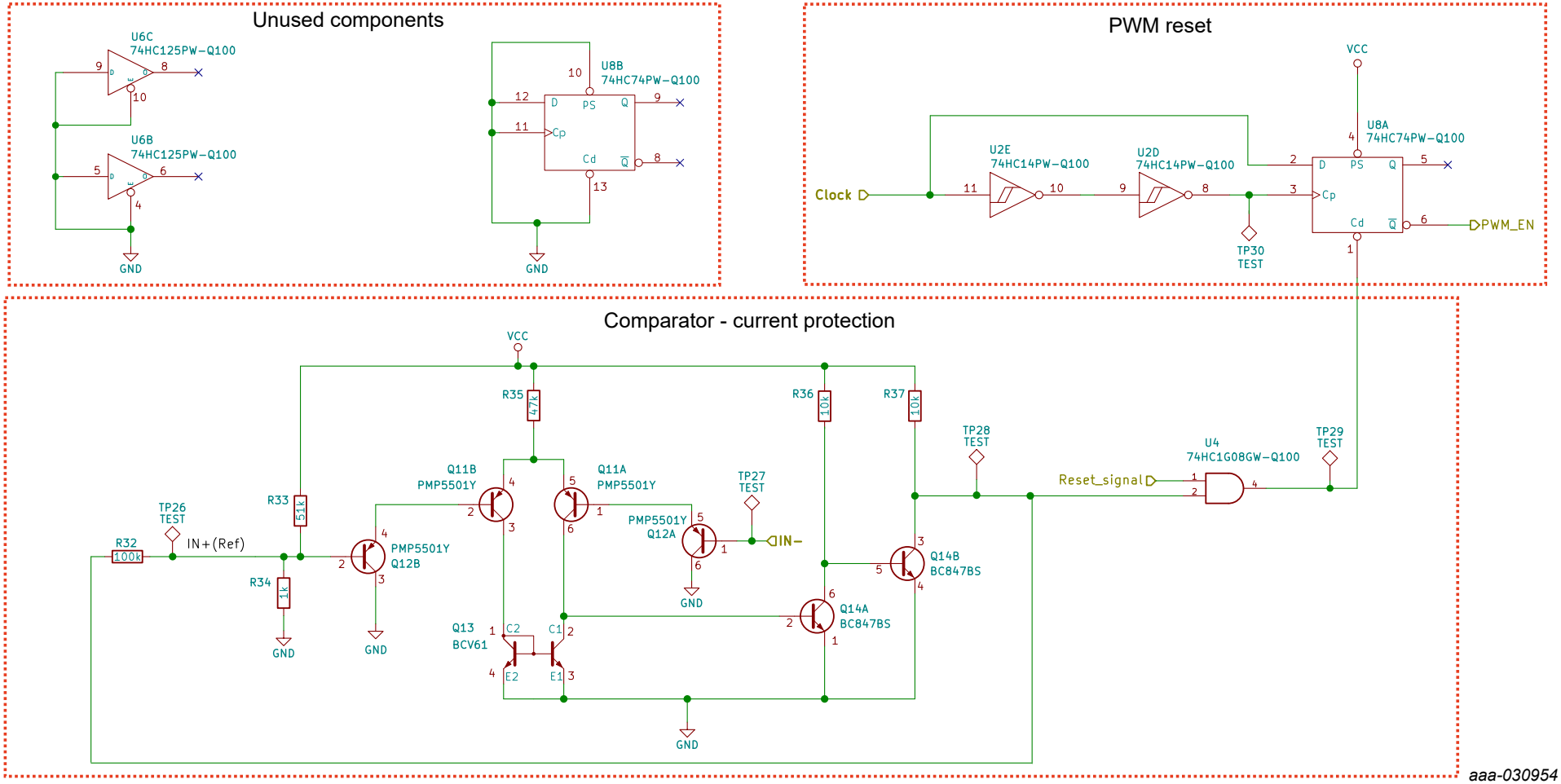


Fig. 32. Overcurrent detection schematic

5.6. H-bridge

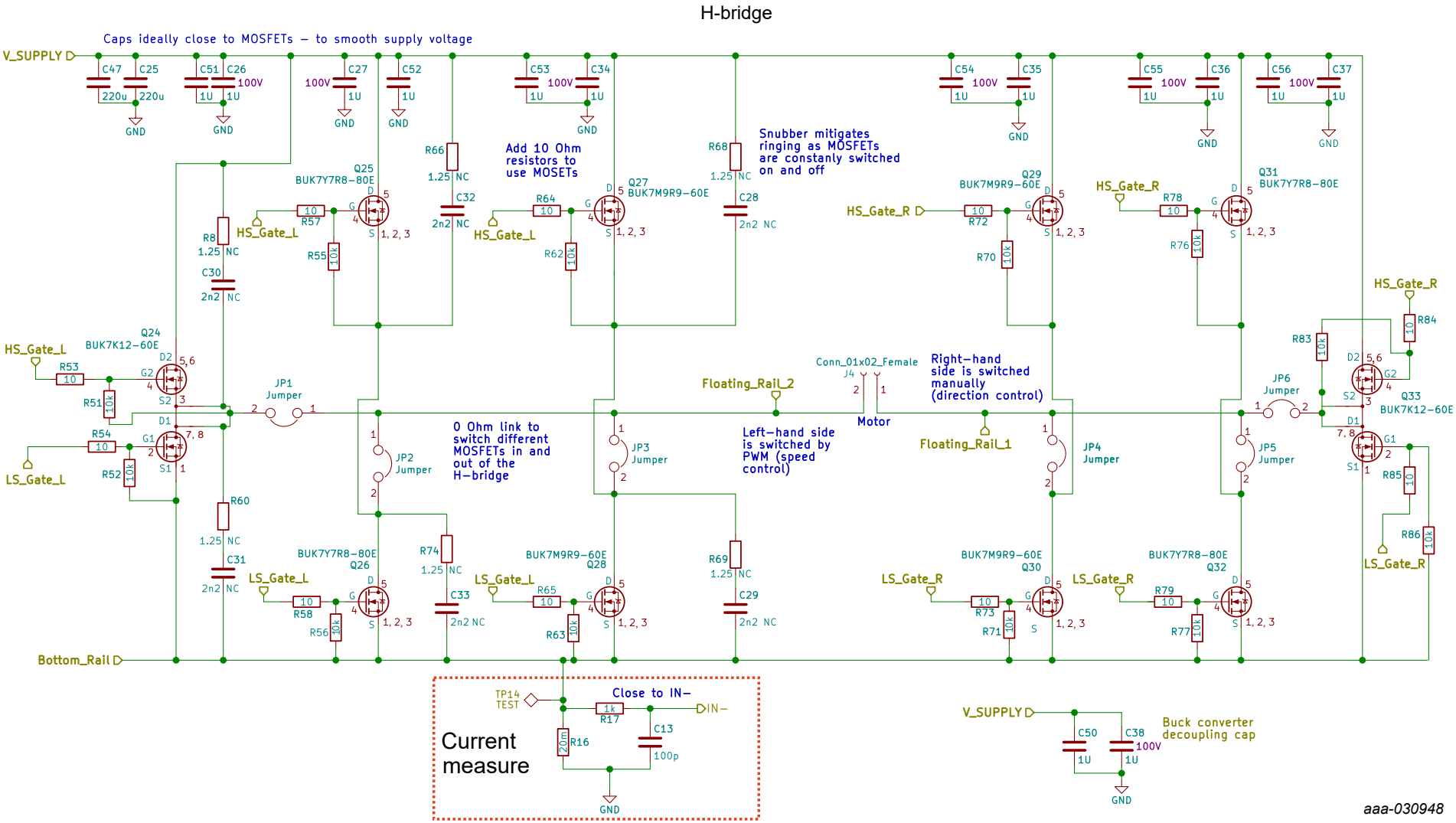


Fig. 33. H-bridge schematic

5.7. Driver circuit

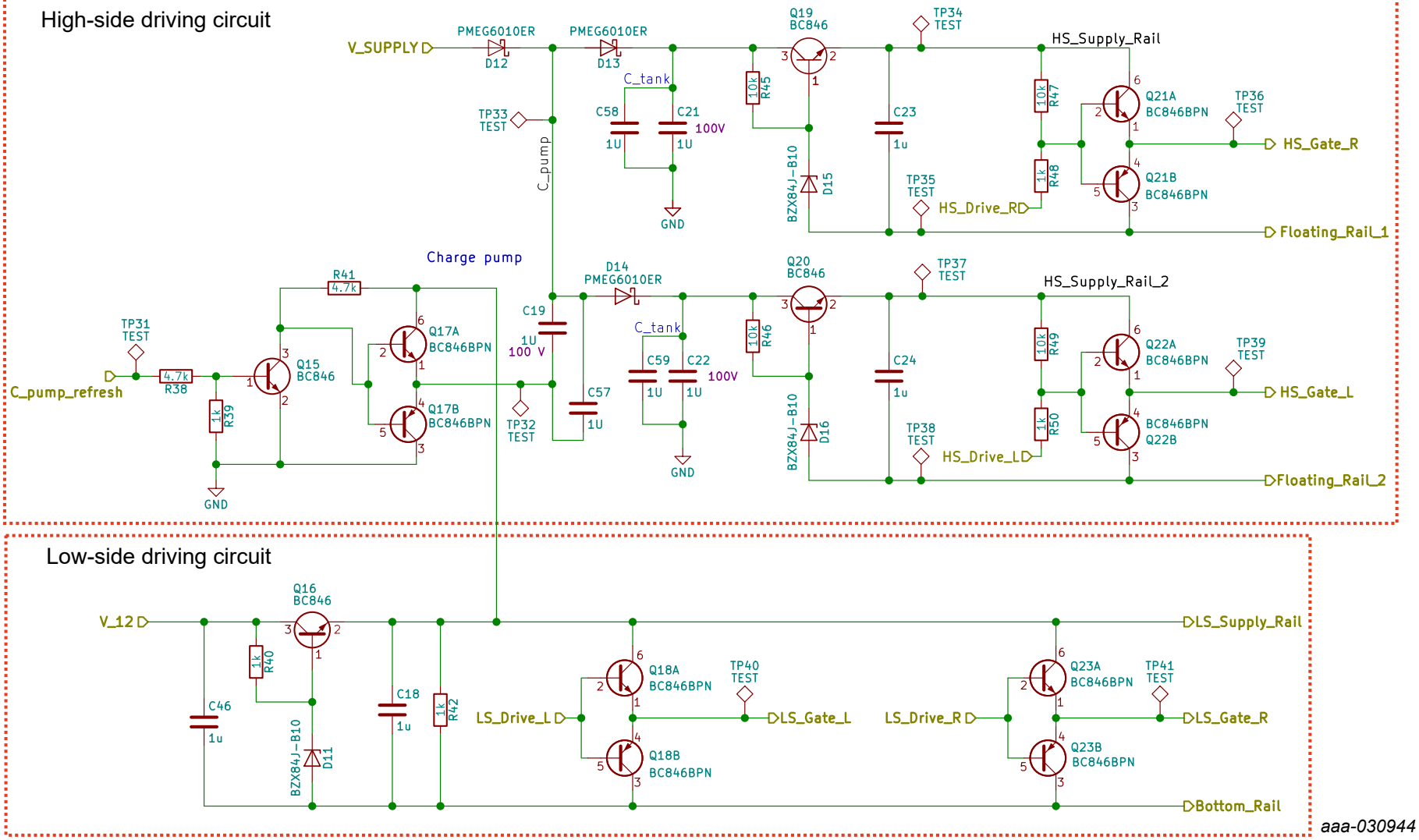


Fig. 34. Driver stage schematic

6. Bill of materials (Nexperia parts)

Table 2. BOM (Nexperia parts)

Reference	Part number	Description
D1, D2, D3, D5, D11, D15, D16	BZX84J-B10	Single Zener diode 10 V
D4, D9, D10, D19	BAS316	High-speed switching diodes
D6	PMEG10030ELP	100 V, 3 A low leakage current Schottky barrier rectifier
D7, D18, D20, D21	BZX84J-B5V6	Single Zener diodes 5.6 V
D8, D17	PTVS60VS1UTR	High-temperature 400 W Transient Voltage Suppressor
D12, D13, D14	PMEG6010ER	1 A low VF MEGA Schottky barrier rectifier
D22	TL431BCDBZR	Adjustable precision shunt regulator
Q1, Q2, Q5	BUK6Y33-60P	P-channel MOSFET in an LFPAK56 (Power SO8) package 60 V, 33 mΩ
Q3, Q9, Q10, Q15, Q16, Q19, Q20	BC846	65 V, 100 mA NPN general-purpose transistors
Q4, Q17, Q18, Q21, Q22, Q23	BC846BPN	65 V, 100 mA NPN/PNP general-purpose transistor
Q6	BCP55	60 V, 1 A NPN medium power transistor
Q7, Q8	BC846BS	65 V, 100 mA NPN/NPN general-purpose transistor
Q11, Q12	PMP5501Y	PNP/PNP matched double transistors
Q13	BCV61	NPN general-purpose double transistors
Q14	BC847BS	45 V, 100 mA NPN/NPN general-purpose transistor
Q24, Q33	BUK7K12-60E	LFPAK56D, dual N-channel MOSFET
Q25, Q26, Q31, Q32	BUK7Y7R8-80E	LFPAK56, N channel MOSFET, 80 V, 7.8 mΩ
Q27, Q28, Q29, Q30	BUK7M9R9-60E	LFPAK33, N channel MOSFET
Q34, Q35, Q37, Q39, Q40	2N7002	60 V, 300 mA N-channel Trench MOSFET
Q36	BC857A	PNP general purpose transistors
Q38	PUMD13	NPN/PNP resistor-equipped transistors; R1 = 4.7 kΩ, R2 = 47 kΩ
U1	74HC4060PW	14-stage binary ripple counter with oscillator
U2	74HC14PW-Q100	Hex inverting Schmitt trigger
U3, U19	74HC151PW-Q100	8-input multiplexer
U4, U12, U17	74HC1G08GW-Q100	2-input AND gate
U6	74HC125PW-Q100	Quad buffer/line driver; 3-state
U8	74HC74PW-Q100	Dual D-type flip-flop with set and reset; positive-edge trigger
U9, U20, U21	74HC1G14GW-Q100	Inverting Schmitt trigger
U10, U22	74HC1G125GW-Q100	Bus buffer/line driver; 3-state
U11	74HC193PW-Q100	Presettable synchronous 4-bit binary up, down counter
U13, U14	74HC1G02GW-Q100	2-input NOR gate
U15, U16	74HC1G00GW-Q100	2-input NAND gate
U18	74HC40103PW	8-bit synchronous binary down counter

7. Bill of materials

Table 3. BOM

Item	Qty	Reference	Value	Footprint	Voltage
1	20	C1, C2, C3, C4, C5, C6, C7, C8, C9, C18, C20, C23, C24, C39, C40, C44, C45, C46, C48, C49	1 µF	Capacitors_SMD: C_1206	
2	1	C10	47 µF	Capacitors_SMD: CP_Elec 6.3 x 5.7	
3	3	C11, C12, C43	51 pF	Capacitors_SMD: C_0805	
4	1	C13	100 pF	Capacitors_SMD: C_0805	
5	3	C14, C41, C42	1 µF	Capacitors_SMD: C_0805	
6	1	C15	470 nF	Capacitors_SMD:C_0805	
7	2	C16, C17	2.2 nF	Capacitors_SMD:C_0805	
8	10	C19, C21, C22, C26, C27, C34, C35, C36, C37, C38	1 µF	Capacitors_SMD:C_1206	100 V
9	2	C25, C47	220 µF	Capacitors_THT: CP_Radial_D 12.5 mm P 5.00 mm	100 V
10	6	C28, C29, C30, C31, C32, C33	* user selected	Capacitors_SMD: C_0805	
11	10	C50, C51, C52, C53, C54, C55, C56, C57, C58, C59	1 µF	Capacitors_SMD: C_0805	100 V
12	7	D1, D2, D3, D5, D11, D15, D16	BZX84J-B10	Diodes_SMD: D_SOD-323 HandSoldering	
13	4	D4, D9, D10, D19	BAS316	Diodes_SMD: D_SOD-323 HandSoldering	
14	1	D6	PMEG10030ELP	Nexperia: SOD128	
15	4	D7, D18, D20, D21	BZX84J-B5V6	Diodes_SMD: D_SOD-323 HandSoldering	
16	2	D8, D17	PTVS60VS1UTR	Nexperia: D_SOD123W	
17	3	D12, D13, D14	PMEG6010ER	Nexperia: D_SOD123W	
18	1	D22	TL431BCDBZR	TO_SOT_Packages_SMD: SOT-23	
19	1	D23	LED	LEDs: LED_0603	
20	1	J1	Conn_01x02	Connectors Phoenix: PhoenixContact_GMSTBVA-G_ 02 x 7.50 mm Vertical	
21	1	J4	Conn_01x02_Female	Connectors Phoenix:PhoenixContact_GMSTBVA-G 02 x 7.50 mm Vertical	
22	9	JP1, JP2, JP3, JP4, JP5, JP6, JP7, JP8, JP9	Jumper	Jumpers: SolderJumper-2_P 1.3 mm Open_TrianglePad 1.0 x 1.5 mm	
23	1	L1	390 µH	Inductors_THT: L_Radial_D 10.0 mm P 5.00 mm Fastron_07M	
24	4	MK1, MK2, MK3, MK4	Mounting_Hole	Mounting_Holes:MountingHole 4.3 mm M4	
25	3	Q1, Q2, Q5	BUK6Y33-60P	TO_SOT_Packages_SMD: SOT-669_LFPAK	
26	7	Q3, Q9, Q10, Q15, Q16, Q19, Q20	BC846	TO_SOT_Packages_SMD: SOT-23	

Item	Qty	Reference	Value	Footprint	Voltage
27	6	Q4, Q17, Q18, Q21, Q22, Q23	BC846BPN	TO_SOT_Packages_SMD: SOT-363_SC-70-6 Handsoldering	
28	1	Q6	BCP55	TO_SOT_Packages_SMD: SOT-223 3Lead TabPin2	
29	2	Q7, Q8	BC846BS	TO_SOT_Packages_SMD: SOT-363_SC-70-6 Handsoldering	
30	2	Q11, Q12	PMP5501Y	TO_SOT_Packages_SMD: SOT-363_SC-70-6 Handsoldering	
31	1	Q13	BCV61	Nexperia: SOT-143B	
32	1	Q14	BC847BS	TO_SOT_Packages_SMD: SOT-363_SC-70-6 Handsoldering	
33	2	Q24, Q33	BUK7K12-60E	Nexperia: LFPAK56D	
34	4	Q25, Q26, Q31, Q32	BUK7Y7R8-80E	TO_SOT_Packages_SMD: SOT-669_LFPAK	
35	4	Q27, Q28, Q29, Q30	BUK7M9R9-60E	Nexperia: LFPAK33	
36	5	Q34, Q35, Q37, Q39, Q40	2N7002	TO_SOT_Packages_SMD: SOT-23	
37	1	Q36	BC857A	TO_SOT_Packages_SMD: SOT-23	
38	1	Q38	PUMD13	TO_SOT_Packages_SMD: SOT-363 SC-70-6 Handsoldering	
39	2	R1, R2	10 kΩ	Resistors_SMD: R_1206	
40	14	R3, R11, R17, R19, R23, R29, R30, R34, R39, R40, R42, R48, R50, R87	1 kΩ	Resistors_SMD: R_0805	
41	34	R4, R6, R12, R13, R14, R20, R24, R36, R37, R44, R45, R46, R47, R49, R51, R52, R55, R56, R59, R62, R63, R70, R71, R76, R77, R81, R82, R83, R86, R88, R89, R91, R92, R104	10 kΩ	Resistors_SMD: R_0805	
42	10	R5, R7, R18, R21, R22, R27, R28, R31, R38, R41	4.7 kΩ	Resistors_SMD:R_0805	
43	6	R8, R60, R66, R68, R69, R74	* user selected	Resistors_SMD:R_0805	
44	3	R9, R108, R109	100 Ω	Resistors_SMD: R_0805	
45	1	R10	20 kΩ	Resistors_SMD: R_1206	
46	4	R15, R43, R80, R93	1 MΩ	Resistors_SMD: R_0805	
47	1	R16	20 mΩ	Resistors_SMD: R_2512	
48	3	R25, R26, R101	2.2 kΩ	Resistors_SMD: R_0805	
49	4	R32, R61, R67, R96	100 kΩ	Resistors_SMD: R_0805	
50	1	R33	51 kΩ	Resistors_SMD: R_0805	
51	1	R35	47 kΩ	Resistors_SMD: R_0805	
52	17	R53, R54, R57, R58, R64, R65, R72, R73, R78, R79, R84, R85, R90, R103, R105, R106, R107	10 Ω	Resistors_SMD: R_0805	

Item	Qty	Reference	Value	Footprint	Voltage
53	1	R75	510 kΩ	Resistors_SMD: R_0805	
54	4	R94, R97, R99, R100	1.5 kΩ	Resistors_SMD: R_0805	
55	1	R95	2.4 kΩ	Resistors_SMD: R_0805	
56	2	R98, R102	5 kΩ	Resistors_SMD: R_0805	
57	1	R110	500 Ω	Resistors_SMD: R_0805	
58	2	SW1, SW3	SW_Push	Buttons_Switches_SMD: SW_DIP_x1_W 8.61 mm_Slide_LowProfile	
59	1	SW2	SW_DPDT_x2	Buttons_Switches_THT: SW_CuK_JS202011CQN_DPDT_Straight	
60	1	U1	74HC4060PW	Housings_SSOP: TSSOP-16 4.4 x 5 mm Pitch 0.65 mm	
61	1	U2	74HC14PW-Q100	Housings_SSOP: TSSOP-14 4.4 x 5 mm_Pitch 0.65mm	
62	2	U3, U19	74HC151PW-Q100	Housings_SSOP: TSSOP-16 4.4 x 5 mm Pitch 0.65 mm	
63	3	U4, U12, U17	74HC1G08GW-Q100	TO_SOT_Packages_SMD: SOT-353_SC-70-5	
64	1	U6	74HC125PW-Q100	Housings_SSOP: TSSOP-14 4.4 x 5mm Pitch 0.65 mm	
65	1	U8	74HC74PW-Q100	Housings_SSOP: TSSOP-14 4.4 x 5 mm Pitch 0.65 mm	
66	3	U9, U20, U21	74HC1G14GW-Q100	TO_SOT_Packages_SMD: SOT-353_SC-70-5	
67	2	U10, U22	74HC1G125GW-Q100	TO_SOT_Packages_SMD: SOT-353_SC-70-5	
68	1	U11	74HC193PW-Q100	Housings_SSOP: TSSOP-16 4.4 x 5mm Pitch 0.65 mm	
69	2	U13, U14	74HC1G02GW-Q100	TO_SOT_Packages_SMD: SOT-353_SC-70-5	
70	2	U15, U16	74HC1G00GW-Q100	TO_SOT_Packages_SMD: SOT-353_SC-70-5	
71	1	U18	74HC40103PW	Housings_SSOP: TSSOP-16 4.4 x 5 mm Pitch 0.65 mm	
72	1	Y1	Crystal	Crystals: Crystal_SMD_HC49-SD	

8. Revision history

Table 4. Revision history

Revision number	Date	Description
3.0	20200214	Schematic diagrams, text and BOMs updated to latest type numbers for Q1,Q2 and Q5
2.0	20190422	Schematic diagrams updated to correct IC type numbers
1.0	20190215	Initial version of the document

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