Product Quality Quick Reference Information

Quality information for product types

Quality and reliability data provided by Nexperia is intended to be a non-binding estimate of product performance only. It does not imply that any performance levels reflected in such data can be met if the product is operated outside the conditions expressly stated in the latest published datasheet for a device or in your application.

Quick reference

Information	Content
Device type	PSMNR70-40YSN
Orderable part number (12NC)	934664044115
Package	SOT1023
Waferfab sites	Vanguard, Taiwan
Assembly sites	Nexperia, Phillipines
ESD HBM	2000V - 4000V (2)
ESD CDM	> 1000V

The ESD values shown are typical representative numbers from a sample of devices tested during qualification and not guaranteed. Measurements have been conducted in accordance with JS-001-2017.

Reliability qualification information

Stress	Conditions	Duration	Quantity	Rejects
Stress Pre and Post stress electrical test	T_{amb} = 25°C	N/A	All parts	See below
PC Preconditioning	JESD22-A113 Bake T_{amb} = 125°C Soak T_{amb} = 85°C, RH = 85% reflow	24 hours 168 hours 3 cycles	924	0
HTRB High temperature reverse bias	MIL-STD-750-1 T_j = T_j max, V_{DS} = 80% of rated Voltage M1039 Method A	1000 hours	231	0
HTGB High temperature gate bias	JESD22-A108 T_j = T_j max, V_{GS} = 20V(SL), 16V (LL)	1000 hours	231	0
TC Temperature Cycling	JESD22-A104 -55°C to 150°C	500 cycles	231	0
UHAST Unbiased highly accelerated stress test	JESD22-A118 T_{amb} = 130°C, RH = 85% Pressure = +2.27atm	96 hours	231	0
HAST* Highly accelerated stress test	JESD22-A110 T_{amb} = 130°C, RH = 85% V_{DS} = 80% of rated voltage	96 hours	231	0
H3TRB* Temperature Humidity bias	JESD22-A101 T_{amb} = 85°C, RH = 85% V_{DS} = 80% of rated voltage	1000 hours		
IOL Intermittent operating life	MIL-STD-750 method 1037 ΔTj = 80°C	5000 cycles	231	0
RSH Resistance to solder heat	JESD22-A111 (SMD) 260°C ± 5°C	10s	30	0
SD Solderability	IPC/ECA J-STD-002 Method A dip and look No aging, solder Ta = 245°C	3 sec dip	66	0
	IPC/ECA J-STD-002 Method B dip and look No aging Solder Ta = 245°C >95% lead coverage required Steam Aging: condition C Steam Ta = 93°C, 8 hours Solder Ta = 245°C, 3 sec dip	8 hours 3 sec dip	66	0
	Dry Bake:	16 hours	66	0

*Either HAST or HT3RB are tested for a set of devices.

Calculation of FIT and MTBF

Test considered for FIT calculation: High Temperature Reverse Bias (HTRB) and High temperature Gate Bias (HTGB). Confidence level 60%, derated to 55°C, activation energy 0.7eV test time 168 to 1000 hours.

Technology	Quantity	Failure rate	MTBF
T15	462	2.61	3.83E+08