

Reliability Results for Product Type PMV65XPEA

Time period: Q4/2015 to Q3/2016

Test Results

AEC-Q101 Test	Conditions	Duration	Quantity	Rejects
TEST				
# 1 Pre- and Post-Stress Electrical Test	$T_{amb} = 25\text{ °C}$	N/A	all parts	see below
# 2 PC Preconditioning	JESD22-A113 Bake $T_{amb} = 125\text{ °C}$ Soak $T_{amb} = 85\text{ °C}$, RH = 85% Reflow soldering	24 hours 168 hours 3 cycles	55200	0
# 5 HTRB High Temperature Reverse Bias	MIL-STD-750-1 M1038 Method A $T_j = T_{jmax}$, $V_r = 100\%$ of max. datasheet reverse voltage	1000 hours	4154	0
# 6 HTGB High Temperature Gate Bias	JESD22-A108 $T_j = T_{jmax}$, gate biased at 100% of max. gate voltage rating	1000 hours	14240	0
# 7 TC Temperature Cycling	JESD22-A104 -55 °C to T_{jmax} , not to exceed 150°C	1000 cycles	12560	0
# 8 AC Autoclave	JESD22-A102 $T_{amb} = 121\text{ °C}$, RH = 100 % Pressure = 205 kPa (29.7 psia)	96 hours	13120	0
# 9 H3TRB High Humidity High Temperature Reverse Bias	JESD22-A101 $T_{amb} = 85\text{ °C}$, RH = 85%, $V_R > 80\%$ of rated reverse voltage	1000 hours	14240	0
# 10 IOL Intermittent Operating Life	MIL-STD-750 Method 1037 $t_{on} = t_{off}$, devices powered to insure $\Delta T_j = 125\text{ °C}$ for 7500 cycles or $\Delta T_j = 100\text{ °C}$ for 15000 cycles	1000 hours	14240	0
# 20 RSH Resistance to Solder Heat	JESD22-A111 260 °C \pm 5 °C	10 s	4710	0
# 21 SD Solderability	J-STD-002 Test method B and D		720	0

Calculation of FIT and MTBF

Test considered for FIT calculation: High Temperature Reverse Bias (HTRB, AEC-Q101 Test # 5)
Confidence level 60%, derated to 55 °C, activation energy 0.7 eV, test time 168 to 1000 hours

Wafer Fab	Technology	Quantity	Rejects	Failure Rate	MTBF
Mosel Vitelic	ssMOS	4154	0	1.02 FIT	111589 years