

## Quarterly Reliability Monitoring Results

Quarters: Q1/2023 to Q4/2024

Based on structural similarity

Supplier		User Part Number				
Nexperia B.V.		PBSS4160PANS-Q				
Name of Laboratory		Part Description				
Assembly reliability labs		Nexperia DHAM MCD package Small Signal Bipolar Transistor				
Based on AEC-Q101 Test		Test Conditions	Duration	# Lots	# Quantity	# Rejects
# E1	<b>TEST</b> Pre- and Post-Stress Electrical Test	Tamb = 25 °C	N/A	see below	all parts	see below
# A1	<b>PC</b> Preconditioning	JESD22-A113 Bake Tamb = 125 °C Soak Tamb = 85 °C, RH = 85% Reflow soldering	24 hours 168 hours 3 cycles	448	17920	0
# B1	<b>HTRB</b> High Temperature Reverse Bias	MIL-STD-750-1 M1039 Method A Tj = Tjmax, Vr = 100% of max. datasheet reverse voltage	1000 hours	394	15760	0
# A4	<b>TC</b> Temperature Cycling	JESD22-A104 -65 °C to Tjmax, not to exceed 150°C	1000 cycles	112	4480	0
# A3 or	<b>UHAST</b> Unbiased HAST	JESD22-A118 Tamb = 130 °C, RH = 85 %	96 hours	112	4480	0
# A3 alt	<b>AC</b> Autoclave	JESD22-A102 Tamb = 121 °C, RH = 100 % Pressure = 205 kPa (29.7 psia)				
# A2 alt	<b>H3TRB</b> High Humidity High Temperature Reverse Bias	JESD22-A101 Tamb = 85 °C, RH = 85%, VR = 80 % of rated reverse voltage <sup>[1]</sup>	1000 hours	112	4480	0
# A5	<b>IOL</b> Intermittent Operating Life	MIL-STD-750 Method 1037 ton = toff, devices powered to insure ΔTj = 100 °C for 15000 cycles	1000 hours	112	4480	0
# C8	<b>RSH</b> Resistance to Solder Heat	JESD22-A111 260 °C ± 5 °C	10 s	n.a.	n.a.	n.a.
# C10	<b>SD</b> Solderability	J-STD-002		85	2550	0

[1] The maximum applied voltage is limited by test chamber set up and does not exceed 115V.

### Calculation of FIT and MTTF

Test considered for FIT calculation: High Temperature Reverse Bias (HTRB, Test #B1)

Confidence level 60%, derated to 55 °C, activation energy 0.7 eV, test time 168 to 1000 hours

Wafer Fab	Technology	Quantity	Rejects	Failure Rate (FIT)	MTTF (hrs)
Nexperia DHAM	Small Signal Bipolar Transistor	15760	0	0,27	3,71E+09

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