

## Reliability Monitoring Results

Quarters: Q1/2022 to Q4/2022

Based on structural similarity

Supplier		User Part Number				
Nexperia B.V.		74LVC74APW-Q100				
<b>Part Description:</b> Dual D-type flip-flop with set and reset; positive-edge trigger						
Function Family: LVC Process family: Sub micron Package family: TSSOP						
JESD47 Test	Test Conditions	Duration	# Lots	# Quantity	# Rejects	
# 1 <b>TEST</b> Pre- and Post-Stress Electrical Test	Tamb = 25 °C	N/A	see below	all parts	see below	
# 2 <b>PC</b> Preconditioning	JESD22-A113 MSL 1	N/A	1070	83683	0	
# 5a <b>HTOL EFR</b> High Temperature Operating Life Extrinsic	JESD22-A108 Tj = 150°C VCCMAX ≤ V ≤ 1.2*VCCMAX	48 hours or 168 hours	380	56512	0	
# 5b <b>HTOL IFR</b> High Temperature Operating Life Intrinsic	JESD22-A108 Tj = 150°C VCCMAX ≤ V ≤ 1.2*VCCMAX	≥500 hours	155	11552	0	
# 7 <b>TC</b> Temperature Cycling	JESD22-A104 -65 °C to 150°C	≥500 cycles	549	43127	0	
# 9 <b>uHAST / HAST</b> unbiased or biased High Accelerated Stress Test	JESD22-A101 Tamb = 130 °C, RH = 85%, V = VCCMAX	96 hours	521	40556	0	

### Calculation of PPM, FIT and MTTF

Test considered for PPM calculation: High Temperature Operating LifeTest Extrinsic (HTOL EFR, Test # 5a above)

Test considered for FIT and MTTF calculations: High Temperature Operating LifeTest Intrinsic (HTOL IFR, Test # 5b above)

Confidence level 60%, derated to 55 °C, activation energy 0.7 eV, test time 168 to 1000 hours

Product Family	Package Family	Quantity	Rejects	Extrinsic Failure Rate (PPM)	Intrinsic Failure Rate (FIT)	MTTF (hrs)
LVC	TSSOP	11552	0	17	0.4	2.77 E+09