

Voltage-translating Shift Register for Modular Designs

Ideal for multiple I/O voltages, 74LVC8T595 performs voltage-level translation using an 8-stage shift register and an 8-bit storage register with 3-state outputs. The device operates in the 1.1 to 5.5 V range, enabling newer low-voltage controllers to interface with legacy solutions. 74LVC8T595 is suitable for SIPO (serial-in/parallel-out) shift register implementations.

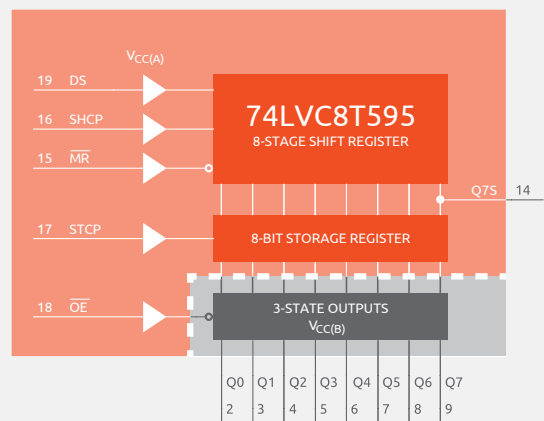


74LVC8T595 benefits from Nexperia's LVC family technology with I_{OFF} circuitry for partial power down-mode operation, which contributes to energy savings.

74LVC8T595's shift and storage register have separate clocks. Data is shifted on the positive edge of the SHCP input and data in the shift register is transferred to the storage register on a positive edge of the STCP input.

Part of our Standard Logic range, 74LVC8T595 is available in 20-pin TSSOP leaded and DQFN leadless packages. Both packages are specified for -40 °C to +125 °C and can be released in our Automotive (-Q100) portfolio.

Circuit Diagram



Technical details

$V_{CC(A)}$	$V_{CC(B)}$	Logic switching levels	Output Drive	Prop Delay (t_{pd})	Temperature Range	Static Current (I_{CC})
1.1-5.5 V	1.1-5.5V	CMOS/LVTTL	+/-24 mA	4.1 ns	-40 °C to +125 °C	0.01 μ A (typ.)

Key Features & benefits

- › Voltage level translation between nodes
1.2V, 1.5V, 1.8V, 2.5V, 3.3V and 5.0V
- › Over voltage tolerant inputs
- › I_{OFF} circuitry for partial power-down
- › Suspend mode
- › High noise immunity

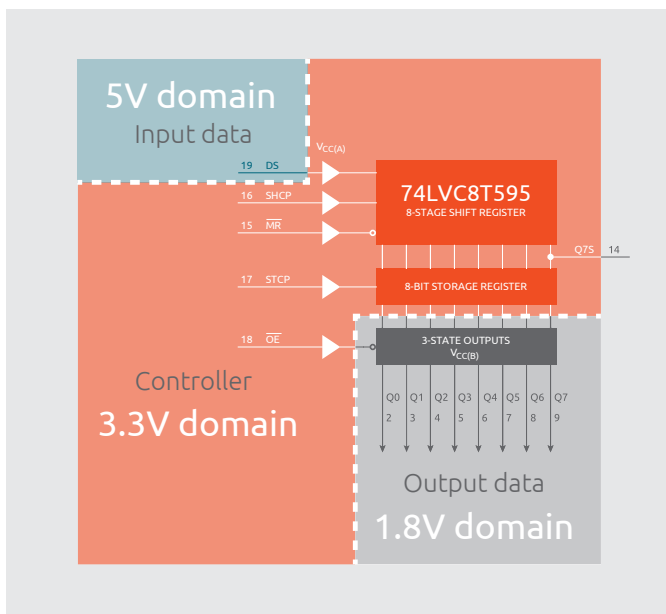
Over voltage tolerance

74LVC8T595 has over-voltage tolerant inputs, which do not have input clamp diodes and can be used to interface to higher-voltage systems without using external current-limiting resistors. This reduces BOM and cost. 74LVC8T595 is suitable for high-to-low level translation and can be used at 3.3 V with 5.5 V applied to the inputs.



74LVC8T595 allows the creation of modular systems consisting of circuits in three different voltage domains. A 3.3 V controller can be used to interface 5V serial data to 1.8V parallel data.

Modular design with partial power down (I_{OFF} circuitry)

74LVC8T595 includes I_{OFF} circuitry that prevents current paths through inputs and outputs (supply rails) when it is powered down, i.e., supply voltage $V_{CC} = 0$ V. I_{OFF} circuitry enables power management strategies to use partial-power down of sub-systems, saves energy in battery powered applications, and prevents damage to devices in handheld applications.



Recommended packages

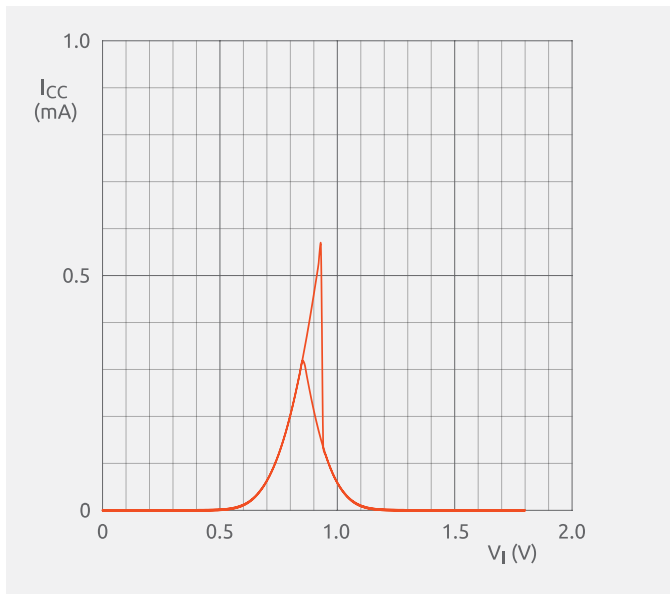
Suffix	Name	Package family	Dimensions (L x W x H, in mm)	
BQ	SOT764-1	DQFN20	4.5 x 2.5 x 1.0	
PW	SOT360-1	TSSOP20	6.5 x 6.4 x 1.1	



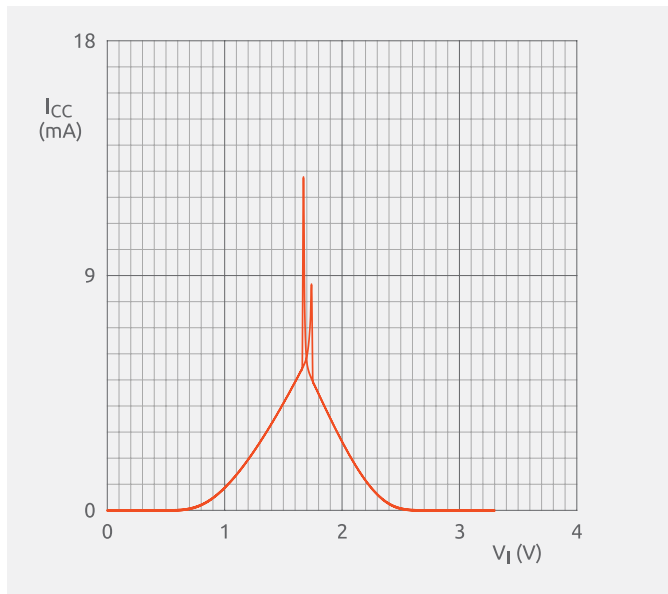
[Download the product datasheet](#)

Input Characteristics (typical)

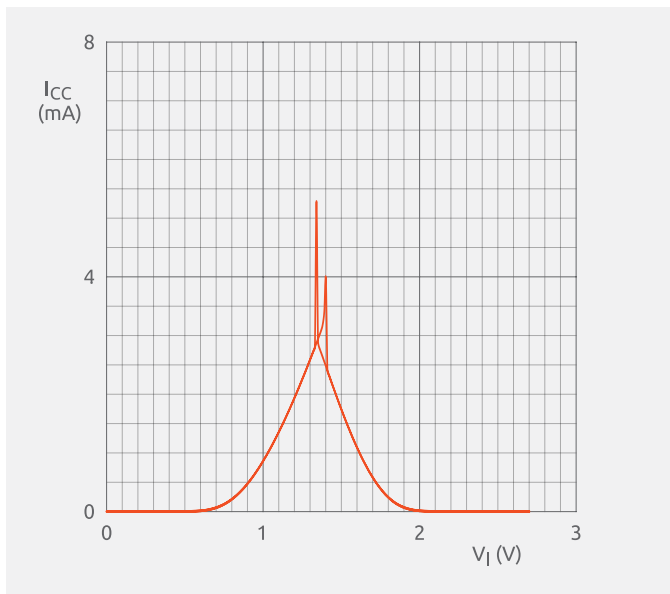
LVC8T595 uses Schmitt action to provide small hysteresis to prevent false switching and ensure well-defined outputs when driven by slowly transitioning signals.



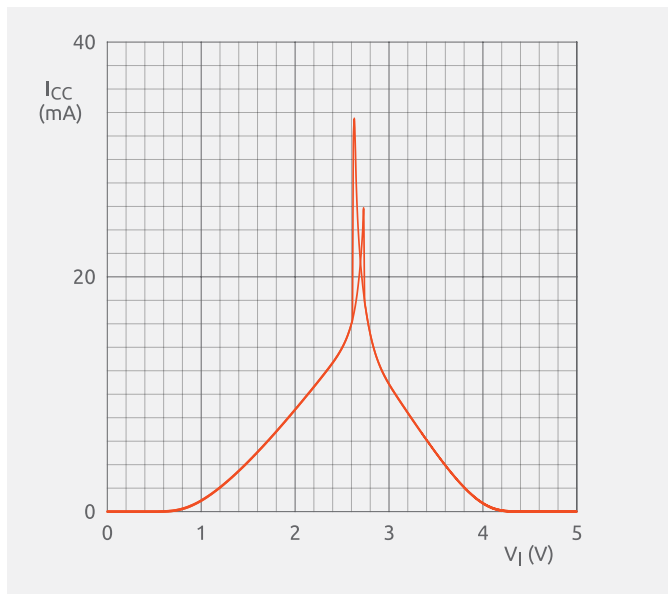
1.8 V Schmitt action



3.3 V Schmitt action

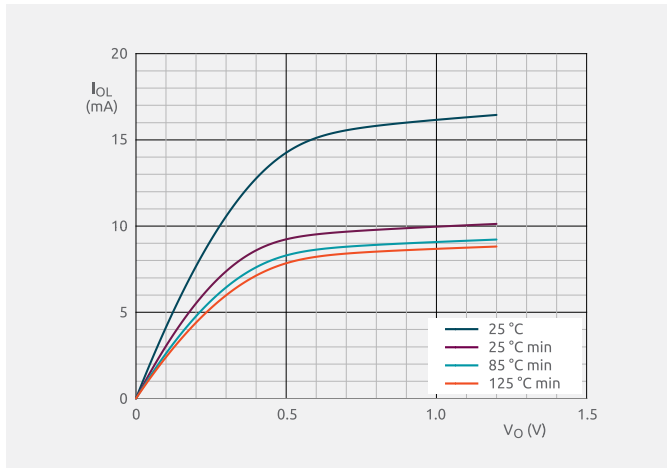


2.7 V Schmitt action

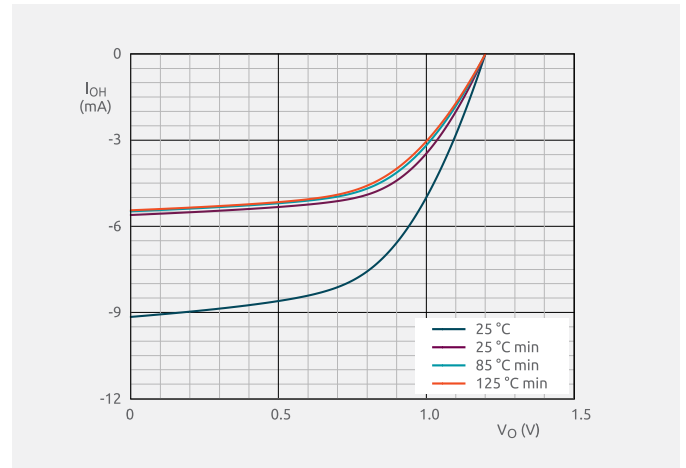


5.0 V Schmitt action

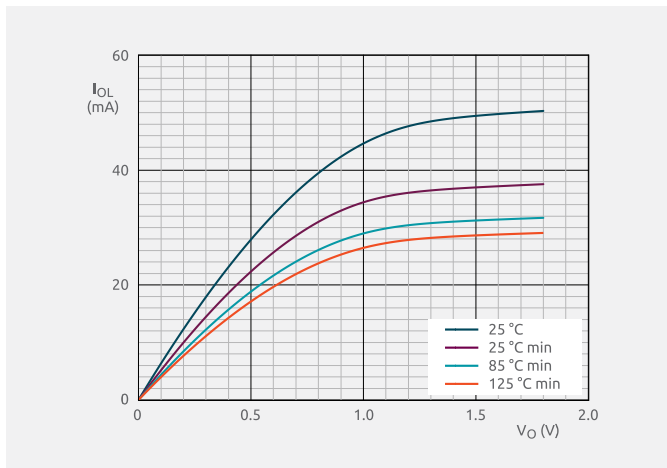
Outputs Characteristics (typical)



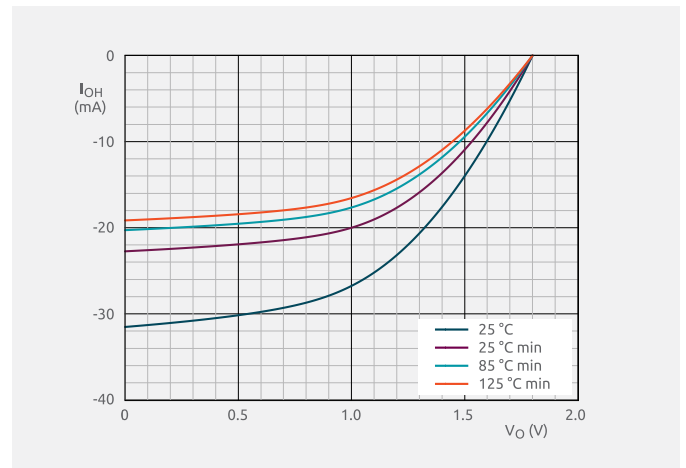
1.2 V Output driving LOW



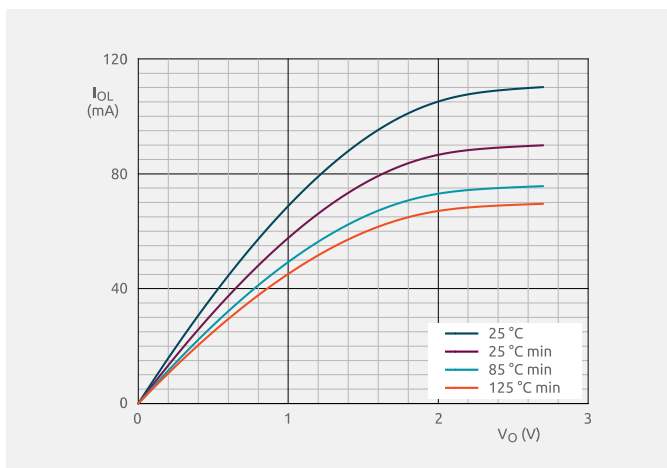
1.2 V Output driving HIGH



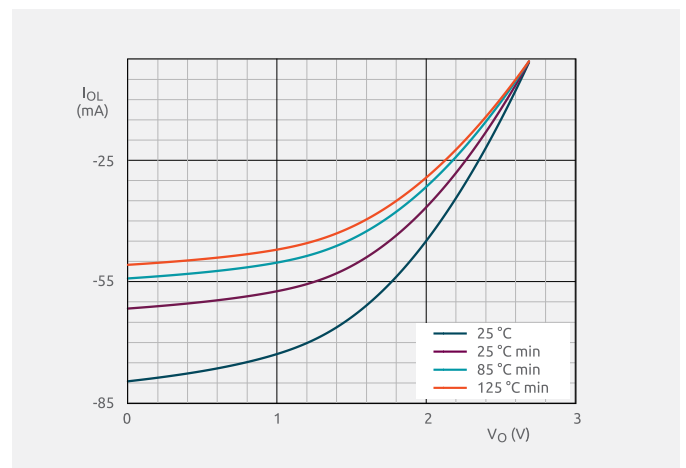
1.8 V Output driving LOW



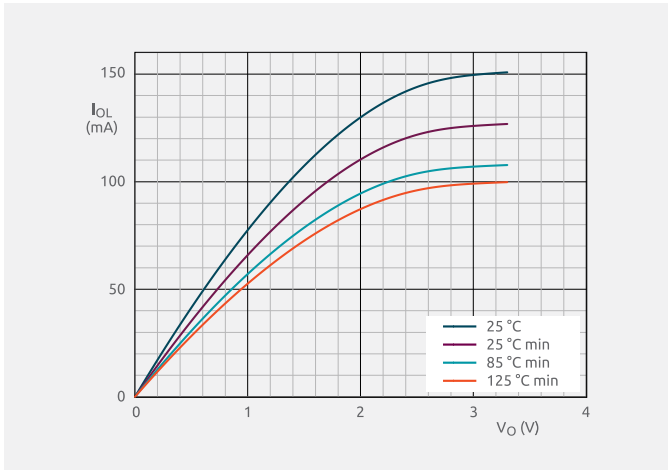
1.8 V Output driving HIGH



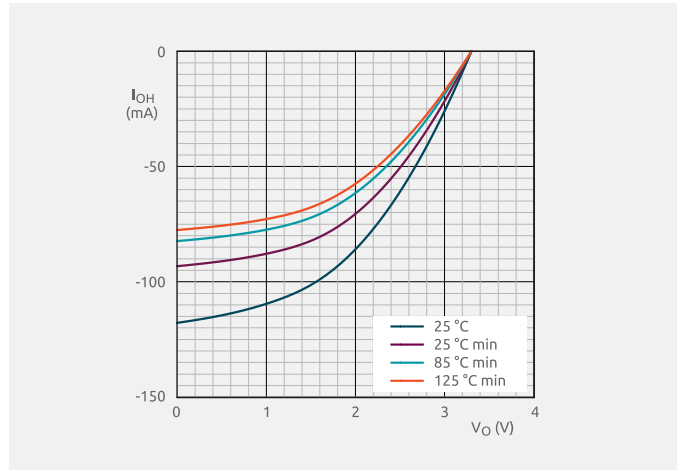
2.7 V Output driving LOW



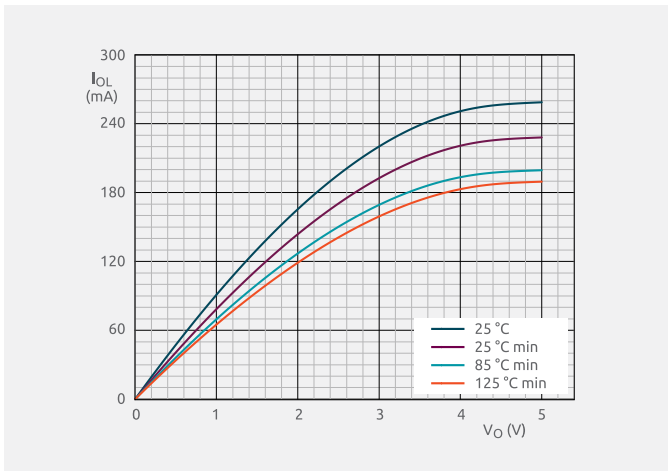
2.7 V Output driving HIGH



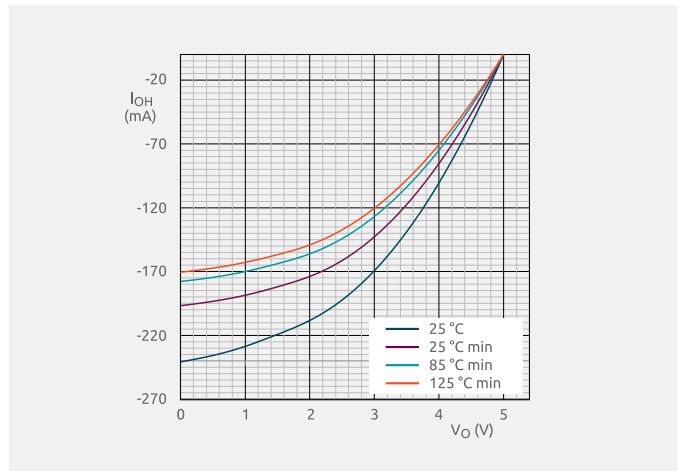
3.3 V Output driving LOW



3.3 V Output driving HIGH



5 V Output driving LOW



5 V Output driving HIGH

 [More information about our LVC technology](#)

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