



Nexperia ESD Seminar

Fundamentals of ESD Protection
and Automotive Interfaces

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EFFICIENCY WINS.



Session 1 | Fundamentals of ESD Protection

Does Nexperia provide SPICE models with air gap resistance modelling (e.g. Rompe-Weizel model)?

At Nexperia we focus on device modelling including SPICE models. However, we do not use SPICE models considering air gaps due to poor repeatability of results. Models with contact discharge and optimized signal integrity show better measurement quality. For even better insights, we recommend to use SEED simulation representing the application and ESD event very precisely.

How do I determine if I should add discrete series resistance on my signal lines, or if the inherent trace impedance is enough to protect the circuit?

The maximum resistance is always given by the application. You should try without additional resistance in the beginning. If you see that you cannot reach the target ESD level, you have to evaluate how much the application allows you to add and, try if this is sufficient.

Can you give a very brief history of ESD protection internal to the IC?

Throughout history, new ESD protection technologies were developed. First, people used large capacitors, but they have extremely bad clamping behaviour and are not applicable for data lines. Next, Zener diodes were used and optimized. This can be applied to both internal IC as well as external ESD protection. The main target is to reduce the clamping voltage to lower the ESD stress within the IC and system. New approaches such as "snap-back" behaviour offer a great protection behaviour to lower the clamping voltage. In addition, new materials and structures can be considered and help to improve the device level robustness for assembly but also the more important system level robustness.

Why is in some case V_{CL} lower than V_{BR} ?

The clamping voltage can be lower than breakdown voltage due to protection behaviours where the clamping voltage is actively lowered. The "snap-back" technology is a great example. A lower clamping voltage offers better system level protection and is not a disadvantage.

How is the dynamic resistance defined?

The gradient of the tangent in the operating point (OP) provides the dynamic resistance $R_{dyn(TLP)}$. $R_{dyn(TLP)}$ is determined for reverse and forward directions of the DUT. In fact of the linear behaviour $V = f(I)$, the tangent in the operating point can be approximated via the trendline Linear $V_{CL(TLP)} = f(I)$ and hence provides the dynamic resistance $R_{dyn(TLP)}$.



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How do you recommend maintaining the capacitance matching between the signal lines with separate devices?

The relative deviation of capacitance of separate ESD protection devices is almost the same. For instance, a 20 pF device for CAN bus shows about the same relative capacitance deviation as a 2 pF solution for Ethernet protection. As such, the absolute capacitance deviation becomes smaller if the device capacitance is lower. In this case, a 2 pF solution would show only 0.2 pF deviation (10% relative) showing minor impact on signal integrity and performance.

What is the difference between V_{RWM} and V_{BR} ?

The reverse working maximum voltage V_{RWM} indicates the DC voltage that can be applied without the device being active in order to not interrupt normal operation mode. The breakdown voltage V_{BR} is higher compared to the V_{RWM} and describes the transition of non-operating to operating mode. This can be also seen at the stated current. Therefore, there is a gap between both voltages to ensure safe operation.

Why does, in case of an ESD event, the EMI scanner shows higher current density at a different trace on PCB?

On the shown PCB, the ground connection is on the upper left. Thus, in case of the ESD event with external ESD protection, the current flows through the protection device directly to ground as the ESD protection functions as a current divider. Without external ESD protection, the ESD pulse can flow directly through the traces into the IC causing malfunction and less current flows to ground.

Is it needed to perform power dissipation calculation approximation?

Power dissipation is the product of clamping voltage times peak pulse current: $P = U \times I$. For instance, $I_{PP} = 5 \text{ A}$ and $V_{CL} = 41 \text{ V}$ would result in 205 W. Important to mention is that you can only draw limited information about the robustness and do not learn about the system level robustness. In case of a "snap-back" protection behaviour where the clamping voltage is actively lowered, the power dissipation would be lower as well. This can be confusing since the "snap-back" behaviour offers superior ESD protection. Therefore, the power dissipation does not provide a good indication of ESD robustness.



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Based on your photos for failure modes, an ESD failure is not only pin holes, but also burned polysilicon or metals?

Basically, everything can be destroyed but it is difficult to detect the exact root cause once the device is fully destroyed. To reconstruct the failure mode, a disruptive physical analysis and further investigation including SEED simulation can help.

Do the designers have to compute the area under the IEC61000-4-2 waveform and select proper ESD protection to reduce the second peak?

The parameters clamping voltage and peak pulse current provide a good indication of ESD protection. A low clamping voltage will, in effect, lower the shoulder of the ESD waveform. Different ESD protection technologies such as open-base transistors or thyristors with a "snap-back" behaviour can improve further.

What is SEED simulation?

SEED (System Efficient ESD Design) simulation is an effective approach to simulate an ESD event. It especially helps to match an IC with discrete ESD protection. For further introduction, we recommend our [white paper describing the concept and basic steps](#).

How is an EMI scanner working?

An EMI scanner can be used to measure the magnetic field and current flow on the PCB in case of ESD event. It operates with a near field probe which is positioned above the circuit. The duration ESD Event is roughly 100 ns. The EMI scanner cannot simulate but records a video of the PCB under test. The blue colour indicates low current density where the yellow or red colour indicates high current density. As such, it is possible to get a visual insight of ESD concept effectivity.

What are the derating parameters for ESD diodes?

Temperature is a major factor for derating parameters, however, silicon based ESD protection is characterized by minor performance loss over temperature. Thermal robustness is usually provided in the datasheet for a typical PCB stack-up.



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What is the difference between Zener and snap-back behaviour?

The main difference is the topology. The snap back devices have the open base or silicon controlled rectifier topology. Both of them allow to snap back which results in significant clamping voltage reduction. In comparison, a Zener protection starts to clamp when the breakdown voltage is achieved and clamping voltage is increasing slowly. All typologies should be considered when choosing an ESD protection device, though, for high-speed lines a snap-back typology will increase performance significantly.

If I have a circuit input voltage up to 42V DC and I would like to add a ESD diode. Can I use two ESD diodes with 24V RWM stack in series, if I do not like to use a single high V_{RWM} diode due to size and parasitic capacitance?

"It is possible to stack ESD protection devices in series. If you place two times the same ESD protection in series, the following happens:

- V_{RWM} is doubled
- $V_{trigger}$ / breakdown is doubled
- $V_{clamping}$ is doubled
- C_D is halved

Lab support - please indicate costs associated with this service. Is the EMI scanner (of ESD current) probably for sale/rental?

Nexperia offers consultancy and evaluation support on customer request. Extra cost may arise on an individual basis for e.g. special test boards. Please reach out to your Nexperia contact for further details.

After ESD tests, do you think thermal stress tests are necessary to identify any latency issues? How effective of the thermal stress test (after ESD tests) will be to identify any latency issues from your experience?

Usually, the ESD protection devices survive a reasonable amount of ESD pulses very well, without degradation. Thermal issues should be considered when a longer duration surge pulses are applied.



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Can ESD trigger a latch-up in an IC and thus cause secondary damage?

If a snap-back device is triggered, a latch-up can happen if the on-state current is higher than the hold current of the ESD protection device. However, most ESD protection devices withstand the current arising from this condition: Nexperia parts were tested in latch-up with 100mA for several hours without showing any damage or degradation. If an interface is affected, a soft fail occurs but no hardware fail. For many interfaces, the snap-back device automatically returns to its off-state once the affected data line is in single-ended low state.

Which type of material of product housing helps ESD surge to pass to PCB and damage Electronic components?

Nexperia uses industry proven mold compounds that fulfil all automotive quality requirements such as AEC-Q101 or MSL levels. Damage caused by electrical overstress (EOS) can be prevented by application design. In addition, a high I_{PPM} value can increase safety margin on device level.

What is the general failure mode of ESD diodes and which key factors have impact in operation lifetime?

ESD protection devices are usually robust devices. However, the environmental impacts usually are covered by qualifications tests, such as AEC-Q101 or similar.

Where in the datasheet can I find the forward voltage of bidirectional ESD diodes?

Usually, the forward voltage of ESD protection devices is not of importance for ESD purposes. However, this information can be shared with you on demand.

In case of quickly repeating spikes (transients rather than ESD), is the breakdown voltage decreasing due to repetition on newer devices?

While applying repeating spikes the device might be heated up. The increasing temperature will for sure impact the electrical behaviour, such as the break down voltage. We provide a measurement data over temperature on demand.

At which trace distance ESD pulses do not jump over?

The cross talk of ESD events is strongly dependent on your sub-application including the PCB, its stack-up etc. So, we cannot give a specific recommendation.



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Initial ESD peak we saw earlier goes typically to in between 50 and 100V (for both Zener type and latching devices) - isn't that dangerous enough for an IC? How do we check this against IC specifications?

The IC are typically robust for HBM up to 2kV. Or at least 500V. In addition, this is the first peak with has a duration of a few nanoseconds only. There is not much energy in this strike, and hence, usually not a problem for classic networks. It can be a problem for very sensitive, e.g. high speed ICs. Therefore, we suggest to use ESD devices with very low trigger and clamping voltage and, in addition with smallest parasitics, e.g. leadless packages, as discussed during the second session.

What is the difference between HBM requirements of car customers and AEC-Q101?

Quality requirements from customers may deviate due to individual assembly guidelines and special quality aspects. Nexperia offers dedicated product groups to fulfil highest quality standards above AEC-Q101.

In serial video links (FPD Link, GMSL, etc.) is it better to put the protection right next to the connector or after the decoupling capacitor?

The ESD protection should always be placed close to the connector in order to work as current divider and clamp the ESD current to ground. Depending on board net voltage, a higher V_{BR} must be considered. For instance, for a 24 V board net, a V_{BR} of >32 V should be chosen.

Do the trigger voltage of the SCR-based protectors depend on the $\Delta V/\Delta t$?

The trigger voltage is more determined by the physical structure of the ESD device but the dynamic resistance has a minor impact on the triggering behaviour as well.

Is there any tool developed by you which you can recommend for selection of ESD protection devices?

Nexperia provides a parametric search to filter certain parameters on our [webpage](#).



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What is TLP and how is it measured?

The transmission line pulse (TLP) is a short-duration rectangular pulse in a controlled impedance environment of 50Ω, which improves test accuracy and measurement reproducibility.

TLP characterizes performance attributes of devices under stresses that have a short pulse width and fast rise time. Each measurement result becomes a point on the TLP graph that shows a TLP I-V characteristic, i.e. the TLP-curve.

Regarding the leaded vs non-leaded packages comparison. Have you done an analysis on high vibration applications?

Nexperia automotive grades products are AEC-Q101 qualified if indicated in the datasheet. The ESD devices show very low self-heating since no power is applied. In addition, Nexperia performs several reliability tests according to JEDEC and ISO norms to ensure high reliability.

Some of the ESD failures are latent. How can you detect such failures?

Basically, there are two ESD failure modes: destructive where the device is damaged and non-destructive which show soft failure. Non-destructive failures are hard to detect but it helps to perform tests under incrementally higher voltages to determine destructive failure point. As such, sometimes degradation of the device can be detected early which provides a first indication of potential risk. Deviation of leakage current gives also a good indication.

For 24VDC power line would you use a reverse standoff voltage of 24V also?

For 24 V DC power line, a reverse standoff voltage of min. 32 V is required due to jump start requirements.

Is there a good way to simulate the model of an ESD gun to use for example in SPICE in order to try to prevent issues before building PCBs?

SEED (System Efficient ESD Design) simulation is an effective approach to simulate an ESD event. It especially helps to match an IC with discrete ESD protection. For further introduction, we recommend our white paper describing the concept and basic steps.



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Would the ESD design strategy be different for automotive safety critical systems?

The ESD design strategy is independent due to general ESD design aspects. However, additional requirements may narrow the range of suitable protection devices and include further tests. For instance, the ISO10605 states additional tests for automotive applications.

Are all Nexperia ESD protection devices AEC-Q200 qualified, and suitable for applications that require ASIL D?

Nexperia automotive grades products are AEC-Q101 qualified if indicated in the datasheet. All of our products are considered basic building blocks, where the functional safety criticality is defined by the system. This is important as a default failure mode for one device/system may not be suitable for another, and is the reason why we cannot assume any ASIL rating based on the ISO26262 methodology. Nexperia can provide further details and support to customers who will use ESD protection devices in safety critical applications.

Do you include S-Parameters in your datasheets for a specific test PCB layout as reference?

Scattering parameters can be included in datasheets depending on application and protection device. S-Parameter data can be send via e-mail on demand.

For sub GHz application, is there a way to optimize the impedance of the ESD device circuitry for better performance?

For sub GHz applications, the ESD protection device capacitance shows major impact on impedance. To improve impedance curve, a lower capacitance device may improve performance. The package has a minor impact in this area.

As the data transfer speeds keep increasing, are there more opportunities for cross talk causing transient spikes?

Cross talk depends on the sub-system. As PCB designs become smaller and show a higher density of traces, there might be a higher risk of cross talk. However, this is more on the PCB surface and not the periphery. The



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In some DC and low speed applications, just a capacitor is used for cost reasons. What is the consequence of just using just a capacitor for ESD protection?

If using just a capacitor, the ESD pulse might be damped a little but the system level protection is very low. A discrete ESD protection device adds significant improvement of system level ESD robustness and increase system reliability.

What are the ESD measures to be taken if a PCB is placed in metal housing and also in plastic housing?

The conducted discharge on the connector is only minor impacted by the housing of the module you are designing. The air discharge is very strongly depending the housing and, hence, should be considered during development.

For this type of small leadless DFN package, do you see any limitation with conformal coating on PCBA, in terms of solder joint fatigue?

For DFN package soldering and AOI guidelines, please refer to [Nexperia application notes](#).

In both SOT23 and DFN packages we need to connect the device to GND - isn't it better to omit the additional via inductance with different pin layout that will make possible connection to the GND on the same layer?

In this example with PCB having 4 or more layers, the GND layer is just below the top layer with a prepreg of around 100 μm . So the via inductance of 100 μm is small. However, depending on your PCB stack up you may route your GND pin differently.

SerDes with coax cable has any special need and offered by Nexperia?

Coax (single ended) or differential transmission has not a real impact on the electrical performance of the ESD protection device. It might impact the package of your protections device, since you need to decide how many lines you have to protect.



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Regarding Ethernet 100 Mbit/s, have you performed eye-diagram timing simulation (S-parameter) with ESD-protection diodes applied to the bus?

We are currently working on eye diagram measurements and simulations for other applications besides USBx and HDMIX.

How to check if the ESD characteristic of a PHY matches to the ESD protection?

A TLP curve comparison provides a quick indication for this. As such, the ESD protection device should trigger before the internal ESD protection of the PHY. For instance, a good match would be if the breakdown voltage of the ESD protection is 35 V and the breakdown voltage of the PHY is 60 V. In this combination, the ESD protection clamps first and takes the vast majority of ESD pulse.

Can you please repeat recommendations regarding RF immunity and which frequency area is more problematic?

There might be some issues related to DPI test. Those are, when too much energy is getting absorbed by the network during the test. In such case you need to choose a ESD protection device with higher trigger voltage.

How should the traces from connector to ESD device to circuit be routed in layout? Would it be possible to provide an layout recommendation in the datasheets?

The traces should be routed directly to the ESD protection device without changing layer or coupling to other PCB structure. However, the routing depends strongly on the sub-application and cannot be covered in datasheets.

Do new package technologies have disadvantages on reliability?

All Nexperia packages fulfil AEC-Q101 and other, highest quality standards.

For OPEN Alliance Ethernet, why does the trigger voltage has to be >100 V while the DC voltage is only 24 V?

The reason is the during the DPI test RF noise can achieve amplitudes up to 100 V. To avoid clamping of the ESD protection device, the triggering voltage was defined to be >100 V. The DC voltage over 24 V is related to the short to battery requirement (similar as for CAN/LIN).



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Do you see any disadvantage by destroying the differential pair on PCB because of a 3-pin package?

For some application such as LIN/CAN/Ethernet the 3-pin package does not impact the signal integrity significantly. For high frequency applications such as SerDes and Multimedia we recommend other, e.g. leadless packages.

Can dual ESD-diode PESD2ETH100-T be used in 1000 Mbit/s Ethernet bus?

For 1000BASE-T1 the PESD2ETH1G-T can be used with even smaller parasitic capacitance (<2 pF). For further product information use the selection guide on the [webpage](#).

Using eye diagram how can you tell what ESD diode is suitable?

By an eye diagram you can judge if the ESD protection is impacting your digital system too much or not. Besides S-parameters and parasitic capacitance, this is another view on the signal integrity on device level.

How important are s parameters for CAN?

For CAN it is more importance to look on the capacitance. However, for some CAN products Nexperia also provides S-parameters for CAN products.

What is the recommended TVS for Camera protection since they will be many cameras in a vehicle in the future?

For further product information please visit our [webpage](#).

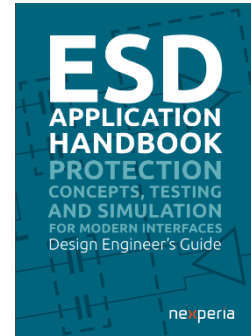
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Please find even more details in our ESD Handbooks

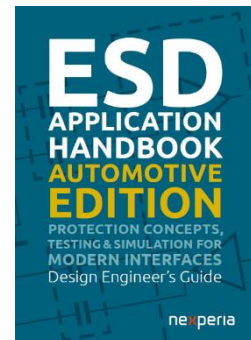
ESD Handbook with focus on ESD fundamentals and standard applications

- Fundamentals of ESD
- Datasheet parameters of ESD protection devices
- ESD testing standards and TLP testing
- Principles of ESD protection
- Failure symptoms caused by ESD and surge events
- Common interfaces and applications



Automotive ESD Handbook covering ESD fundamentals with high focus on automotive applications:

- Fundamentals of ESD
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- Principles of ESD protection
- Failure symptoms caused by ESD and surge events
- Automotive interfaces e.g. LIN, CAN & ETHERNET
- ESD simulations using SEED approach



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