SEED ROUND

Sergej Bub and Lukas Droemer show how seed modelling helps develop automotive Ethernet ESD protection that meets Open Alliance specifications

New trends in the automotive industry such as increased connectivity, electrification or autonomous driving are increasing the amount of data that must be transmitted around vehicles. This causes a corresponding increase in bandwidth requirements and existing protocols such as Lin, Can-FD and Flexray are no longer sufficient in a heterogeneous in-vehicle network.

Automotive Ethernet will be the way to handle data payload but new ESD protection devices are required to ensure safety. With system-efficient ESD design (seed), system-level approaches to ESD simulation are being employed to develop protection components that meet industry requirements.

As applications and technologies will continue to increase significantly the data payload that needs to be managed and transmitted in the car, a startling prediction is that the cost of wiring harness and electronics is increasing and could shortly account for 40 per cent of the cost of a car.

Changing the wiring harness to a hierarchical homogeneous network and zonal architecture is expected to reduce cost and cabling weight but also supports rising demands of high data-rates, data security and flexibility.

Automotive Ethernet therefore becomes vital for this network design to handle future requirements.

To encourage the wide scale adoption and standardisation of Ethernet-based networks, major automotive OEMs and tier-one suppliers are collaborating in the

non-profit Open (One-Pair EtherNet) Alliance special interest group (sig). Moreover, security and reliability have become more an issue to ensure safe operation of networks.

When it comes to system level robustness, discrete ESD protection devices as well as the system design take a crucial role and requirements emerging with Open Alliance standardised Ethernet must be considered.

A fundamental ESD design challenge is the prediction of system level robustness. A general misconception is that system level robustness depends on the robustness of individual components. Instead, it depends on several factors:

- the robustness of the weakest device in the system, usually the SoC that is to be protected;
- the properties of the protection device;
- properties of other elements in the signal path; and
- parasitic effects arising from the board and mounting wires.

The concept of seed is to consider all these parameters as an equivalent circuit or circuit-like simulation to predict system level robustness. An equivalent circuit

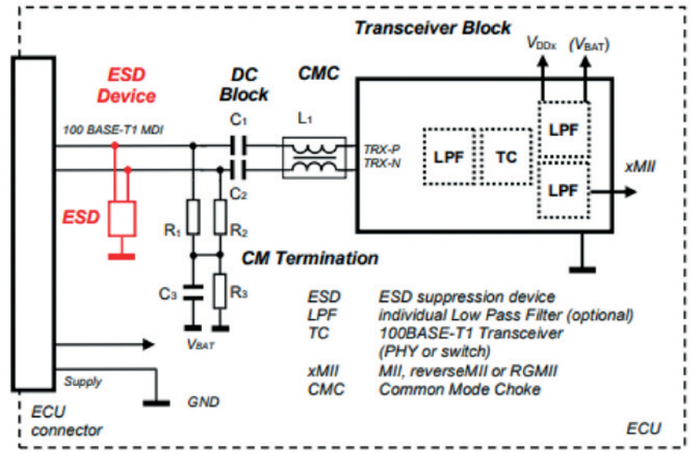

Fig. 1: Arrangement of ESD suppression device within the 100baseT1 MDI interface, Open Alliance sig (2019)

representation of the system, including the SoC, is connected with a model of the protection device to evaluate protection performance. As well as Spice-based simulations, other simulation tools such as Verilog-A and customised models based on network parameter blocks can be combined to realise the system simulation.

One key goal of the Open Alliance sig is to enable the deployment of the existing IEEE 100baseT1 and 1000baseT1 physical layer specifications with complementing specifications for conformance and interoperability. In previous Automotive Ethernet implementations, phy (physical layer interface, referring to the transceiver) vendors were advised to put any required discrete ESD protection device between the CMC (common-mode choke) and the phy.

Now, in the arrangement of ESD protection devices within the 100baseT1 MDI network proposed by the Open Alliance, see Fig. 1, the ESD protection device is placed immediately next to the connector, protecting not only the phy but also the CMC and passives. Positioned thus, ESD strikes are directed straight to ground.

The Open Alliance proposes a

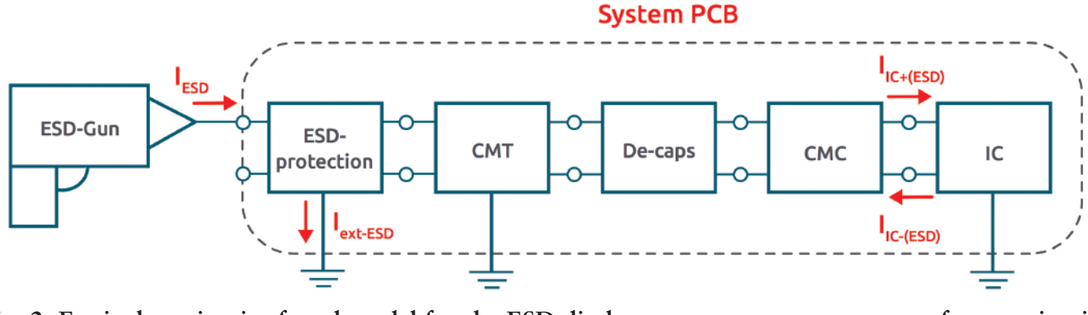

Fig. 2: Equivalent circuit of seed model for the ESD discharge current measurement reference circuit

measurement called ESD discharge current measurement, which gives an estimation of the overall system-level ESD robustness of the system. This test determines the residual current into the phy, identifying the ESD robustness class according to human body model requirements.

When developing silicon-based, Open Alliance-compliant ESD protection for 100 and 1000baseT1 Automotive Ethernet systems, seed methodology can replicate the ESD discharge current measurement test. This simulation allows the investigation into how different parameters, including the parasitic inductance of the external ESD protection device, its trigger and snap-back behaviour, influence the system level ESD robustness. This approach also enables developers to predict the levels of electromagnetic stress that other passive devices are exposed to during an ESD event.

Fig. 2 shows the equivalent circuit block diagram of the seed model for the ESD discharge current measurement reference circuit. It consists of an external ESD device, the common mode termination (CMT) elements, a decoupling network, a CMC and a 100baseT1 phy IC. This is realised in the test board shown in Fig. 3.

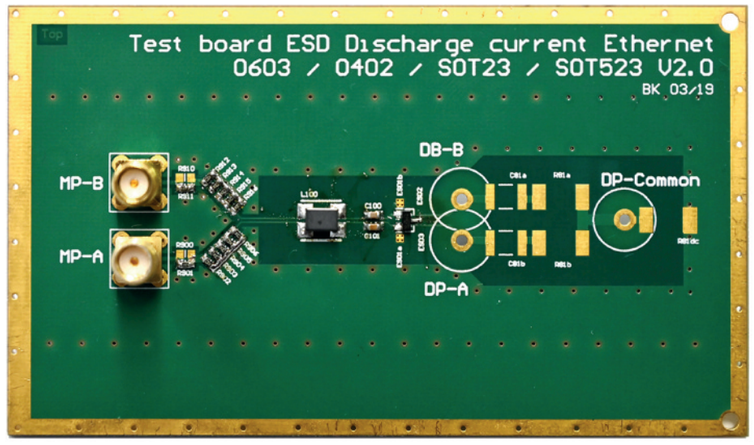

Fig. 3: Photo of reference PCB, actual size 10.25 by 5.95cm

Whereas the CMC is a single device with an inductance in this example of 200μH, the ESD device can be a single device which integrates matched ESD protection for both data lines, as in this example, or two separate devices each connected between GND and one of the data lines.

The phy is replaced by a transceiver emulation network, thus retaining the electrical behaviour during the ESD test. A 2Ω resistor emulates the typical behaviour of the IC internal protection in a simplified way, while the 50Ω resistor reduces the measurement effort of the IC current.

The CMT network, located between the CMC and external ESD protection devices, consists of four discrete elements and two 100nF capacitances are used for decoupling. The input of the test board is connected directly to the ESD device.

To reduce the modelling effort and accelerate the simulation process, a behavioural modelling approach is used. The model, tuned on the device's typical static and dynamic characteristics, is implemented as an equivalent circuit consisting of lumped elements, controlled sources and feedback loops, and S-parameter blocks.

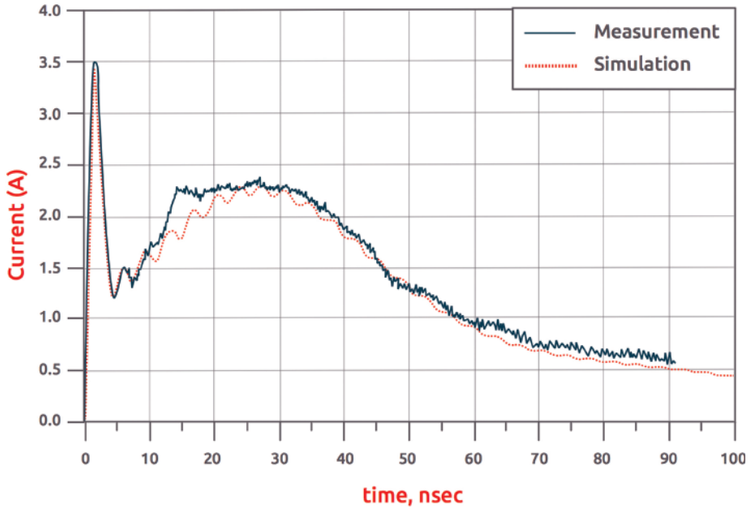

Fig. 4: Model and measurement of ESD generator waveform at 2kV on a 2Ω reference target

Fig. 4 shows a good match between simulated and measured time domain current curves in both first and second peak regions for a 2kV discharge.

Following this, each element of the seed model – decoupling and termination network, CMC, and ESD protector – can be evaluated. Fig. 5 shows the measured and simulated performance for the external silicon based ESD protection lean on peak voltage and current of 1ns rise time TLP pulses.

After this, the complete system model (Fig. 2) was validated against measurements taken from the reference board with and without external ESD protection using TLP.

The TLP graph of a reference board with external ESD protection in Fig. 6 compares measured results and simulation results using seed, demonstrating an extraordinary degree of congruence, showing that the implemented seed model is fully suitable not only for qualitative but also quantitative prediction of overall system-level robustness.

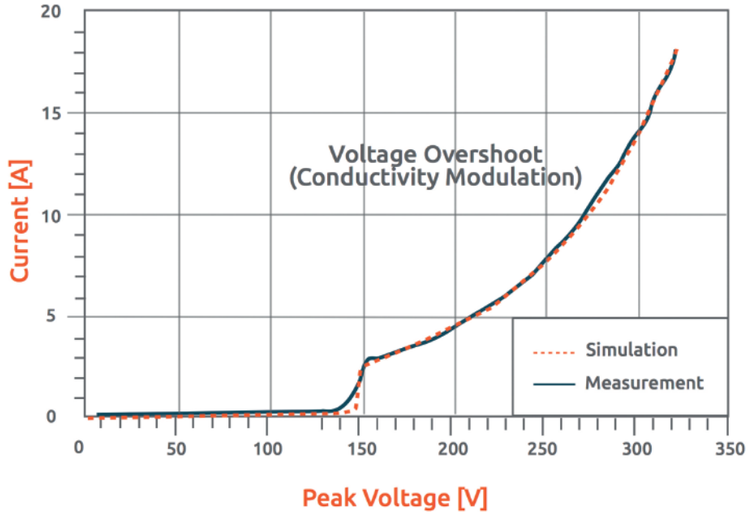

Fig. 5: Measured and simulated plots for external silicon-based ESD protection lean on peak voltage and current of 1ns rise time TLP pulses

An ESD strike may occur when a person touches the GND or IO pin(s) of the system board connector. This is replicated by injecting ESD pulses according to IEC61000-4-2 into the system.

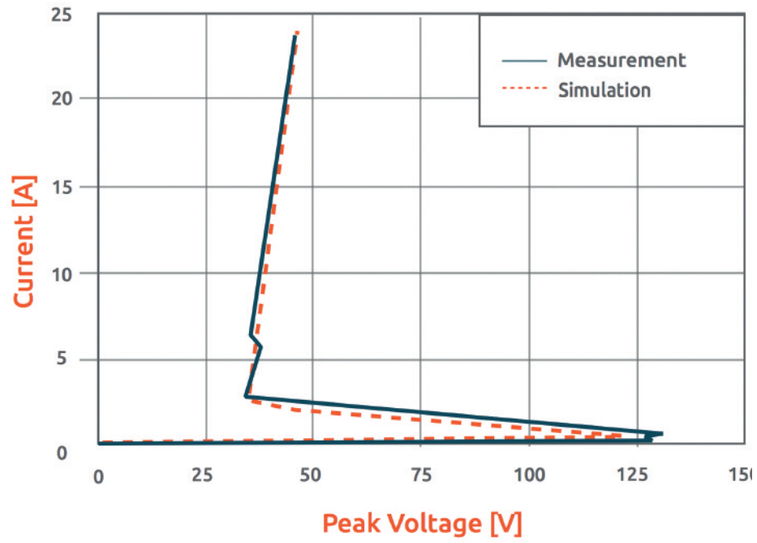

Fig. 6: Measured and simulated TLP plots for the reference board with external ESD protection device; voltage and current are averaged between 70 and 90ns of 100ns TLP pulses

Again, results of the seed-generated simulation showed close agreement with the observed measurement.

Using this approach, Open Alliance-compliant ESD protection for 100 and 1000baseT1 Ethernet has been developed. Silicon devices offer a significantly higher level of protection – up to 30kV system level robustness – than older technologies such as varistors, which are also subject to degradation over time.

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