

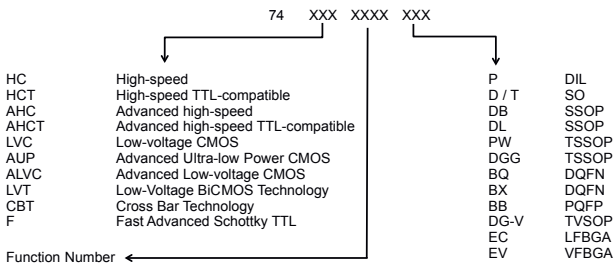
# Competitive Package Cross-Reference: NXP Logic Products

Package Image width x length x height (mm)	Pitch (mm)	NXP	TI	Fairchild	ON	Toshiba
 MicroPak 0.8 x 0.8 x 0.35	0.5	GX				
 MicroPak 1.0 x 0.9 x 0.35	0.3	GN				
 MicroPak 1.0 x 1.0 x 0.5 GF 1.0 x 1.0 x 0.35 GS	0.35	GF GS	DSF	FHX	CMX	fsV fs6
 MicroPak 1.0 x 1.5 x 0.5 GM 1.0 x 1.95 x 0.5 GT	0.5	GM GT	RSE RSE	L6 L8		
 PicoGate 2.0 x 2.0 x 1.0	0.65	GW	DCK	P5 P6	DFT	FU
 PicoGate 2.8 x 2.9 x 1.0	0.95	GV	DBV	M5 M6	DTT	F
 VSSOP-8 2.0 x 3.0 x 1.0 2.0 x 3.0 x 0.5	0.5	DC GD	DCV Footprint compatible	K8 Footprint compatible	VS Footprint compatible	FK Footprint compatible
 TSSOP-8 3.0 x 4.0 x 1.1	0.65	DP	DCT			FU



Package Image	Pitch (mm)	NXP	TI	Fairchild	ON	Toshiba
 8,10,12,16 Leads	0.4	GU	RSW	UMX	MU	
 DQFN	0.5	BQ		BQ		
 48 pin - 96 pin BGA	0.65 0.8	EV EC	ZQL GKE			
 DR-QFN	0.5	BX				
 TSSOP	0.65 0.5	PW DGG	PW DGG	MTC 24 PIN and below MTD Above 24 Pin	DT	FT
 SSOP	0.65 0.635	DB DL	DB DL			
 SO	1.27	D / T	D DW	M / SC	DR DW	FW
 DIL	0.1 (inch)	P	E	CN	CP	BP

Nomenclature for functions in SO, SSOP, TSSOP, BGA, & DQFN Package



Nomenclature for functions in the PicoGate and MicroPak Packages

