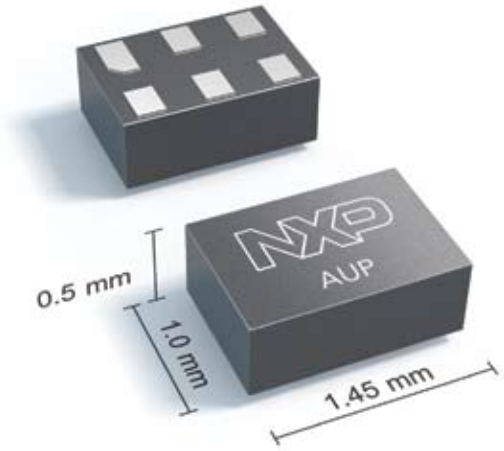

NXP ultra-low-power CMOS logic 74AUP1G/2G/3Gxxx

Advanced, ultra-low-power CMOS logic

Designed for high-performance, low-power applications, these low-voltage, Si-gate CMOS devices offer the industry's lowest dynamic power consumption in a logic device.

Features

- Very low dynamic power dissipation capacitance (C_{PD})
- t_{PD} of 2.5 ns at V_{CC} of 2.5 V
- Wide supply voltage range (0.8 to 3.6 V)
- Schmitt-trigger action on all inputs
- Over-voltage-tolerant I/Os
- PicoGate and MicroPak package options
- Single-, dual-, and triple-gate functions
- Extended temperature range (–40 to +125 °C)

Benefits

- Low propagation delay for advanced applications
- Wide operating voltage for mixed-voltage applications
- Schmitt-trigger action on all inputs for high noise immunity
- Extremely low power consumption for extended battery life

The NXP 74AUP1G/2G/3Gxx family of Si-gate CMOS devices uses advanced process technology and next-generation packaging technology to create extremely small functions that consume very little power. The devices are available in single- (1Gxx), dual- (2Gxx), and triple-gate (3Gxx) formats.

AUP devices offer the industry's lowest power dissipation capacitance (C_{PD}), yet maintain low propagation delays (t_{PD}) and superior ESD protection. Typical C_{PD} at 1.8 V is only 3.5 pF and at 3.3 V is only 4.3 pF, while the t_{PD} at a V_{CC} of 2.5 V is only 2.5 ns.

Mixed-voltage applications

Operating over a very wide supply range of 0.8 to 3.6 V, AUP devices are ideally suited for use in mixed-voltage applications. Schmitt-trigger action at all inputs improves noise immunity by making the circuit tolerant to slower input rise and fall times across the entire range of supply voltage.

Longer battery life

The devices extend battery life by ensuring very low power consumption across the entire V_{CC} range in static and dynamic modes. On average, the AUP family offers power consumption that is 30% lower than competing logic functions.

To save even more battery power, the devices are fully specified for partial power-down applications that use the I_{OFF} feature. The I_{OFF} circuitry disables the output, preventing damage caused by backflow current passing through the device when it's powered down.

PicoGate and MicroPak packaging

AUP devices are available in PicoGate and MicroPak packages, which are roughly ten times smaller than a conven-

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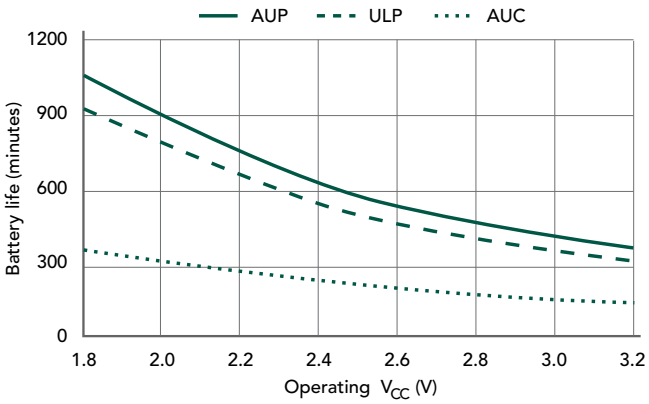
tional SO14 package. PicoGate and MicroPak products reduce time-to-market by making it easy to implement last-minute changes. They also improve the cost-effectiveness of crowded layouts, by simplifying routing and eliminating dependencies in intricate line-layout patterns.

The AUP family operates over an extended temperature range (–40 to +125 °C) that is suitable for a wide range of applications, including portable, consumer, automotive, and military. Multi-pin (5-, 6-, and 8-pin) packages make it easy to select the right combination of features.



AUP product family

Type no.	Description	Pins	Status	SOT353-1	SOT363	SOT765-1	SOT886	SOT833	SOT902
Single-gate functions									
1G00	Single two-input NAND gate	5	Production	•			•		
1G02	Single two-input NOR gate	5	Production	•			•		
1G04	Single inverter	5	Production	•			•		
1G06	Single inverter (open drain output)	5	Production	•			•		
1G08	Single two-input AND gate	5	Production	•			•		
1G125	Dual 3-state buffer with active low OE	5	Production	•			•		
1G126	Dual 3-state buffer with active high OE	5	Production	•			•		
1G14	Single Schmitt-trigger inverter	5	Production	•			•		
1G17	Single Schmitt-trigger buffer	5	Production	•			•		
1G32	Single two-input OR gate	5	Production	•			•		
1G34	Single buffer	5	Production	•			•		
1G66	Analog switch	5	Development	•			•		
1G80	D-type flip-flop; positive-edge trigger	5	Development	•			•		
1G86	Single X-OR gate	5	Production	•			•		
1GU04	Single inverter (unbuffered)	5	Production	•			•		
Dual-gate functions									
2G00	Dual two-input NAND gate	8	Development			•		•	•
2G02	Dual two-input NOR gate	8	Development			•		•	•
2G04	Dual inverter	6	Sampling		•		•		
2G06	Dual inverter (open drain output)	6	Sampling		•		•		
2G08	Dual two-input AND gate	8	Development			•		•	•
2G125	Dual 3-state buffer with active low OE	8	Development			•		•	•
2G126	Dual 3-state buffer with active high OE	8	Development			•		•	•
2G14	Dual Schmitt-trigger inverter	6	Production		•		•		
2G17	Dual Schmitt-trigger buffer	6	Development		•		•		
2G34	Dual buffer	6	Production		•		•		
2GU04	Dual inverter (unbuffered)	6	Production		•		•		
Triple-gate functions									
3G04	Triple inverter	8	Development			•		•	•
3G07	Triple inverter (open drain output)	8	Development			•		•	•
3G14	Triple Schmitt-trigger inverter	8	Development			•		•	•
3G17	Triple Schmitt-trigger buffer	8	Development			•		•	•
3G34	Triple buffer	8	Development			•		•	•
3GU04	Triple inverter (unbuffered)	8	Development			•		•	•

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NXP Semiconductors is in the process of being established as a separate legal entity in various countries worldwide. This process will be finalized in the course of 2006.

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