XC7SET86 2-input EXCLUSIVE-OR gate Rev. 3 — 18 December 2023

Product data sheet

1. General description

XC7SET86 is a high-speed Si-gate CMOS device. It provides a 2-input EXCLUSIVE-OR function.

2. Features and benefits

- Symmetrical output impedance
- High noise immunity
- Low power dissipation
- TTL input levels
- Balanced propagation delays
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

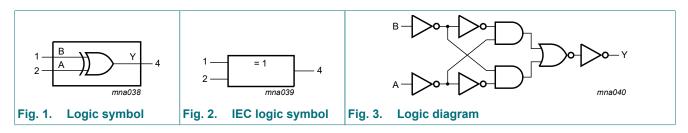
Type number	Package							
	Temperature range Name Description Name							
XC7SET86GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	<u>SOT353-1</u>				
XC7SET86GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	<u>SOT753</u>				

4. Marking

Table 2. Marking codes					
Type number	Marking code [1]				
XC7SET86GW	gH				
XC7SET86GV	g86				

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

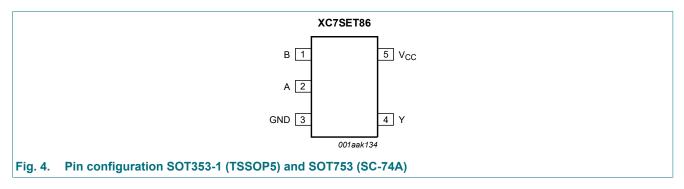
5. Functional diagram



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6. Pinning information

6.1. Pinning



6.2. Pin description

Symbol	Pin	Description
В	1	data input
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V _{CC}	5	supply voltage

7. Functional description

Table 4. Function table

. .

H = HIGH voltage level; L = LOW voltage level.

Inputs	Output	
Α	В	Y
L	L	L
L	Н	Н
Н	L	Н
Н	Н	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
VI	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V	-20	-	mA
I _{OK}	output clamping current	$V_{\rm O} < -0.5 \text{ V or } V_{\rm O} > V_{\rm CC} + 0.5 \text{ V}$ [1]	-	±20	mA
I _O	output current	$-0.5 V < V_{O} < V_{CC} + 0.5 V$	-	±25	mA
I _{CC}	supply current		-	75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	$T_{amb} = -40 \text{ °C to } +125 \text{ °C}$ [2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: Ptot derates linearly with 3.3 mW/K above 74 °C.

For SOT753 (SC-74A) package: Ptot derates linearly with 3.8 mW/K above 85 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		4.5	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate		-	-	20	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	neter Conditions		25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Мах	
VIH	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = -50 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.8	-	3.70	-	V
V _{OL}	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = 50 μA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
l _l	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	1.0	-	10	-	40	μA
ΔI _{CC}	additional supply current	per input pin; V _I = 3.4 V; other inputs at V _{CC} or GND; $I_O = 0 A$; V _{CC} = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
Cı	input capacitance		-	1.5	10	-	10	-	10	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V. For waveform see Fig. 5. For test circuit see Fig. 6.

Symbol	Parameter	Conditions	25		25 °C		-40 °C to +85 °C		-40 °C to +125 °C	
			Min	Тур	Max	Min	Max	Min	Max	
t _{pd}	propagation delay	A and B to Y; [1] [V _{CC} = 4.5 V to 5.5 V	2]							
		C _L = 15 pF	-	3.5	6.9	1.0	8.0	1.0	9.0	ns
		C _L = 50 pF	-	5.0	7.9	1.0	9.0	1.0	10.5	ns
C _{PD}	power dissipation capacitance	f = 1 MHz;	3] -	11	-	-	-	-	-	pF

 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

 V_{CC} = supply voltage in V.

11.1. Waveform and test circuit

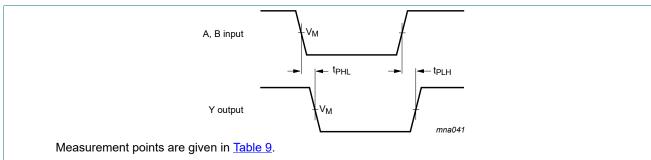
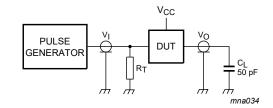


Fig. 5. The input (A and B) to output (Y) propagation delays

Table 9. Measurement points

Input	Output	
VI	V _M	
GND to 3.0 V	1.5 V	$0.5 \times V_{CC}$



Test data is given in <u>Table 10</u>.

Definitions for test circuit:

C_L = load capacitance including jig and probe capacitance;

 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Input		Load	Test
V _I	t _r , t _f	CL	
3.0 V	≤ 3.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

12. Package outline

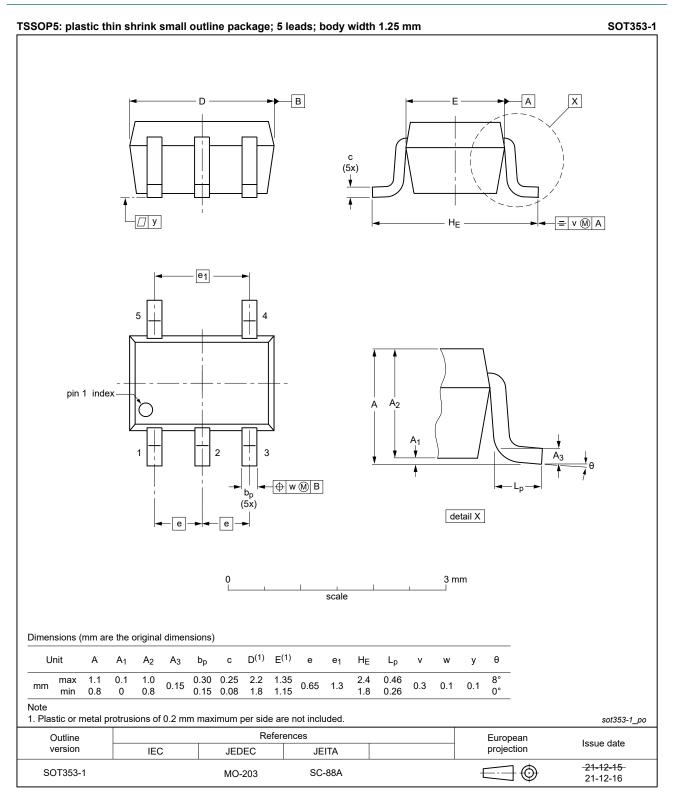


Fig. 7. Package outline SOT353-1 (TSSOP5)

XC7SET86

2-input EXCLUSIVE-OR gate



SOT753

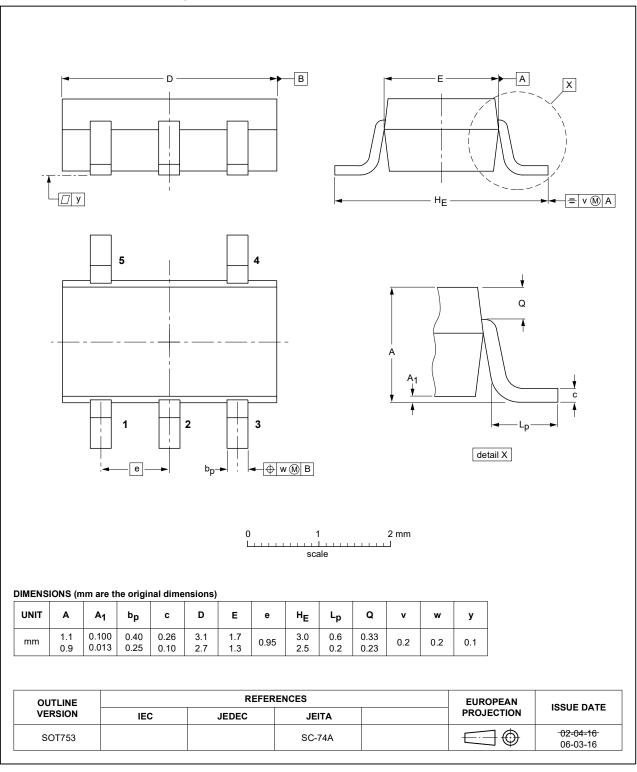


Fig. 8. Package outline SOT753 (SC-74A)

13. Abbreviations

Table 11. Abbreviations					
Acronym	Description				
CDM	Charged Device Model				
CMOS	Complementary Metal-Oxide Semiconductor				
DUT	Device Under Test				
ESD	ElectroStatic Discharge				
HBM	Human Body Model				
TTL	Transistor-Transistor Logic				

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes					
XC7SET86 v.3	20231218	Product data sheet	-	XC7SET86 v.2					
Modifications:	• <u>Section 2</u> : ESD specification updated according to the latest JEDEC standard.								
XC7SET86 v.2	20220113	Product data sheet	-	XC7SET86 v.1					
Modifications:	guidelines o Legal texts I <u>Section 8</u> : D	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. <u>Section 8</u>: Derating values for P_{tot} total power dissipation updated. Fig. 7: Package outline drawing SOT353-1 (TSSOP5) has changed. 							
XC7SET86 v.1	20090907	Product data sheet	-	-					

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
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