1. General description

The device is designed to protect high-speed interfaces such as SuperSpeed and Hi-Speed USB combination, Secure Digital (SD) card 3.0 and Thunderbolt interfaces against ElectroStatic Discharge (ESD).

The device includes six high-level ESD protection diode structures for ultra high-speed signal lines and is encapsulated in a DFN2111-7 (SOT1358-1) leadless ultra small Surface-Mounted Device (SMD) plastic package.

All signal lines are protected by a special diode structure offering ultra low line capacitance of only 0.27 pF. These diodes utilize a unique snap-back structure in order to provide protection to downstream components from ESD voltages up to ±10 kV contact exceeding IEC 61000-4-2, level 4.

2. Features and benefits

- System ESD protection for USB 2.0 and USB 3.2 combination, SD card 3.0 and Thunderbolt interfaces
- All signal lines with integrated rail-to-rail clamping diodes for downstream ESD protection of ±10 kV exceeding IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Signal lines with ≤ 0.05 pF matching capacitance between signal pairs
- Line capacitance of only 0.27 pF for each channel
- Design-friendly pass-through signal routing

3. Applications

The device is designed for high-speed receiver and transmitter port protection:

- Portable and wearable devices
- Smartphones and tablet PCs
- TVs and monitors
- DVD recorders and players
- Notebooks, main board graphic cards and ports
- Set-top boxes and game consoles
4. Pinning information

Table 1. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>CH1</td>
<td>channel 1 ESD protection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>ground[1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>CH2</td>
<td>channel 2 ESD protection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>CH3</td>
<td>channel 3 ESD protection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>CH4</td>
<td>channel 4 ESD protection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>CH5</td>
<td>channel 5 ESD protection</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>CH6</td>
<td>channel 6 ESD protection</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[1] Any pin can be chosen for ground connection; one pin must be connected to ground.

5. Ordering information

Table 2. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>PUSB3TB6</td>
<td>XSON7</td>
<td>plastic, leadless extremely thin small outline package; 7 terminals; 0.5 mm pitch; 1.1 mm x 2.1 mm x 0.5 mm body</td>
<td>SOT1358-1</td>
<td></td>
</tr>
</tbody>
</table>

6. Marking

Table 3. Marking codes

<table>
<thead>
<tr>
<th>Type number</th>
<th>Marking code</th>
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</thead>
<tbody>
<tr>
<td>PUSB3TB6</td>
<td>3T</td>
</tr>
</tbody>
</table>
7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_I$</td>
<td>input voltage</td>
<td></td>
<td>-5.5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$V_{ESD}$</td>
<td>electrostatic discharge</td>
<td>IEC 61000-4-2, level 4; contact discharge [1]</td>
<td>-10</td>
<td>10</td>
<td>kV</td>
</tr>
<tr>
<td></td>
<td>voltage</td>
<td>IEC 61000-4-2, level 4; air discharge [1]</td>
<td>-15</td>
<td>15</td>
<td>kV</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>storage temperature</td>
<td></td>
<td>-55</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{amb}$</td>
<td>ambient temperature</td>
<td></td>
<td>-40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

[1] All pins to ground.

8. Characteristics

Table 5. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BR}$</td>
<td>breakdown voltage</td>
<td>$I_I = 1$ mA; $T_{amb} = 25$ °C</td>
<td>6</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$I_{LR}$</td>
<td>reverse leakage current</td>
<td>per channel; $V_I = 3$ V; $T_{amb} = 25$ °C</td>
<td>-</td>
<td>1</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>$C_{line}$</td>
<td>line capacitance</td>
<td>$f = 1$ MHz; $V_I = 0$ V; $T_{amb} = 25$ °C</td>
<td>[1]</td>
<td>0.27</td>
<td>0.35</td>
<td>pF</td>
</tr>
<tr>
<td>$\Delta C_{line}$</td>
<td>line capacitance difference</td>
<td>$f = 1$ MHz; $V_I = 0$ V</td>
<td>[1]</td>
<td>0.03</td>
<td>0.05</td>
<td>pF</td>
</tr>
<tr>
<td>$r_{dyn}$</td>
<td>dynamic resistance</td>
<td>TLP; positive transient; $T_{amb} = 25$ °C</td>
<td>[2]</td>
<td>0.6</td>
<td>-</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TLP; negative transient; $T_{amb} = 25$ °C</td>
<td>[2]</td>
<td>0.6</td>
<td>-</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td>surge; 8/20 μs; $T_{amb} = 25$ °C</td>
<td>[3]</td>
<td>0.5</td>
<td>0</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>[3]</td>
<td>0.5</td>
<td>-</td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{CL}$</td>
<td>clamping voltage</td>
<td>$I_{PP} = 3.5$ A; positive transient; $T_{amb} = 25$ °C</td>
<td>[3]</td>
<td>4.8</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{PP} = -3.5$ A; negative transient; $T_{amb} = 25$ °C</td>
<td>[3]</td>
<td>-4.8</td>
<td>-</td>
<td>V</td>
</tr>
</tbody>
</table>

[1] The parameter is guaranteed by design.
[2] 100 ns Transmission Line Pulse (TLP), 50 Ω, pulser at 80 ns.
ESD protection for ultra high-speed interfaces

Fig. 1. Insertion loss; typical values

\[ a = \frac{C_{\text{line}}}{C_{\text{line}(V_i = 0 \text{ V})}} \]

Fig. 2. Relative capacitance as a function of input voltage; typical values

Fig. 3. Crosstalk; typical values

normalized to 100 #Ω

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Data rate: 5 Gbit/s
Vertical scale: 160 mV/div
Horizontal scale: 20 ps/div

Fig. 4. **USB 3.0 eye diagram, PCB with device**

Data rate: 5 Gbit/s
Vertical scale: 162.5 mV/div
Horizontal scale: 20 ps/div

Fig. 5. **USB 3.0 eye diagram, PCB without device**
ESD protection for ultra high-speed interfaces

**Fig. 6.** Dynamic resistance with positive clamping; typical values

IEC 61000-4-5; \( t_p = 8/20 \) μS; positive pulse

**Fig. 7.** Dynamic resistance with negative clamping; typical values

IEC 61000-4-5; \( t_p = 8/20 \) μS; negative pulse

**Fig. 8.** Dynamic resistance with positive clamping; typical values

\( t_p = 100 \) ns; Transmission Line Pulse (TLP)

**Fig. 9.** Dynamic resistance with negative clamping; typical values

\( t_p = 100 \) ns; Transmission Line Pulse (TLP)
9. Application information

The device is designed to provide high-level ESD protection for high-speed serial data buses such as HDMI, DisplayPort, eSATA and LVDS data lines.

**Note:** When designing the PCB, give careful consideration to impedance matching and signal coupling. Do not connect the signal lines to unlimited current sources like, for example, a battery.

ESD protection schematic diagram for USB 3.0 or USB 2.0 interface is shown on Figure 10.

---

**Fig. 10. Demo PCB of ESD protection for USB 3.0 or USB 2.0 interfaces using PUSB3TB6**

Any pin can be chosen for ground connection; one pin must be connected to ground.

---

A basic application diagram for ESD protection of SD card interface is shown on Figure 11. GND can be connected to pin 2 for easy routing or to any other rail-to-rail structure.

---

**Fig. 11. Application diagram of SD card ESD protection using PUSB3TB6**

Any pin can be chosen for ground connection; one pin must be connected to ground.
Dynamic resistance
The device uses an advanced clamping structure showing a negative dynamic resistance.
This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

10. Package outline

Fig. 12. Package outline XSON7 (SOT1358-1)
11. Soldering

Footprint information for reflow soldering of DFN2111-7 (SOT1358-1) package

Fig. 13. Reflow soldering footprint for XSON7 (SOT1358-1)
## 12. Revision history

<table>
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<th>Release date</th>
<th>Data sheet status</th>
<th>Change notice</th>
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<td>20180823</td>
<td>Product data sheet</td>
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<td>PUSB3TB6 v.1</td>
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**Modifications:**
- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.
- Legal texts have been adapted to the new company name where appropriate.

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ESD protection for ultra high-speed interfaces

13. Legal information

Data sheet status

<table>
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Preliminary [short] data sheet Qualification This document contains data from the preliminary specification.

Product [short] data sheet Production This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term "short data sheet" is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com

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