



PUSB3CB4

Extremely low capacitance bidirectional ESD protection diode array

8 August 2023

Product data sheet

1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode array, part of the TrEOS protection family. This device is housed in a DFN2510A-10 (SOT1176) leadless ultra small Surface-Mounted Device (SMD) plastic package, designed to protect four signal lines from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection for four signal lines
- $V_{RWM} = 3.3$ V device
- Extremely low clamping voltage to protect sensitive I/Os
- Extremely low clamping voltage: 5.4 V for 6.5 A 8/20 μ s surge
- IEC 61000-4-4 robust up to 40 A into a 50 Ohm termination (2 kV)
- IEC 61000-4-5 (surge): $I_{PP} = 8.2$ A peak pulse (average measured)
- Extremely low diode capacitance $C_d = 0.19$ pF typical at 1.5 V
- ESD protection up to ± 15 kV according to IEC 61000-4-2
- Leadless ultra small DFN2510A-10 (SOT1176) surface mount package

3. Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals
- USB3.2 and HDMI2.1 data lines

4. Quick reference data

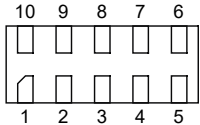
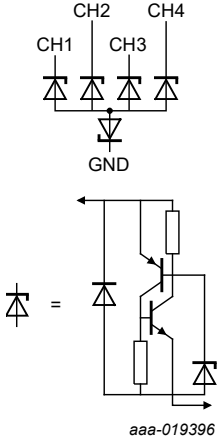
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage		-3.3	-	3.3	V
C_d	diode capacitance	$f = 1$ MHz; $V_R = 1.5$ V; $T_{amb} = 25$ °C	[1]	0.19	0.23	pF

[1] Measured on pin 1

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CH1	channel 1 ESD protection	 <p>Transparent top view</p> <p>DFN2510A-10 (SOT1176-2)</p>	 <p>aaa-019396</p>
2	CH2	channel 2 ESD protection		
3	GND	ground		
4	CH3	channel 3 ESD protection		
5	CH4	channel 4 ESD protection		
6	n.c.	not connected		
7	n.c.	not connected		
8	GND	ground		
9	n.c.	not connected		
10	n.c.	not connected		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUSB3CB4	DFN2510A-10	plastic, extremely thin small outline package; no leads; 10 terminals; body 1.0 x 2.5 x 0.5 mm	SOT1176-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PUSB3CB4	C4

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{RWM}	reverse standoff voltage			-3.3	3.3	V
I_{PPM}	rated peak pulse current	$t_p = 8/20 \mu s$	[1]	-6.5	6.5	A
T_{stg}	storage temperature			-65	150	°C
T_{amb}	ambient temperature			-40	125	°C
ESD maximum ratings						
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2]	-15	15	kV
		IEC 61000-4-2; air discharge	[2]	-15	15	kV

[1] Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC 61000-4-5.

[2] Device stressed with ten non-repetitive ESD pulses.

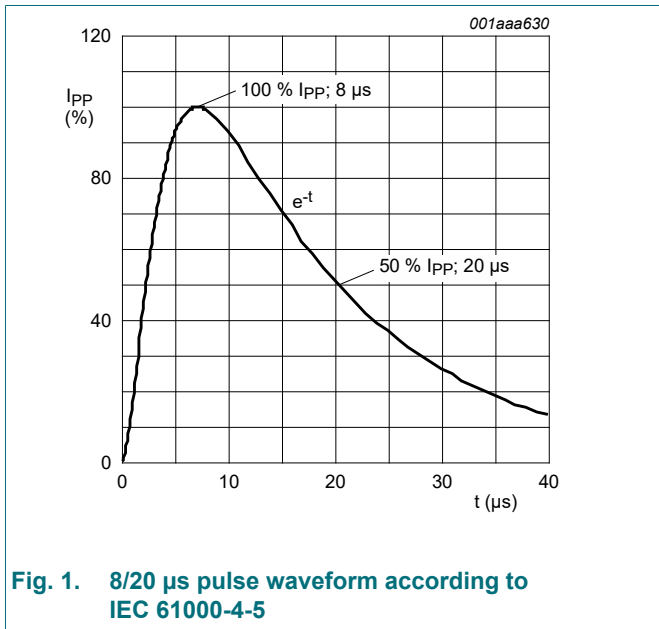


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

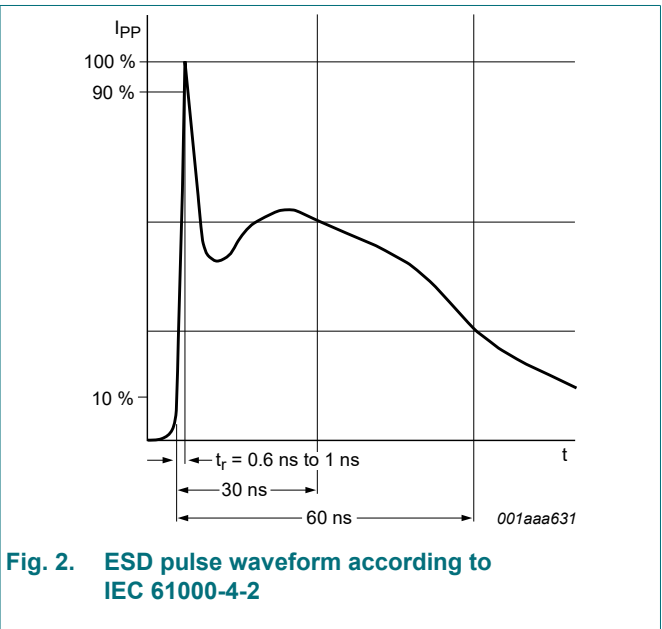


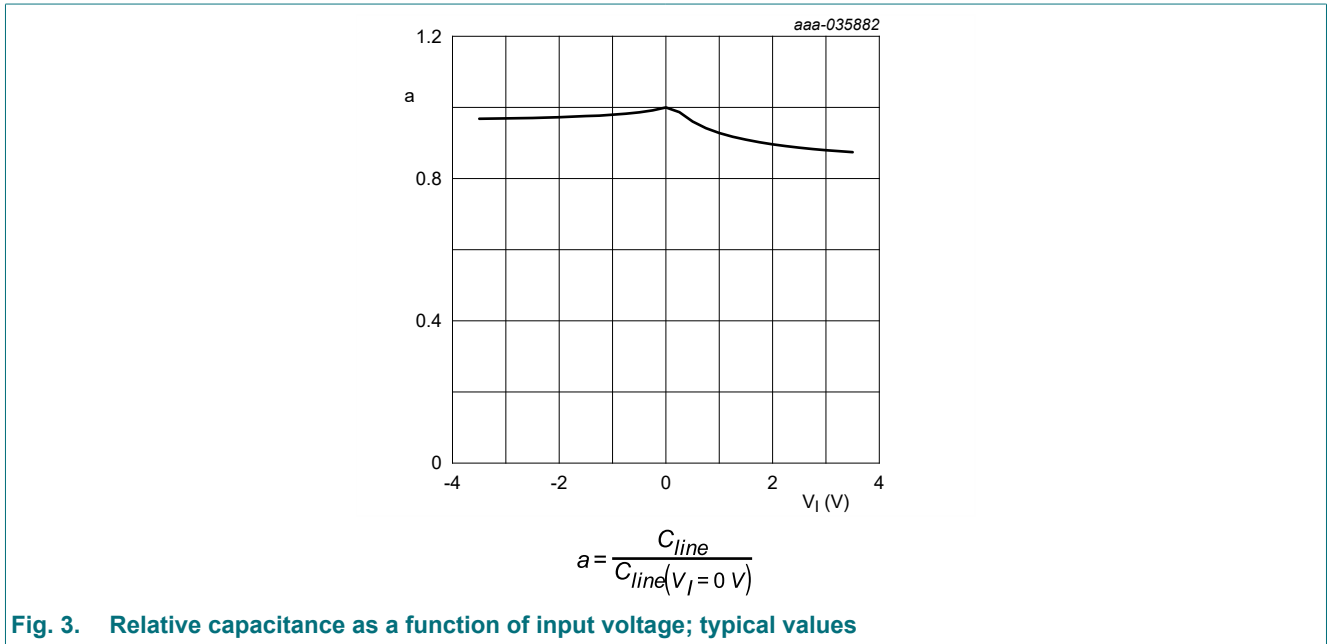
Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

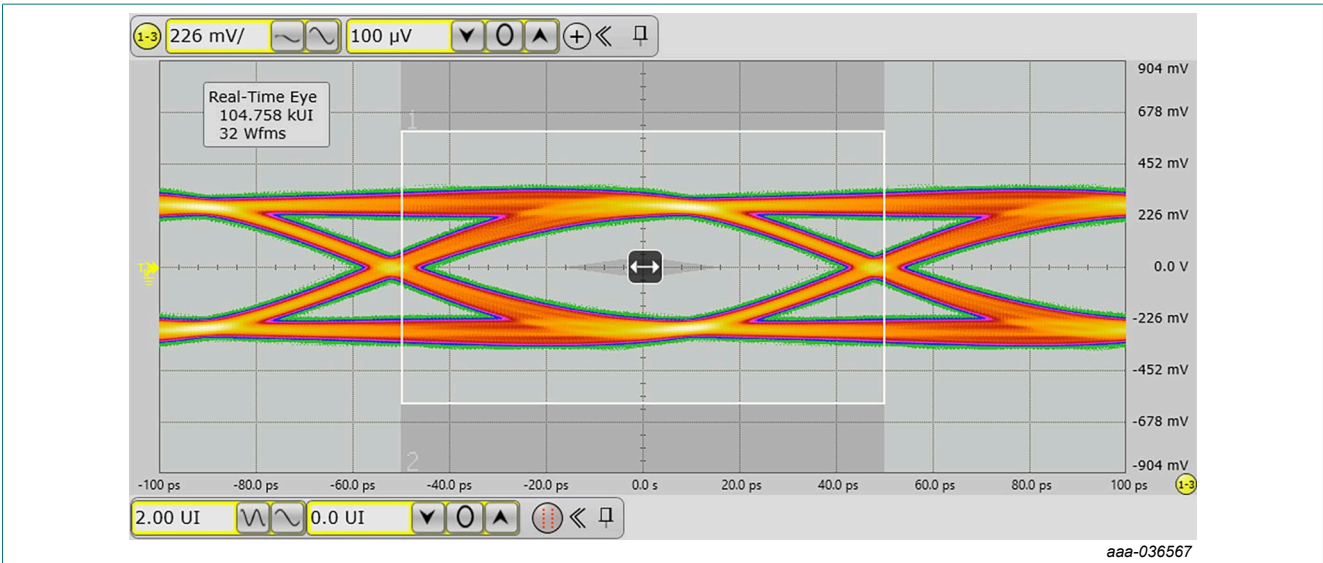
Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{BR}	breakdown voltage	$I_R = 1 \text{ mA}; T_{amb} = 25 \text{ }^\circ\text{C}$		5.5	9.1	11.5	V
V_{CL}	clamping voltage	$I_{TLP} = 8 \text{ A}; t_p = 100 \text{ ns}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1] [2]	-	5.2	-	V
		$I_{TLP} = 16 \text{ A}; t_p = 100 \text{ ns}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1] [2]	-	8	-	V
		$I_{PPM} = 6.5 \text{ A}; t_p = 8/20 \text{ } \mu\text{s}; T_{amb} = 25 \text{ }^\circ\text{C}$	[3]	-	5.4	-	V
I_{RM}	reverse leakage current	$V_{RWM} = 3.3 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$		-	1	100	nA
R_{dyn}	dynamic resistance	$I_R = 10 \text{ A}; t_p = 100 \text{ ns}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1] [2]	-	0.34	-	Ω
		$I_R = -10 \text{ A}; t_p = 100 \text{ ns}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1] [2]	-	0.34	-	Ω
C_d	diode capacitance	$f = 1 \text{ MHz}; V_R = 1.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	[4]	-	0.19	0.23	pF

- [1] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008
- [2] Measured on pin 2
- [3] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.
- [4] Measured on pin 1

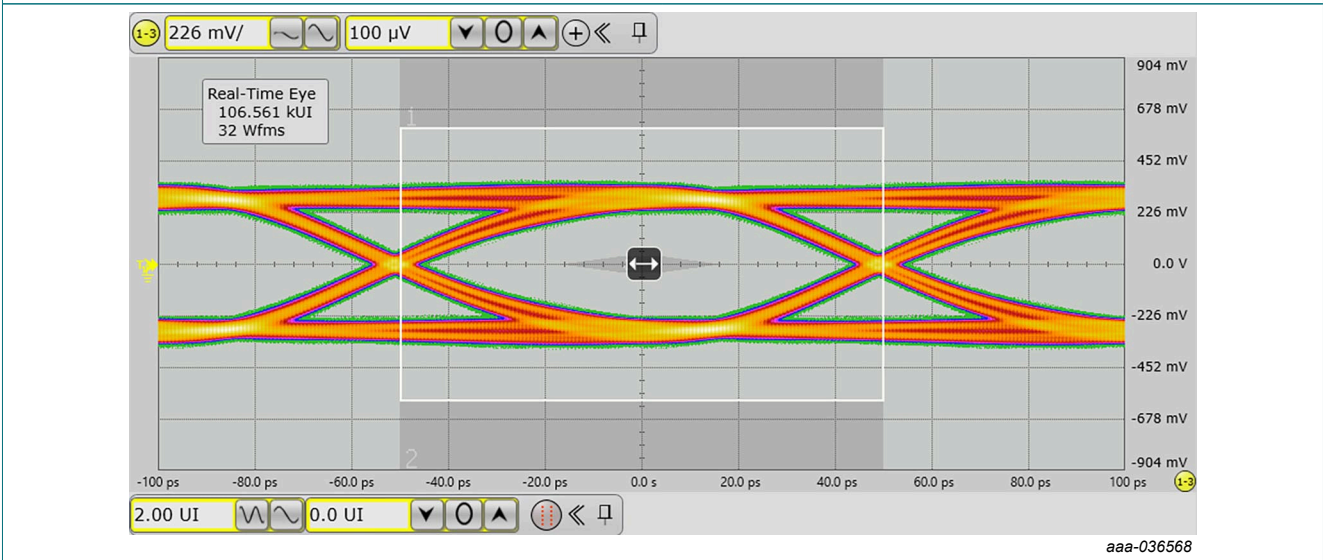


Extremely low capacitance bidirectional ESD protection diode array



Data rate: 10 Gbit/s

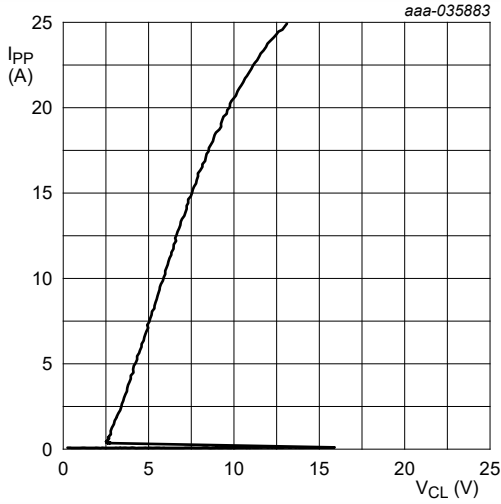
Fig. 4. USB3.2 eye diagram, PCB with device; typical values



Data rate: 10 Gbit/s

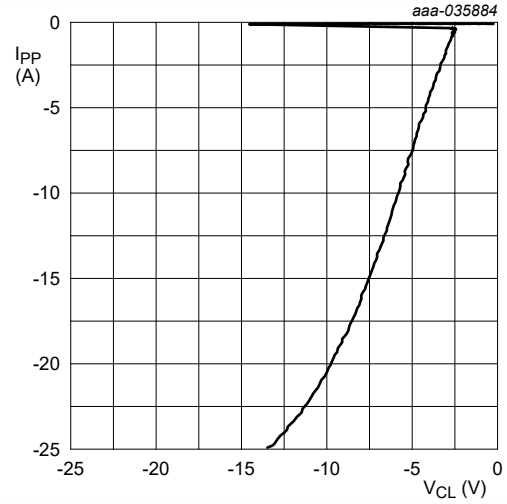
Fig. 5. USB3.2 eye diagram, PCB without device; typical values

Extremely low capacitance bidirectional ESD protection diode array



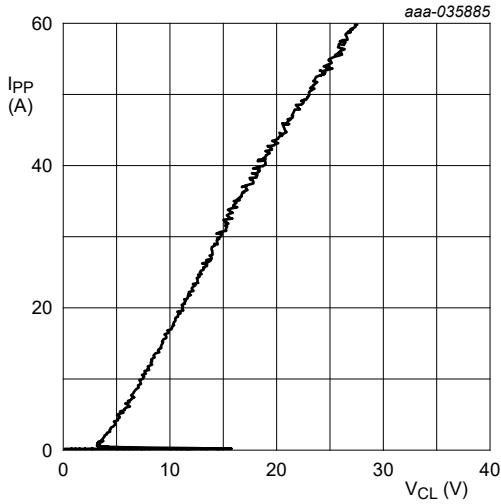
Transmission Line Pulse (TLP);
 $t_p = 100 \text{ ns}$; $t_r = 1 \text{ ns}$; pin 2

Fig. 6. Dynamic resistance with positive clamping; typical values



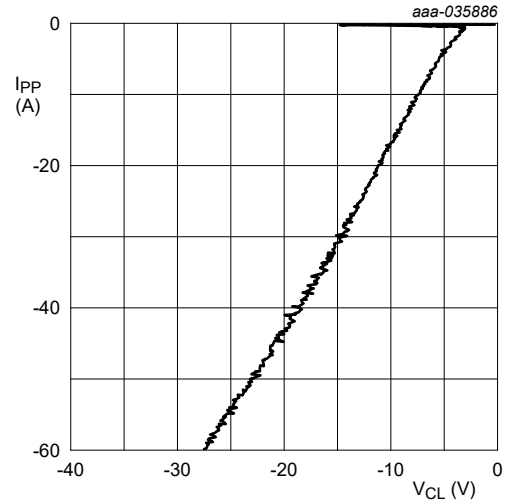
Transmission Line Pulse (TLP);
 $t_p = 100 \text{ ns}$; $t_r = 1 \text{ ns}$; pin 2

Fig. 7. Dynamic resistance with negative clamping; typical values



Very Fast Transmission Line Pulse (VF-TLP);
 $t_p = 5 \text{ ns}$; $t_r = 600 \text{ ps}$; pin 2

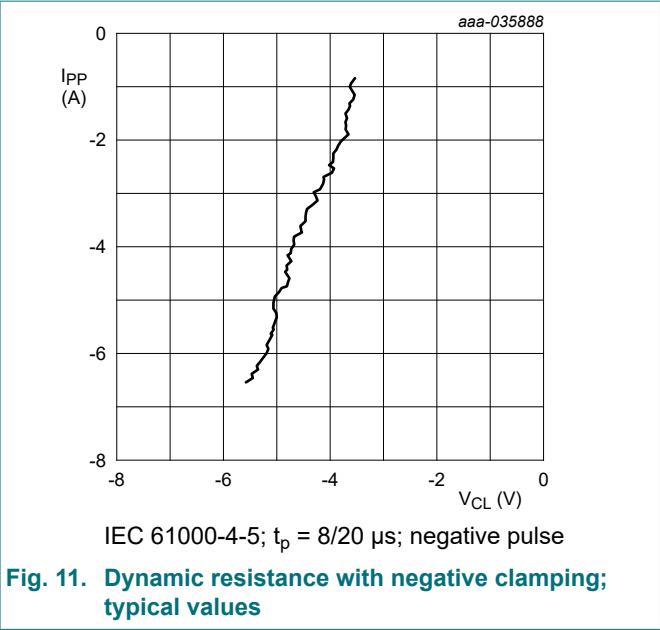
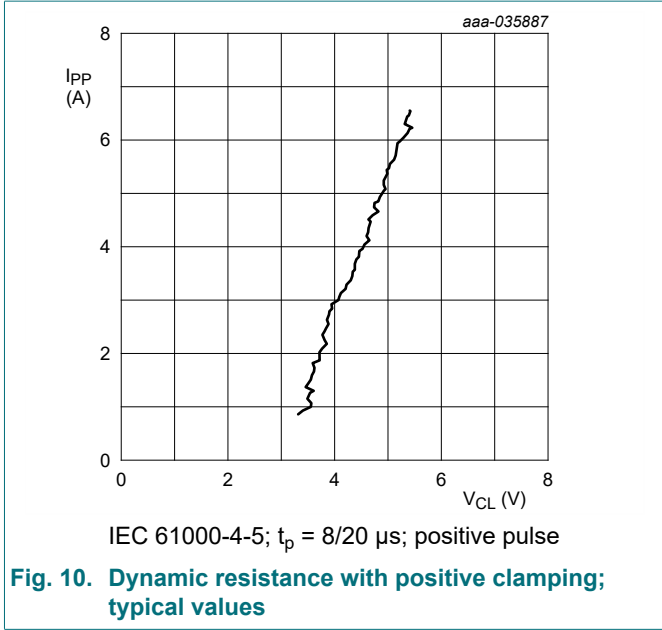
Fig. 8. Dynamic resistance with positive clamping; typical values



Very Fast Transmission Line Pulse (VF-TLP);
 $t_p = 5 \text{ ns}$; $t_r = 600 \text{ ps}$; pin 2

Fig. 9. Dynamic resistance with negative clamping; typical values

Extremely low capacitance bidirectional ESD protection diode array



10. Application information

The device is designed for the protection of four bidirectional data or signal lines from surge pulses and ESD damage.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Package outline

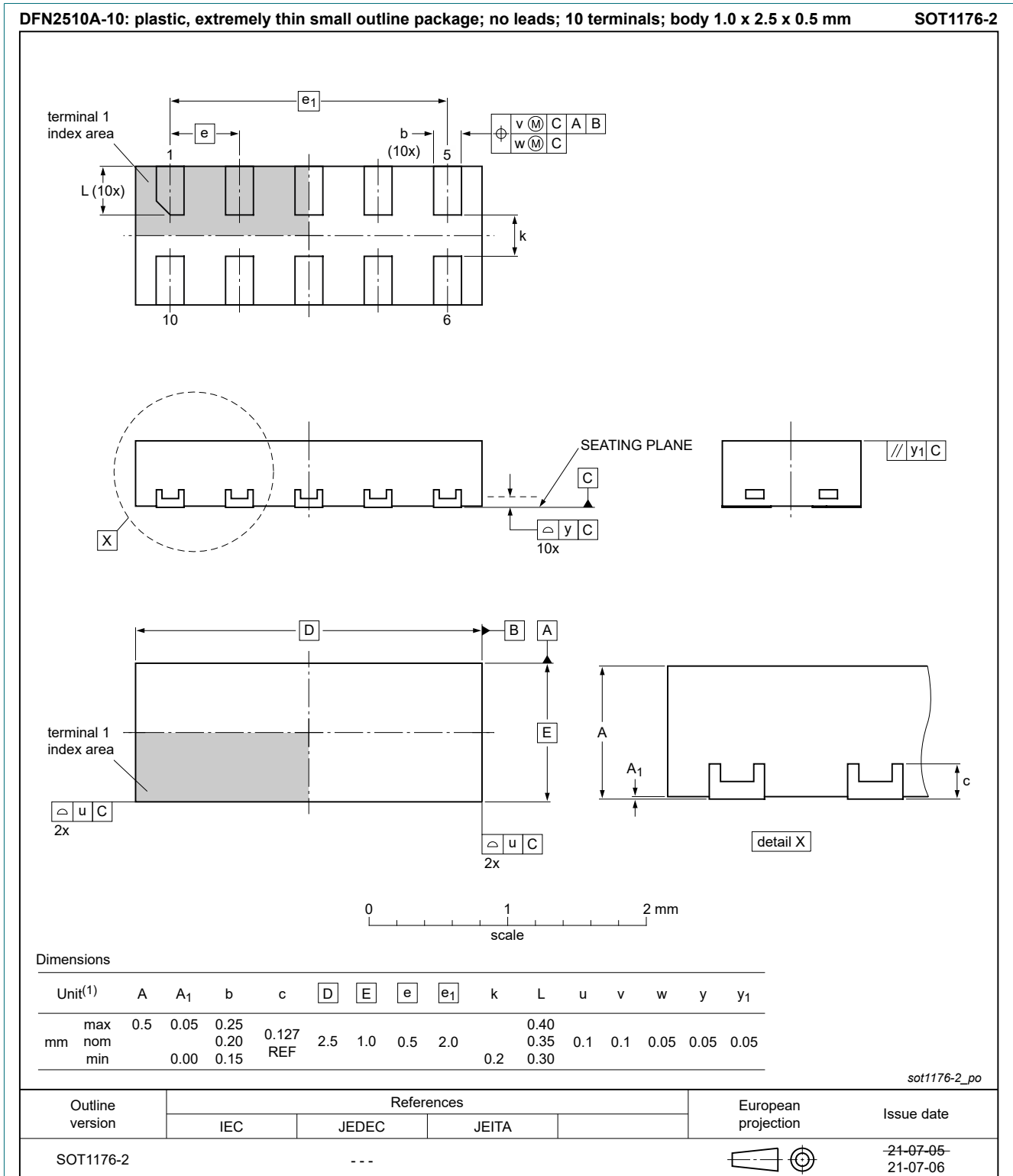


Fig. 12. Package outline DFN2510A-10 (SOT1176-2)

12. Soldering

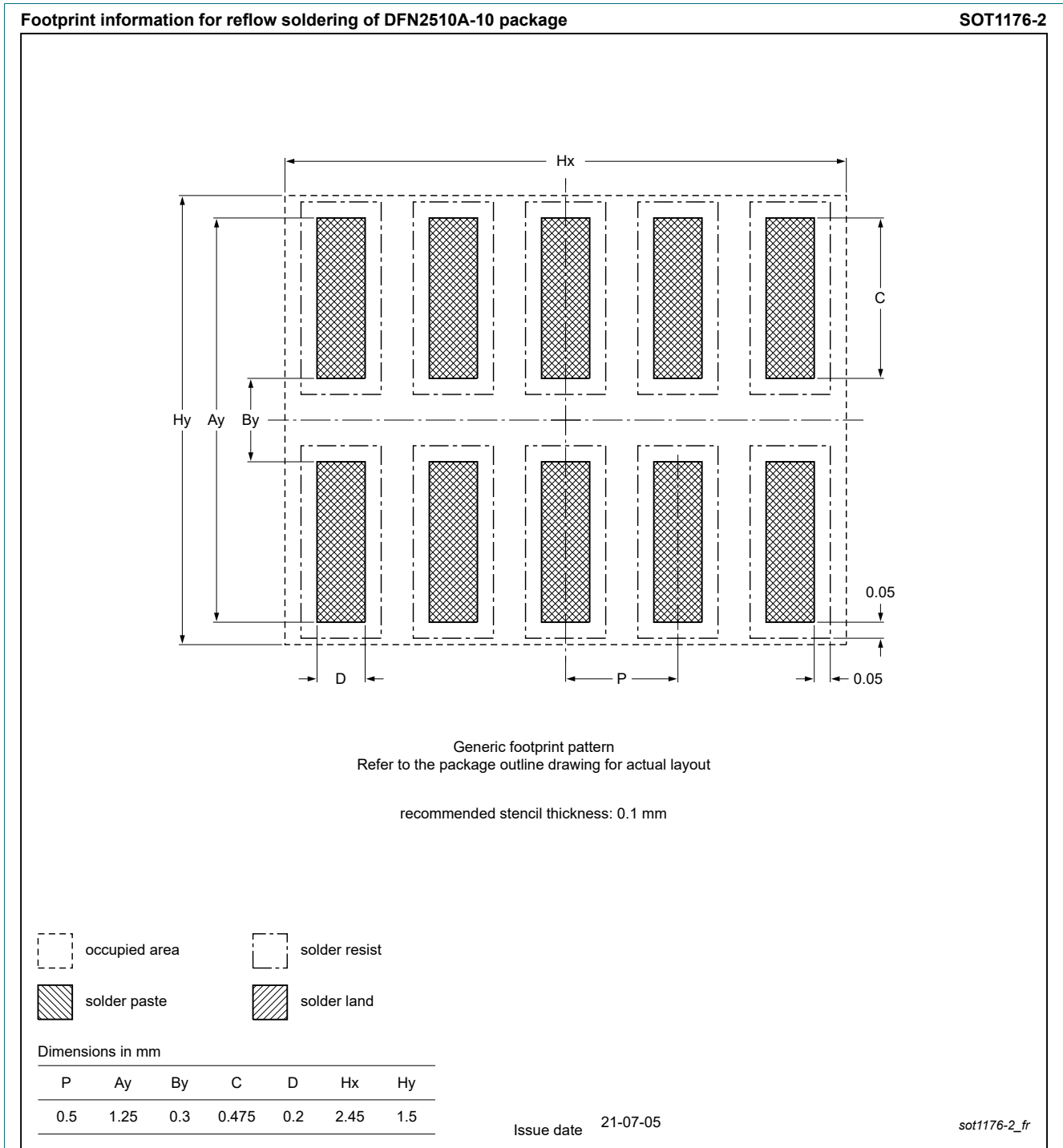


Fig. 13. Reflow soldering footprint for DFN2510A-10 (SOT1176-2)

13. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUSB3CB4 v.1	20230808	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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