



PSMNR90-80ASE

N-channel, 80 V, 0.9 mOhm, MOSFET with enhanced SOA in CCPAK1212 package

3 May 2024

Objective data sheet

1. General description

N-channel enhancement mode MOSFET in a CCPAK1212 package qualified to 175 °C. Part of Nexperia's Application Specific MOSFETs (ASFETs) for Hotswap and Soft Start. The PSMNR90-80ASE delivers very low R_{DSon} and enhanced safe operating area performance in a high-reliability copper-clip package (CCPAK1212).

PSMNR90-80ASE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn-on, low R_{DSon} to minimize I^2R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low R_{DSon} for low I^2R conduction losses
- CCPAK1212 package for applications that demand the highest performance and reliability

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	[1]	-	400	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	1.071	kW
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	0.71	0.9	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 175\text{ °C}$	-	[tbd]	[tbd]	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 40\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ °C}; \text{Fig. 2}$	-	46	-	nC
$Q_{G(tot)}$	total gate charge		[tbd]	286	[tbd]	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 129\text{ A}; V_{sup} \leq 80\text{ V}; R_{GS} = 50\text{ Ω}; V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; \text{unclamped}$	[2]	-	-	1781 mJ

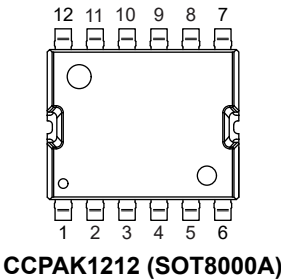
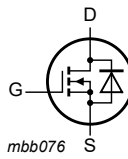
N-channel, 80 V, 0.9 mOhm, MOSFET with enhanced SOA in CCPAK1212 package

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 40\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 3	[3]	-	108	- nC

- [1] Max current will be demonstrated through application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test
- [3] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>CCPAK1212 (SOT8000A)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	S	source		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMNR90-80ASE	CCPAK1212	Plastic, surface mounted copper clip package (CCPAK1212); 13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body	SOT8000A

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	80	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	1.071	kW
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$	[1]	400	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$	-	282	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	1600	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	400	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	1600	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 129\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped	[2]	1781	mJ

- [1] Max current will be demonstrated through application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test

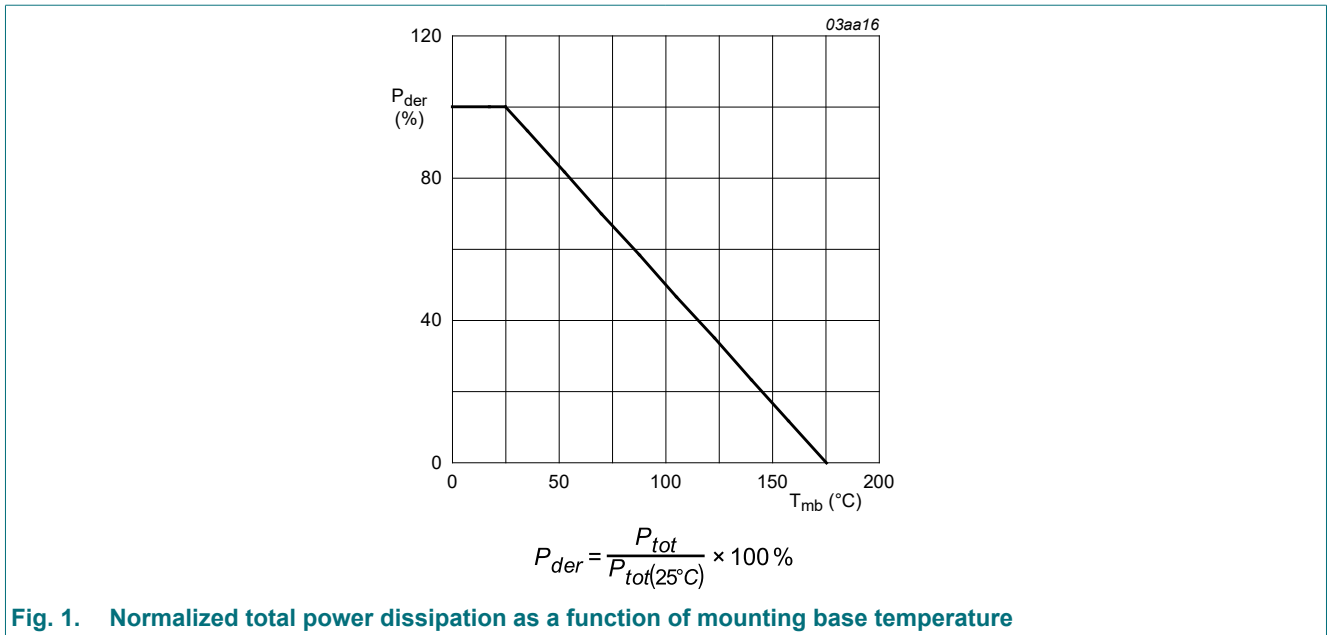


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	[tbd]	0.14	K/W

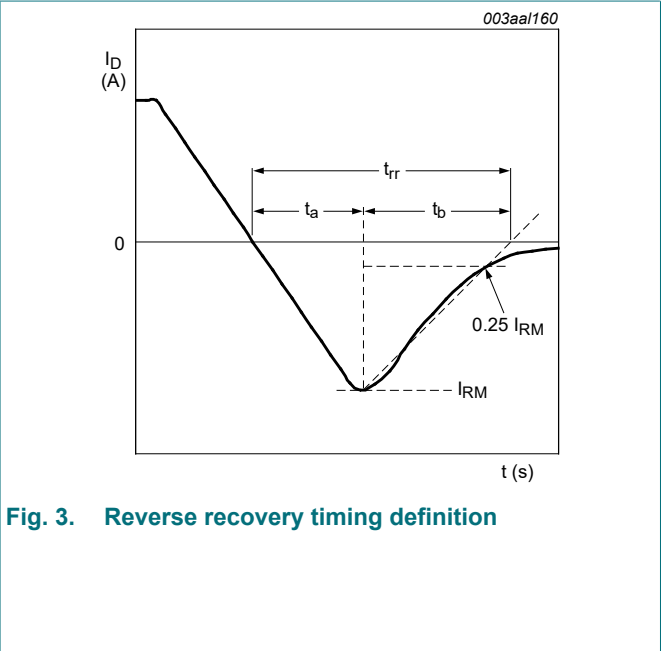
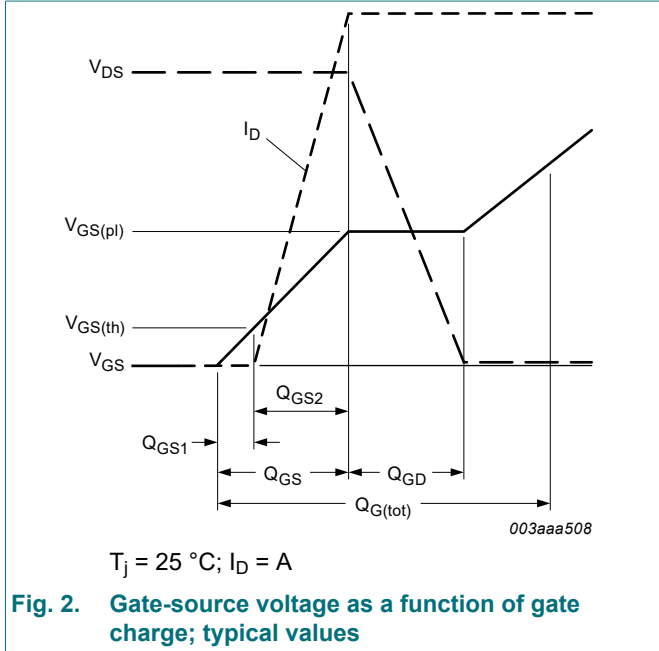
9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$	2	2.6	3.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.6	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	[tbd]	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	[tbd]	5	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	[tbd]	[tbd]	μA
I_{GSS}	gate leakage current	$V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
			-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$	-	0.71	0.9	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C$	-	[tbd]	[tbd]	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$	-	[tbd]	[tbd]	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	[tbd]	2.7	[tbd]	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C; \text{ Fig. 2}$	[tbd]	286	[tbd]	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$	-	148	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C; \text{ Fig. 2}$	[tbd]	115	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C$	-	68	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	47	-	nC
Q_{GD}	gate-drain charge	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V}; T_j = 25 \text{ }^\circ C; \text{ Fig. 2}$	-	46	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; T_j = 25 \text{ }^\circ C$	-	[tbd]	-	V
C_{iss}	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 0.5 \text{ MHz}; T_j = 25 \text{ }^\circ C$	[tbd]	24703	[tbd]	pF
C_{oss}	output capacitance		[tbd]	5434	[tbd]	pF
C_{rss}	reverse transfer capacitance		[tbd]	81	[tbd]	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 1.6 \text{ } \Omega; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	90	-	ns
t_r	rise time		-	75	-	ns
$t_{d(off)}$	turn-off delay time		-	169	-	ns
t_f	fall time		-	88	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	[tbd]	1	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}$; $dI_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$;	-	85	-	ns
Q_r	recovered charge	$V_{DS} = 40 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$; Fig. 3	[1]	108	-	nC

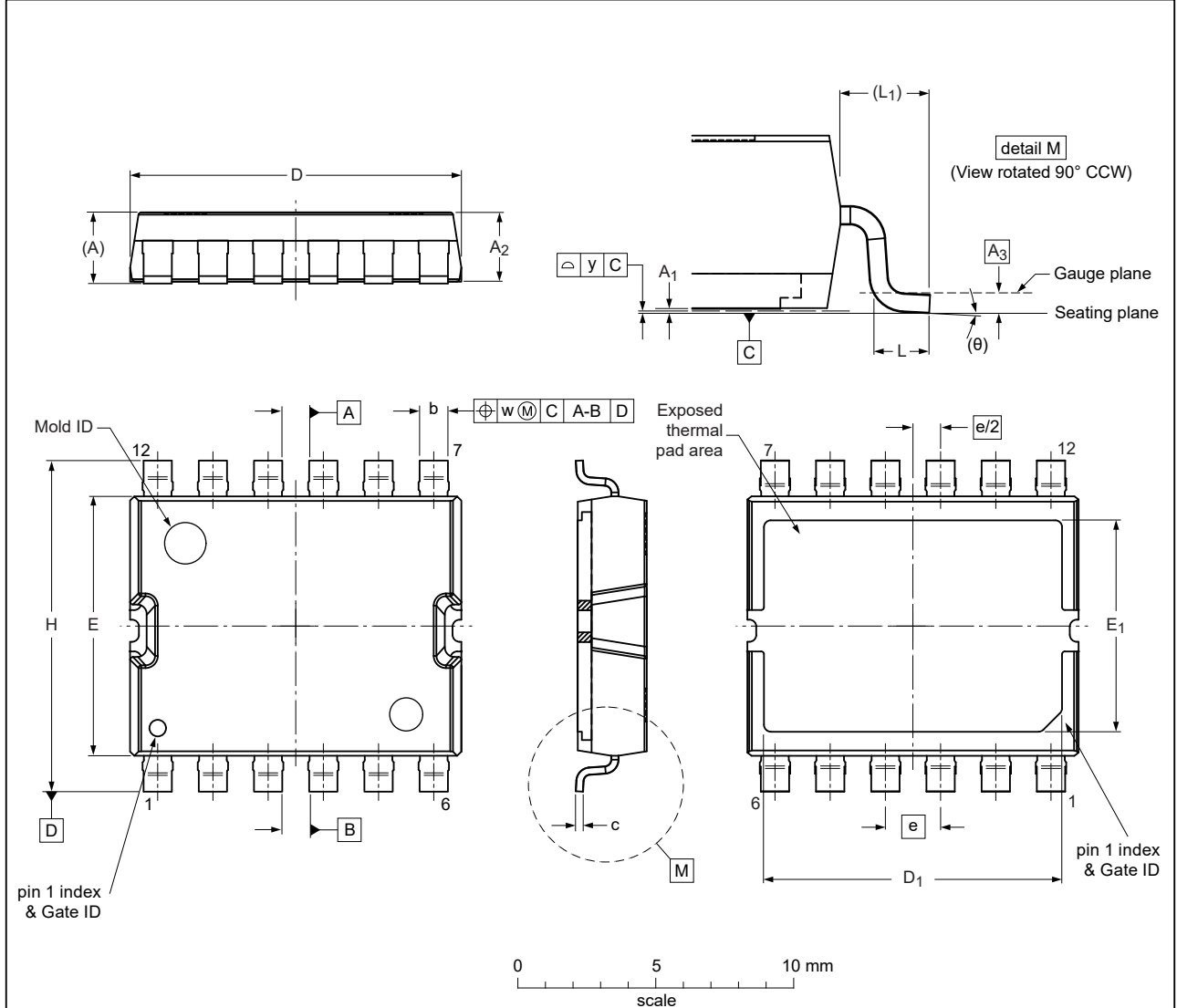
[1] includes capacitive recovery



10. Package outline

Plastic, surface mounted copper clip package (CCPAK1212);
13 terminals; 2.0 mm pitch, 12 mm x 12 mm x 2.5 mm body

SOT8000A



Dimensions (mm are the original dimensions)

Unit ⁽¹⁾	A(ref)	A ₁	A ₂	A ₃	b	c	D	D ₁	E	E ₁	e	H	L	L ₁ (ref)	w	y	θ(ref)	
max		0.13	2.65		1.12	0.30	12.15	10.95	9.55	7.40		12.15	1.0					
mm nom	2.75			0.25							2.0			1.3	0.20	0.1	4°	
min		0	2.4		0.93	0.22	11.85	10.65	9.25	7.10		11.85	0.6					

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included for dimension D.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included for dimension E.

sot8000a_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT8000A		MO-359			—23-12-12— 24-04-16

Fig. 4. Package outline CCPAK1212 (SOT8000A)

11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Contents

1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Limiting values.....	3
8. Thermal characteristics.....	3
9. Characteristics.....	4
10. Package outline.....	6
11. Legal information.....	7

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