



PSMNR90-50SLH

N-channel 50 V, 0.92 mOhm, 320 A logic level MOSFET in LFPAK88 using NextPower-S3 Schottky-Plus technology

8 January 2021

Objective data sheet

1. General description

320 Amp, logic level gate drive N-channel enhancement mode MOSFET in 175 °C LFPAK88 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance industrial applications.

2. Features and benefits

- 320 Amp continuous current capability
- LFPAK88 (8 x 8 mm) LFPAK-style low-stress exposed lead-frame for ultimate reliability, optimum soldering and easy solder-joint inspection
- Copper-clip and solder die attach for low package inductance and resistance, and high $I_{D(max)}$ rating
- Ideal replacement for D2PAK and 10 x 12 mm leadless package types
- Qualified to 175 °C
- Avalanche rated, 100 % tested
- Low Q_G , Q_{GD} and Q_{OSS} for high efficiency, especially at higher switching frequencies
- Superfast switching with soft body-diode recovery for low-spiking and ringing, recommended for low EMI designs
- Unique "SchottkyPlus" technology for Schottky-like switching performance and low I_{DSS} leakage
- Narrow $V_{GS(th)}$ rating for easy paralleling and improved current sharing
- Very strong linear-mode / safe operating area characteristics for safe and reliable switching at high-current conditions

3. Applications

- Brushless DC motor control
- Synchronous rectifier in high-power AC-to-DC applications, e.g. server power supplies
- Battery protection
- eFuse and load switch
- Hotswap / in-rush current management
- 10 cell lithium-ion battery applications (36 V – 42 V)

4. Quick reference data

Table 1. Quick reference data

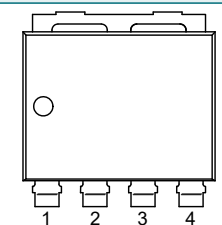
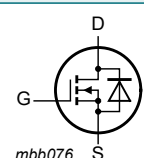
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	50	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	320	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	375	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	0.76	0.92	mΩ

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 25\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 4	-	24	[tbd]	nC
$Q_{G(\text{tot})}$	total gate charge	$I_D = 25\text{ A}$; $V_{DS} = 25\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 4	-	236	[tbd]	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LPAK88 (SOT1235)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR90-50SLH	LPAK88	plastic, single-ended surface-mounted package (LPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Limiting values

Table 4. Limiting values

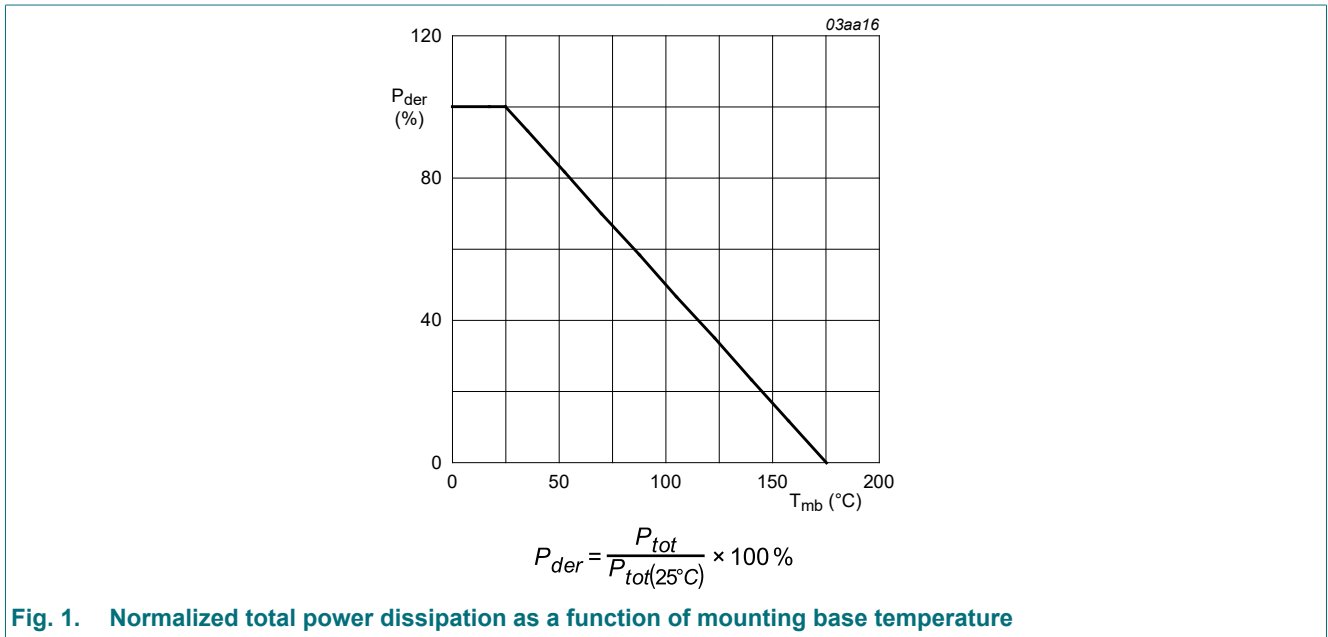
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	50	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	50	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{\text{mb}} = 25\text{ °C}$; Fig. 1	-	375	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{\text{mb}} = 25\text{ °C}$	-	320	A
		$V_{GS} = 10\text{ V}$; $T_{\text{mb}} = 100\text{ °C}$	-	305	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{\text{mb}} = 25\text{ °C}$	-	1726	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{\text{slid(M)}}$	peak soldering temperature		-	260	°C
Source-drain diode					
I_S	source current	$T_{\text{mb}} = 25\text{ °C}$	-	313	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{\text{mb}} = 25\text{ °C}$	-	1726	A

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Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 25\text{ A}$; $V_{sup} \leq 50\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped; $t_p = 8.7\text{ ms}$	[1]	-	7.1	J
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 50\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $R_{GS} = 50\ \Omega$	[1]	-	[tbd]	A

[1] Protected by 100% test

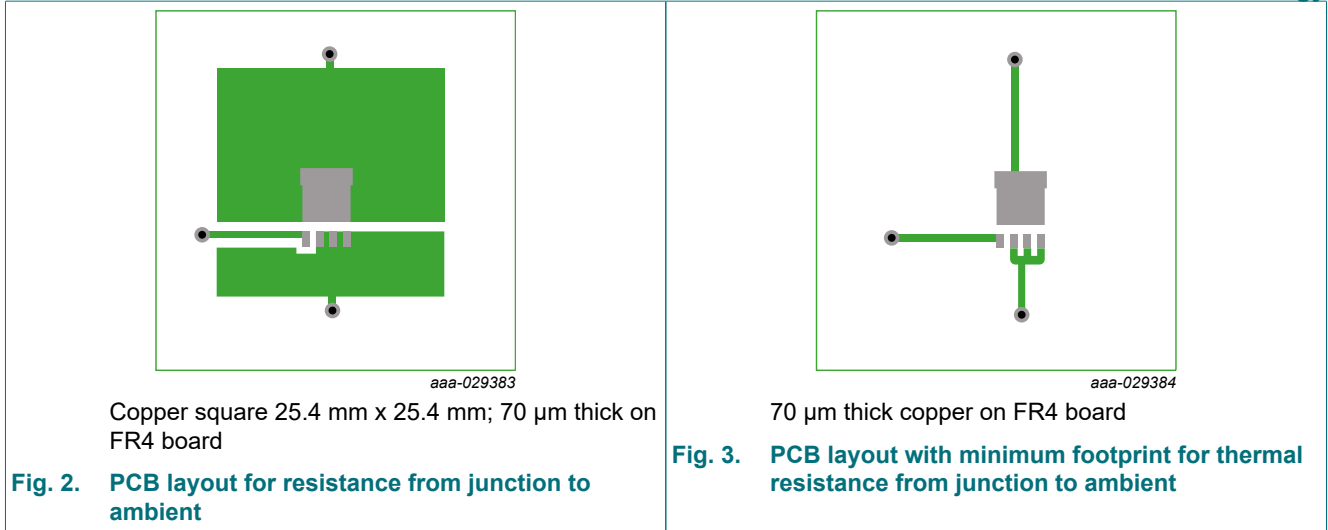


8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	0.35	0.4	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 2	-	35	-	K/W
		Fig. 3	-	70	-	K/W

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9. Characteristics

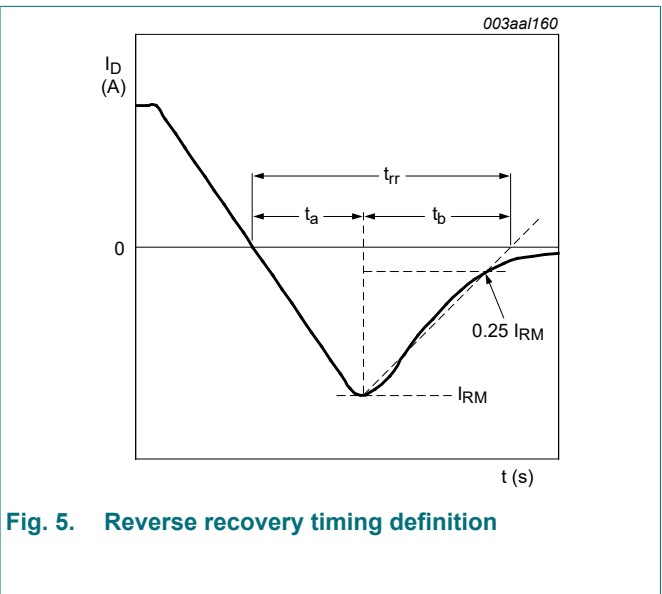
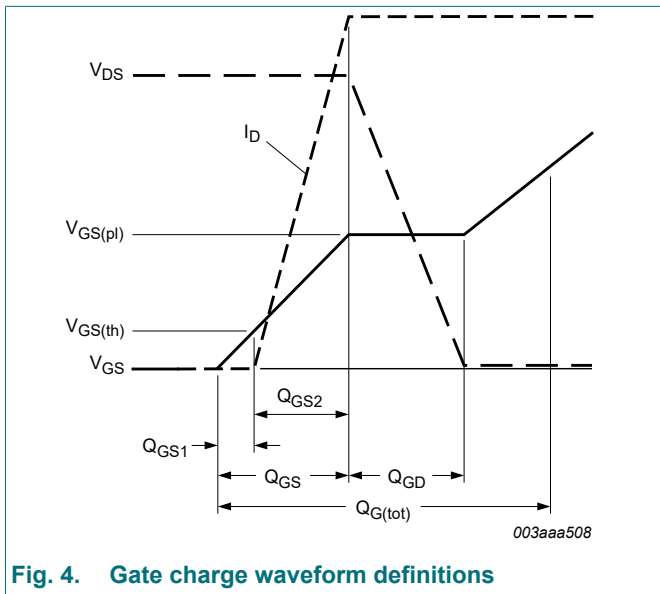
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	50	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	45	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	1.2	1.78	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	[tbd]	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	[tbd]	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
		$V_{GS} = -16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$	-	0.76	0.92	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C$	-	-	[tbd]	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$	-	[tbd]	[tbd]	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 25 \text{ A}; T_j = 150 \text{ }^\circ C$	-	-	[tbd]	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	[tbd]	[tbd]	[tbd]	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 25 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 4	-	107	[tbd]	nC
		$I_D = 25 \text{ A}; V_{DS} = 25 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 4	-	236	[tbd]	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	125	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 25 \text{ V}; V_{GS} = 4.5 \text{ V};$ Fig. 4	-	34	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	23	[tbd]	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	11	[tbd]	nC
Q_{GD}	gate-drain charge		-	24	[tbd]	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}$; $V_{DS} = 25\text{ V}$; Fig. 4	-	[tbd]	-	V	
C_{iss}	input capacitance	$V_{DS} = 25\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$	-	16553	[tbd]	pF	
C_{oss}	output capacitance		-	1583	[tbd]	pF	
C_{rss}	reverse transfer capacitance		-	418	[tbd]	pF	
$t_{d(on)}$	turn-on delay time	$V_{DS} = 25\text{ V}$; $R_L = 1\ \Omega$; $V_{GS} = 4.5\text{ V}$; $R_{G(ext)} = 5\ \Omega$	-	[tbd]	-	ns	
t_r	rise time		-	[tbd]	-	ns	
$t_{d(off)}$	turn-off delay time		-	[tbd]	-	ns	
t_f	fall time		-	[tbd]	-	ns	
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$	-	93	-	nC	
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$	-	0.75	1	V	
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; Fig. 5	-	[tbd]	-	ns	
Q_r	recovered charge		[1]	-	[tbd]	-	nC
t_a	reverse recovery rise time		-	-	[tbd]	-	ns
t_b	reverse recovery fall time		-	-	[tbd]	-	ns

[1] includes capacitive recovery



10. Package outline

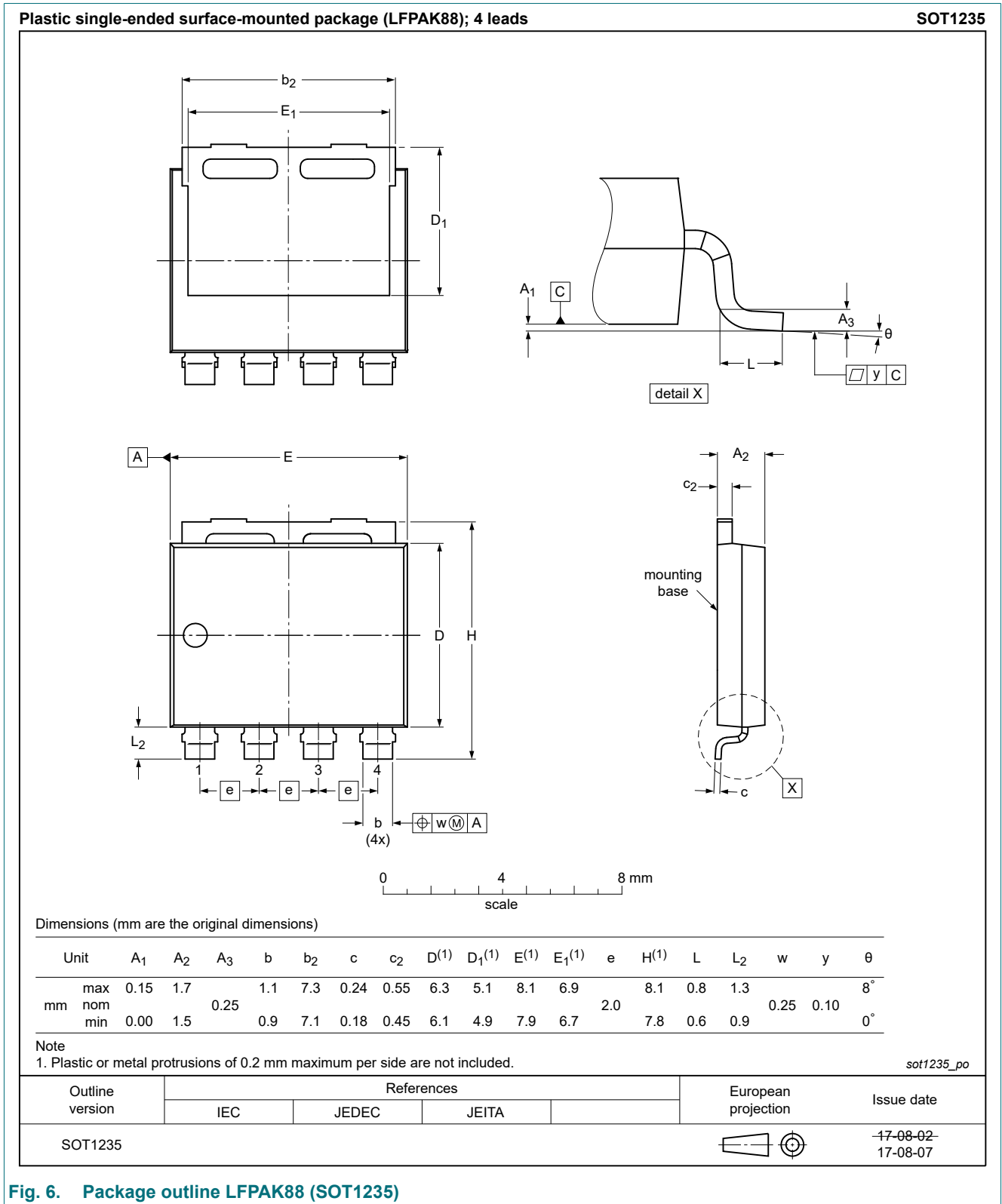


Fig. 6. Package outline LPAK88 (SOT1235)

11. Soldering

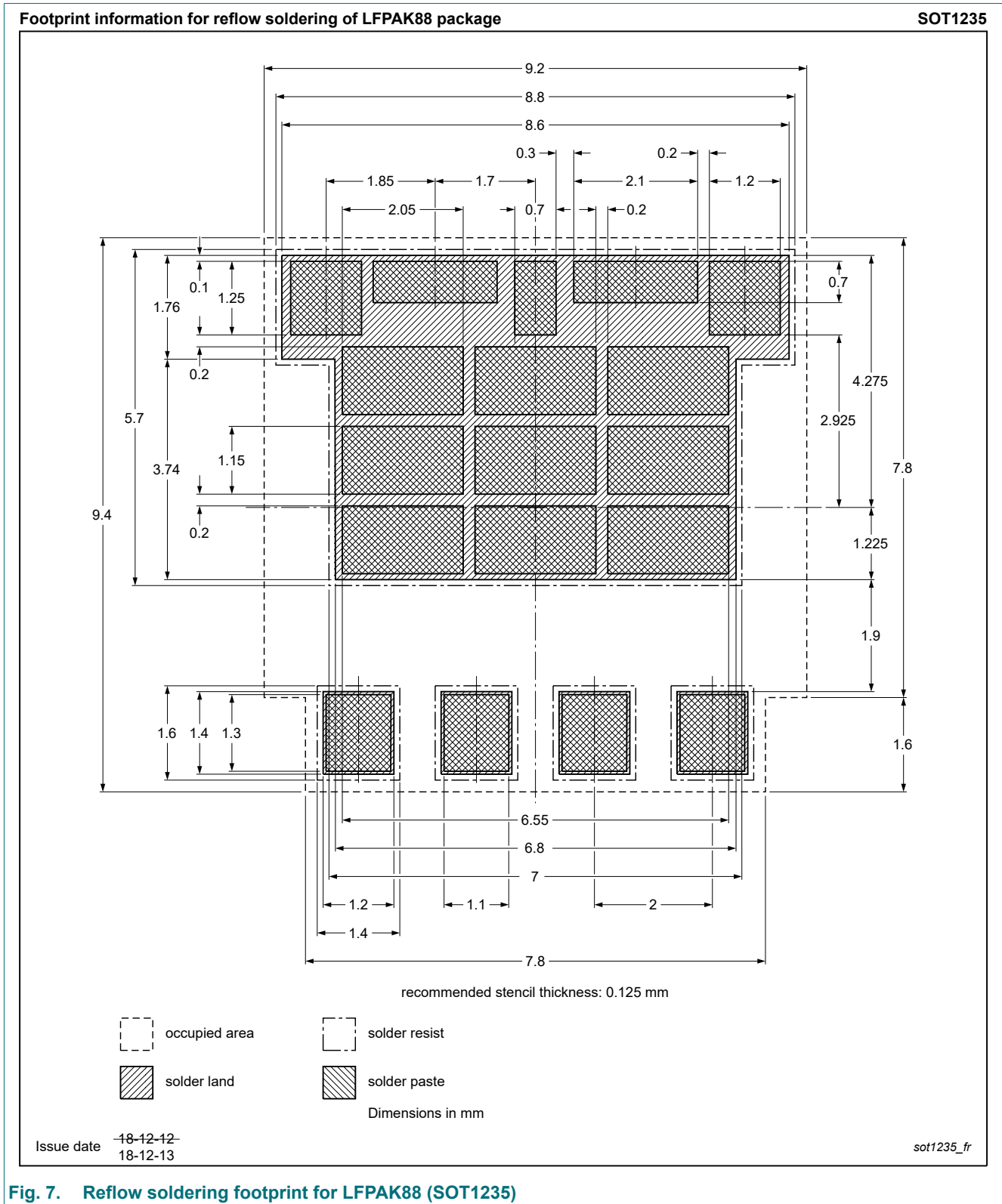


Fig. 7. Reflow soldering footprint for LPAK88 (SOT1235)

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12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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