



# PSMNR90-40YSN

N-channel 40 V, 0.97 mOhm, ASFET for Battery System in LFPAK56E

12 September 2024

Product data sheet

## 1. General description

ASFET for Battery System applications, characterized by low  $R_{DS(on)}$  and strong SOA capability for reduced  $I^2R$  conduction losses. ASFETs deliver high efficiency, reduced heat generation and superior handling of inrush current during transient and fault conditions.

## 2. Features and benefits

- 320 A continuous  $I_{D(max)}$
- Strong SOA capability
- Avalanche rated, 100% tested at  $I_{AS} = 190$  A
- High reliability LFPAK (Power-SO8) package, qualified to 175 °C
- LFPAK copper clip
- LFPAK gull wing lead

## 3. Applications

- Battery management systems (BMS)
- eFuse
- Load-switch
- BLDC motor control
- High-performance power supply
- High-performance synchronous rectification

## 4. Quick reference data

Table 1. Quick reference data

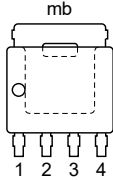
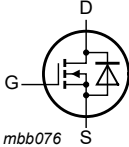
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_J \leq 175\text{ °C}$		-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	[1]	-	-	320	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>		-	-	268	W
<b>Static characteristics</b>							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 25\text{ A}$ ; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 12</a>		0.57	0.81	0.97	mΩ
<b>Dynamic characteristics</b>							
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}$ ; $V_{DS} = 32\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		12	42	72	nC
<b>Source-drain diode</b>							
$Q_r$	recovered charge	$I_S = 25\text{ A}$ ; $dI_S/dt = -100\text{ A/μs}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 20\text{ V}$ ; $T_J = 25\text{ °C}$ ; <a href="#">Fig. 18</a>	[2]	-	24	-	nC

[1] 320 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR90-40YSN	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR90-40YSN	N9040S

8. Limiting values

Table 5. Limiting values

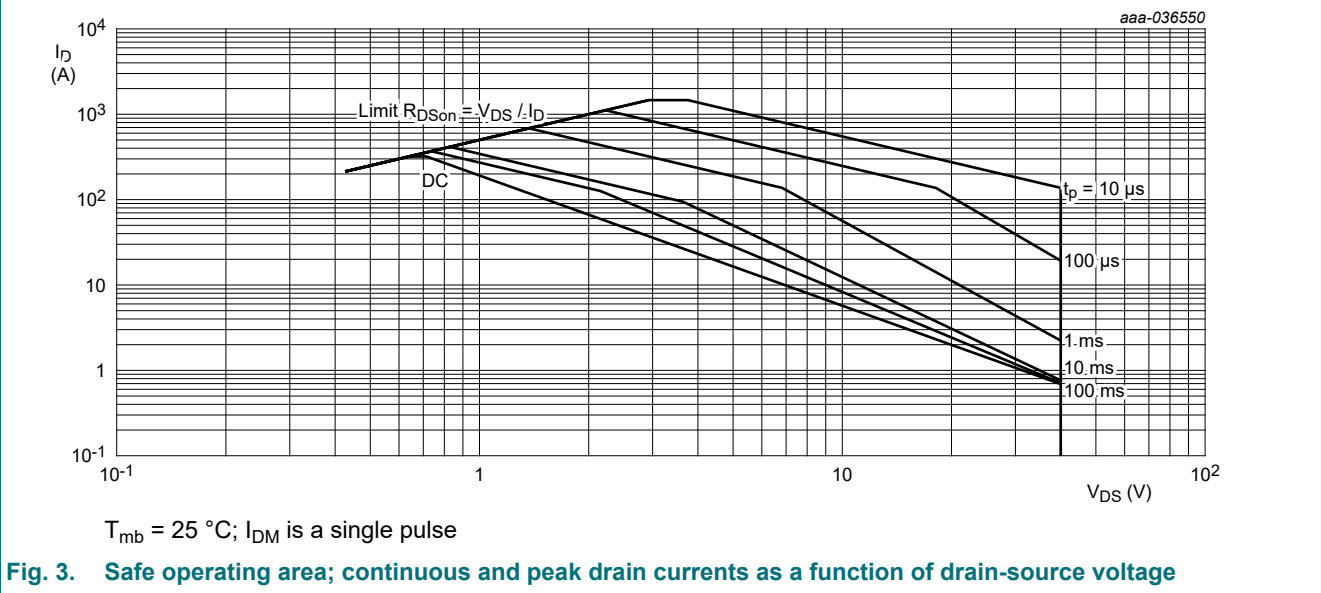
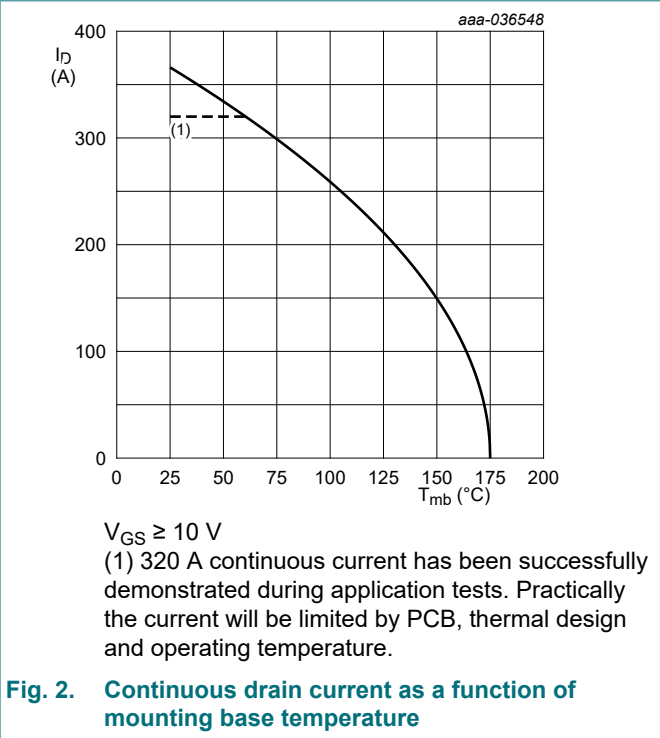
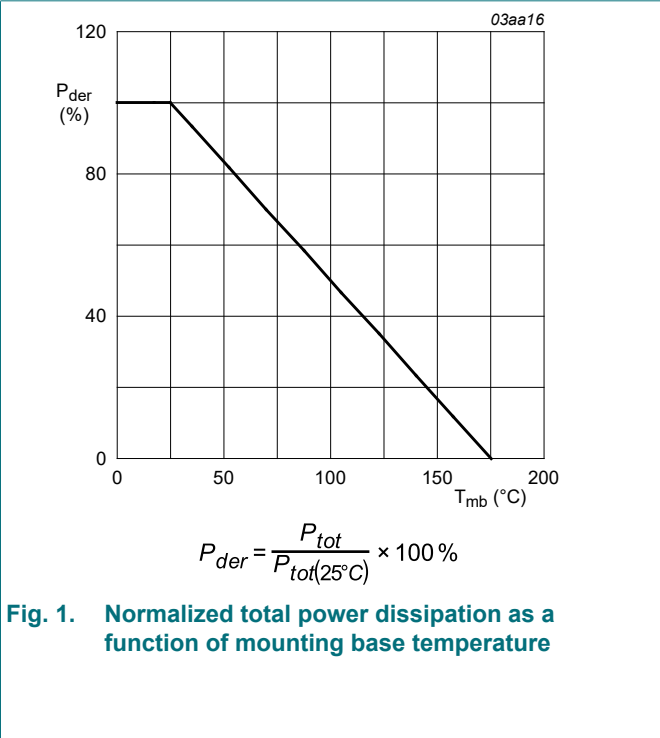
In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25\text{ }^{\circ}\text{C}$  unless otherwise stated.

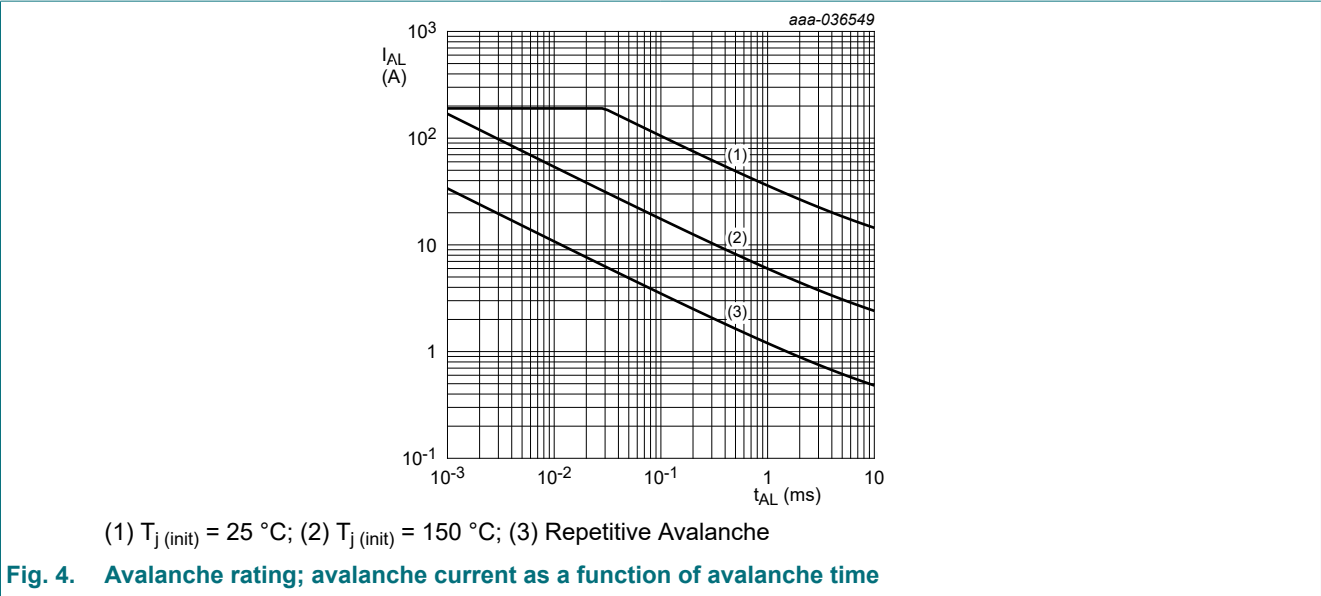
Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ }^{\circ}\text{C} \leq T_j \leq 175\text{ }^{\circ}\text{C}$		-	40	V
$V_{DSM}$	peak drain-source voltage	$t_p \leq 20\text{ ns}$ ; $f \leq 500\text{ kHz}$ ; $E_{DS(AL)} \leq 200\text{ nJ}$ ; single pulse		-	45	V
$V_{GS}$	gate-source voltage			-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^{\circ}\text{C}$ ; Fig. 1		-	268	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ }^{\circ}\text{C}$ ; Fig. 2	[1]	-	320	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ }^{\circ}\text{C}$ ; Fig. 2		-	259	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ }^{\circ}\text{C}$ ; Fig. 3		-	1465	A
$T_{stg}$	storage temperature			-55	175	$^{\circ}\text{C}$
$T_j$	junction temperature			-55	175	$^{\circ}\text{C}$
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 40\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $R_{GS} = 50\text{ }\Omega$	[2]	-	190	A
Source-drain diode						
$I_S$	source current	$T_{mb} = 25\text{ }^{\circ}\text{C}$		-	268	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ }^{\circ}\text{C}$		-	1465	A

N-channel 40 V, 0.97 mOhm, ASFET for Battery System in LPAK56E

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 67.5 A; V <sub>sup</sub> ≤ 40 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped; t <sub>p</sub> = 252 μs; Fig. 4	[2]	-	443	mJ

- [1] 320 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test.

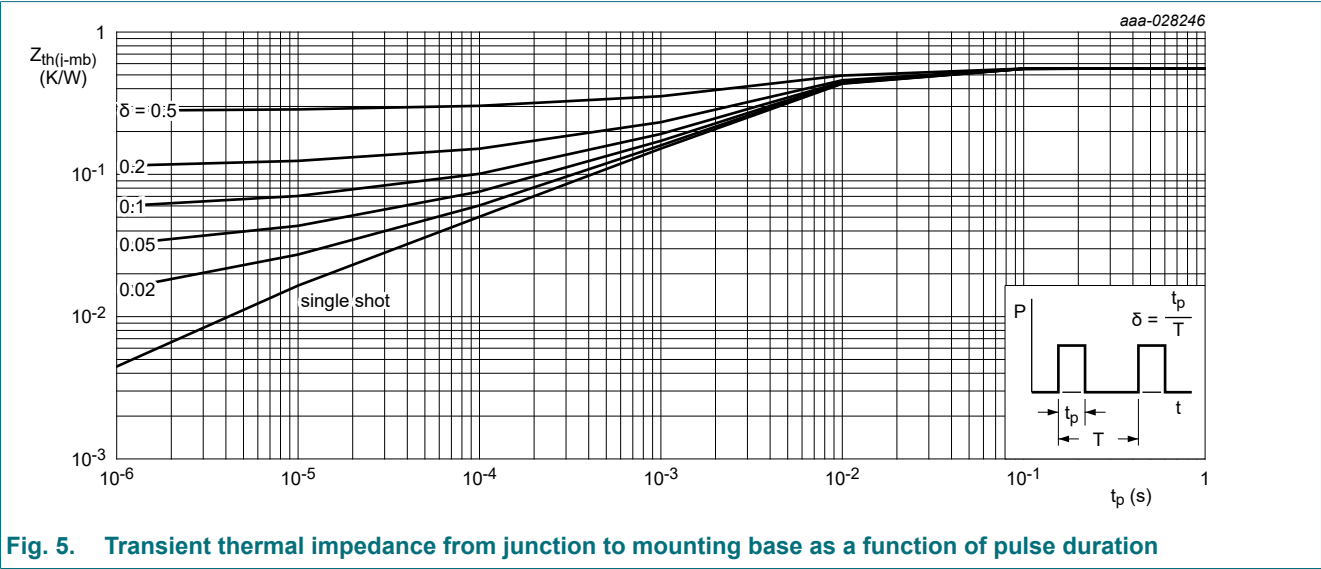


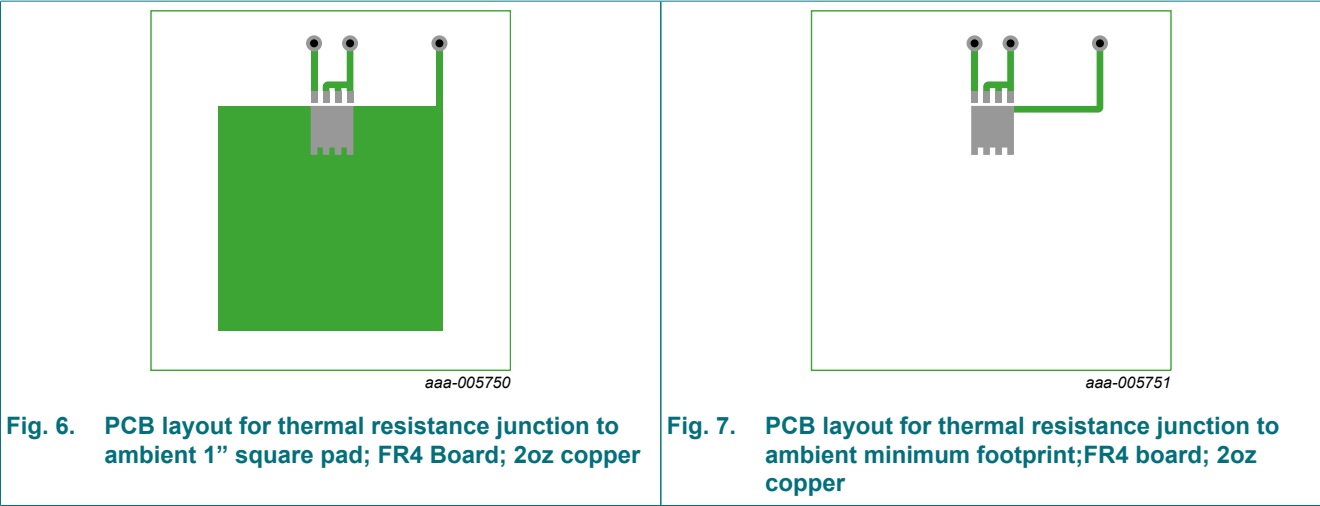


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.48	0.56	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	50	-	K/W
		Fig. 7	-	125	-	K/W





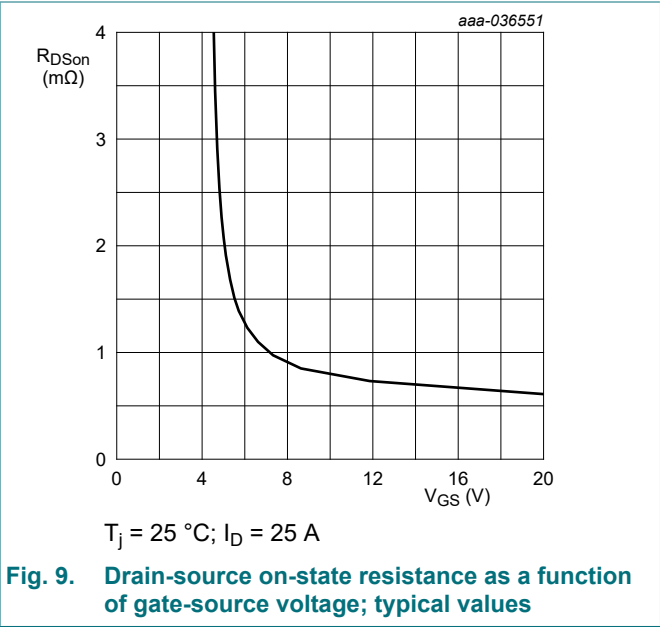
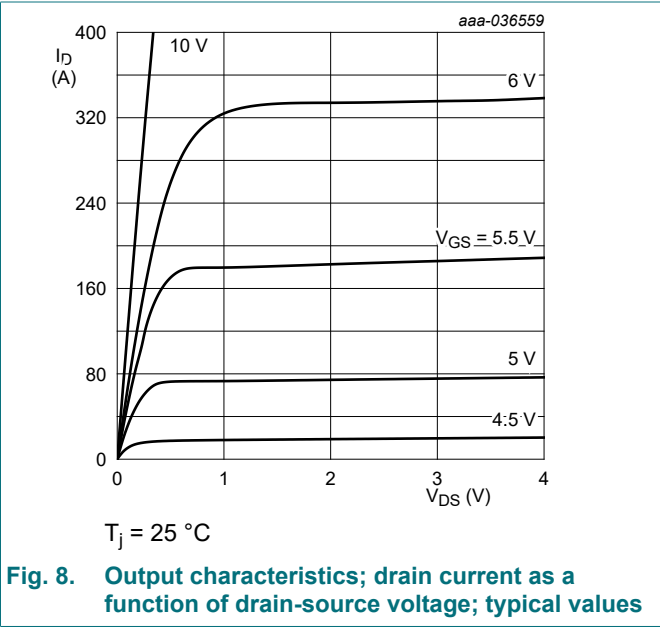
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C		40	43	-	V
		I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>J</sub> = -55 °C		36	40	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>J</sub> = 25 °C; <a href="#">Fig. 11</a>		2.4	3	3.6	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>J</sub> = -55 °C		-	3.5	-	V
		I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>J</sub> = 175 °C		-	1.9	-	V
ΔV <sub>GS(th)</sub> /ΔT	gate-source threshold voltage variation with temperature	25 °C ≤ T <sub>J</sub> ≤ 175 °C		-	-7.2	-	mV/K
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C		-	0.1	1	μA
		V <sub>DS</sub> = 16 V; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 125 °C		-	1.1	10	μA
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C		-	2	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C		-	2	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 25 °C; <a href="#">Fig. 12</a>		0.57	0.81	0.97	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 105 °C; <a href="#">Fig. 13</a>		0.77	1.15	1.46	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 125 °C; <a href="#">Fig. 13</a>		0.84	1.25	1.6	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 175 °C; <a href="#">Fig. 13</a>		1	1.52	2	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>J</sub> = 25 °C		0.2	0.63	1.6	Ω
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		81	135	189	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; T <sub>J</sub> = 25 °C		-	107	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; V <sub>GS</sub> = 10 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		14	26	38	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge			10	19	28	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge			4	7.6	11	nC
Q <sub>GD</sub>	gate-drain charge			12	42	72	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 32 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>		-	4.1	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 25 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>J</sub> = 25 °C; <a href="#">Fig. 16</a>		4552	7587	10622	pF
C <sub>oss</sub>	output capacitance			1166	1666	2166	pF
C <sub>rss</sub>	reverse transfer capacitance			252	631	1010	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 1.2 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>J</sub> = 25 °C		-	25	-	ns
t <sub>r</sub>	rise time			-	49	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	79	-	ns
t <sub>f</sub>	fall time			-	58	-	ns
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 17</a>		-	0.79	1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 20 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 18</a>		-	34	-	ns
Q <sub>r</sub>	recovered charge		[1]	-	24	-	nC

[1] includes capacitive recovery



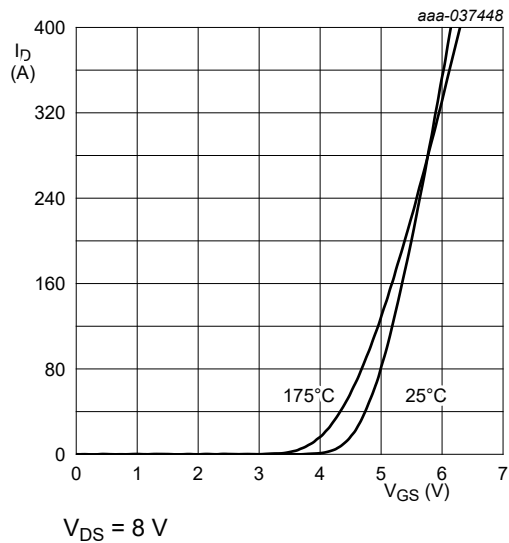


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

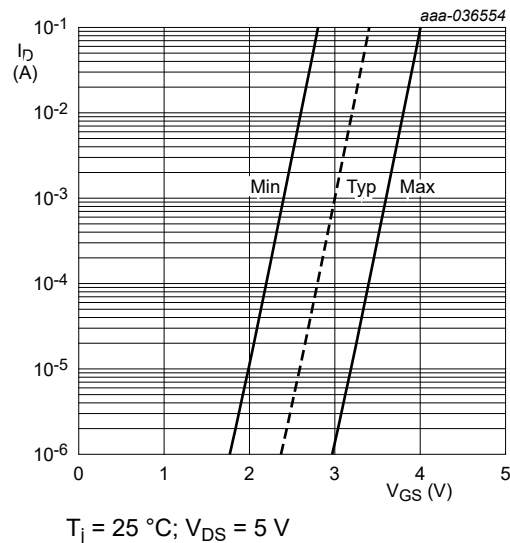


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

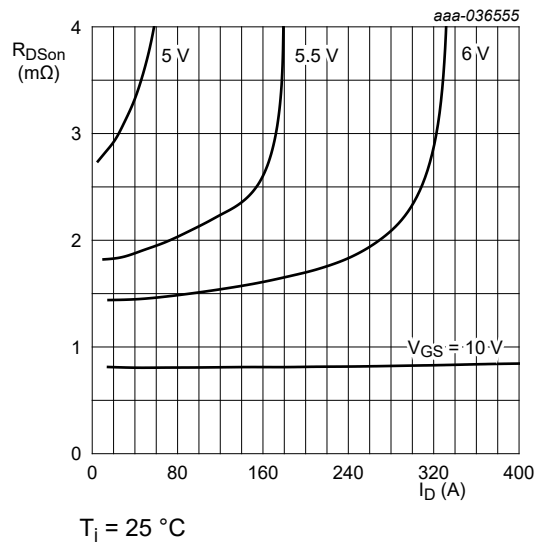


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

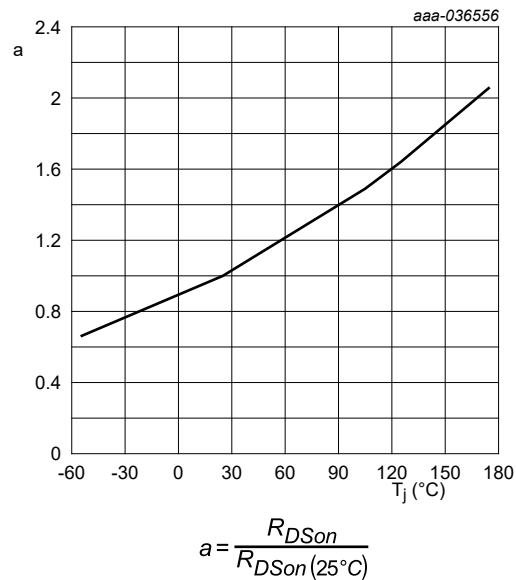


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

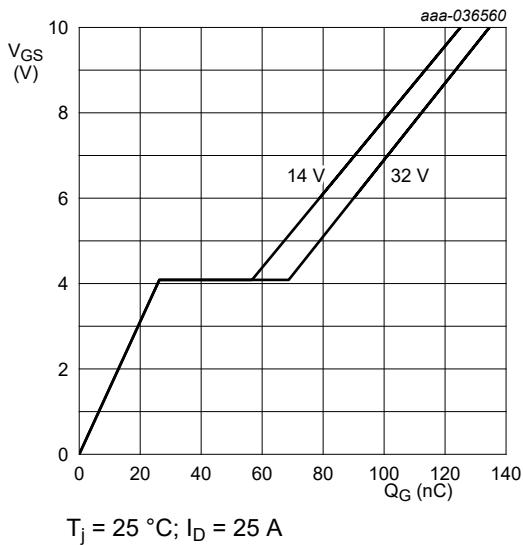


Fig. 14. Gate-source voltage as a function of gate charge; typical values

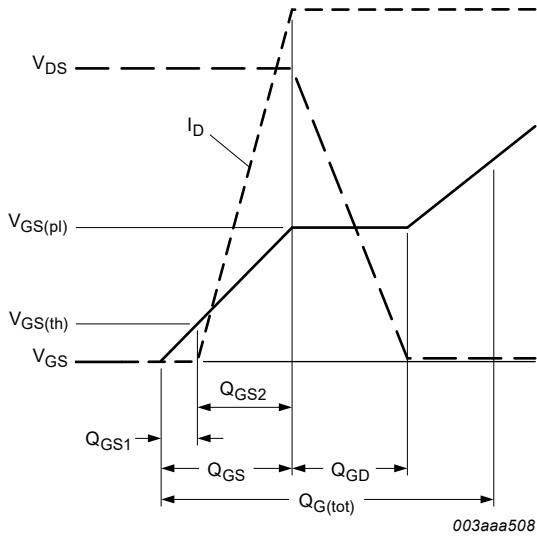


Fig. 15. Gate charge waveform definitions

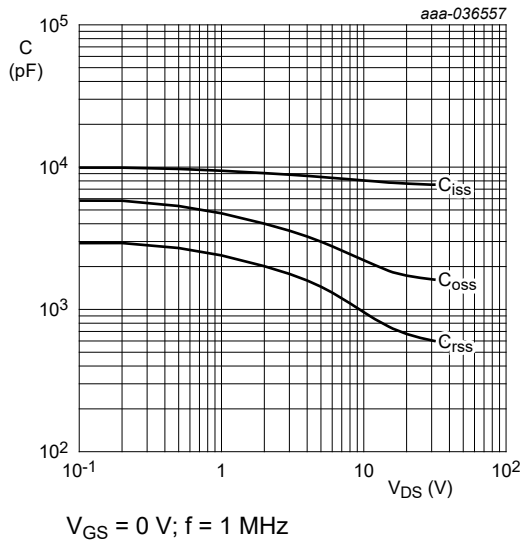


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

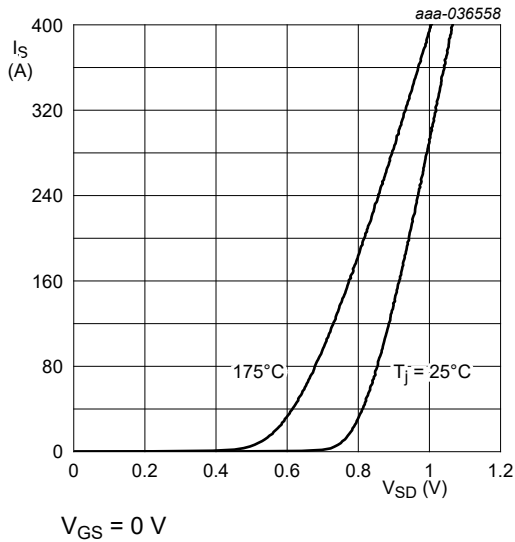


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

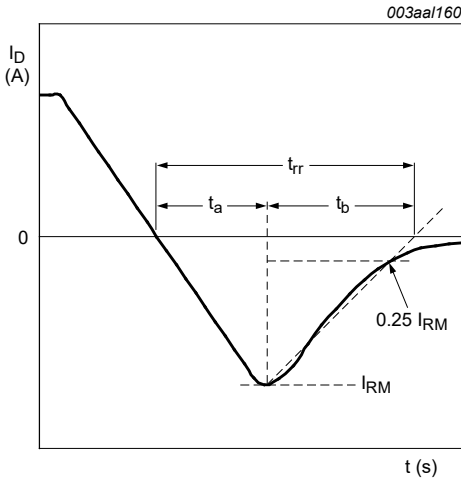


Fig. 18. Reverse recovery timing definition



11. Package outline

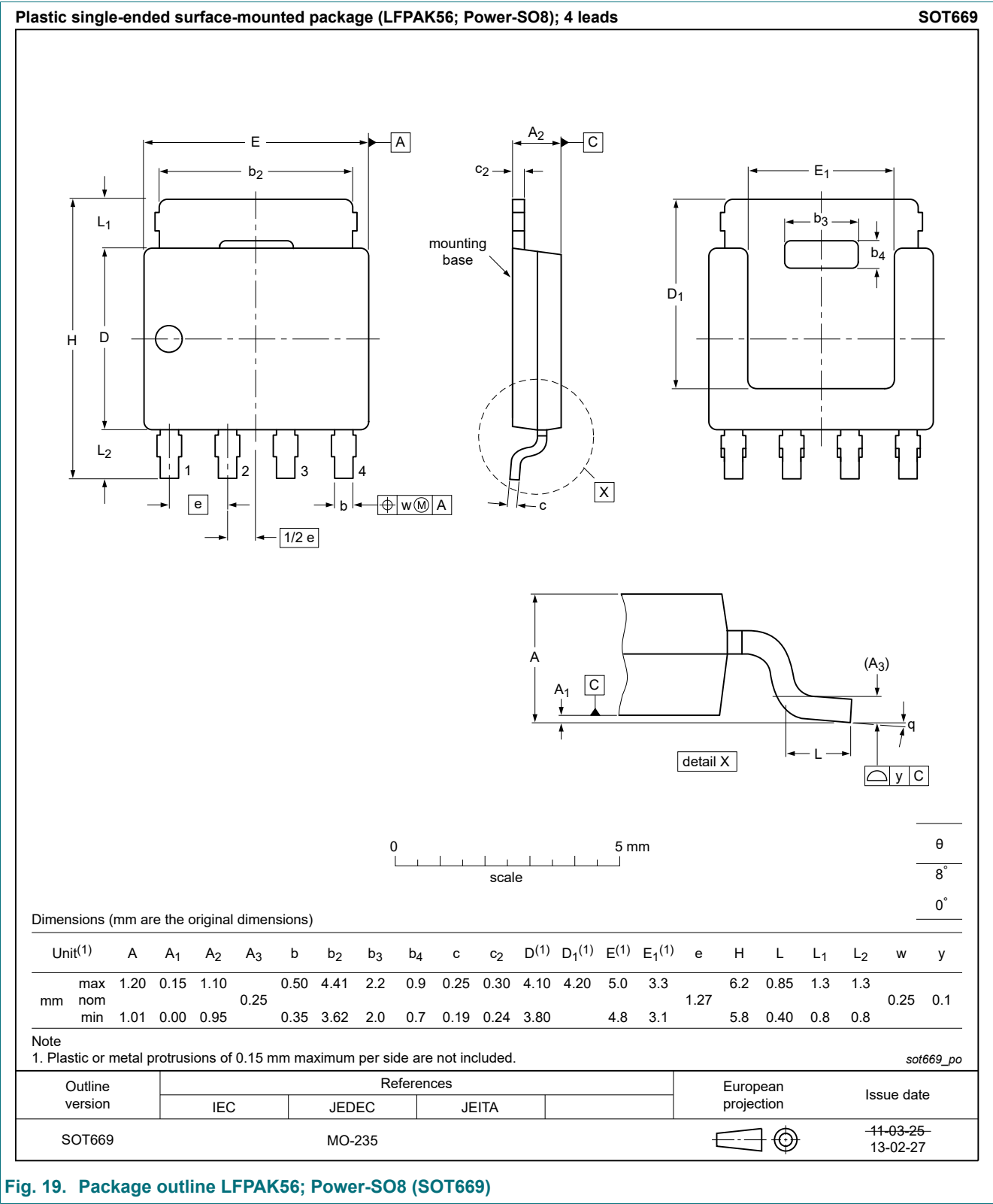
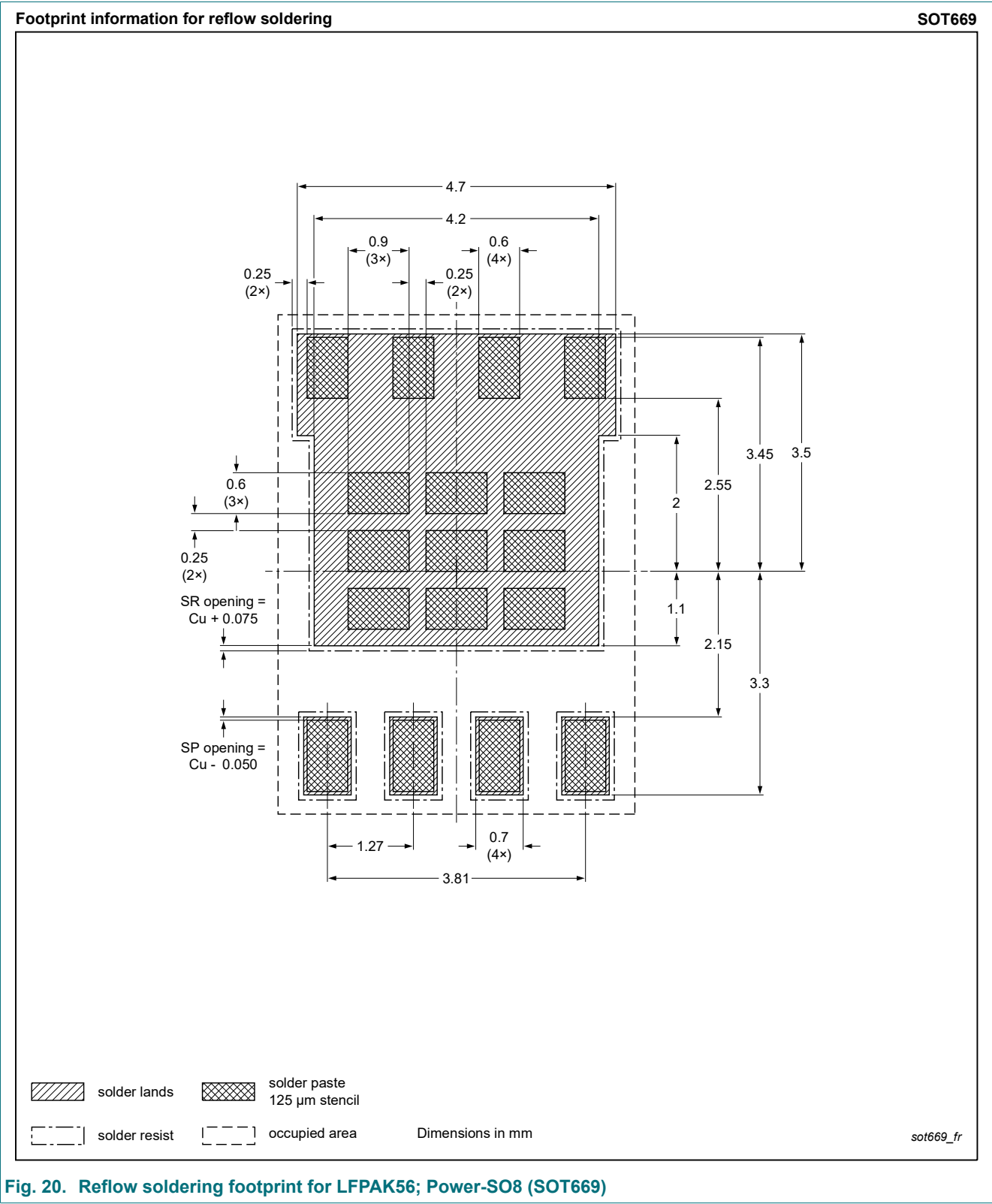


Fig. 19. Package outline LPAK56; Power-SO8 (SOT669)

12. Soldering



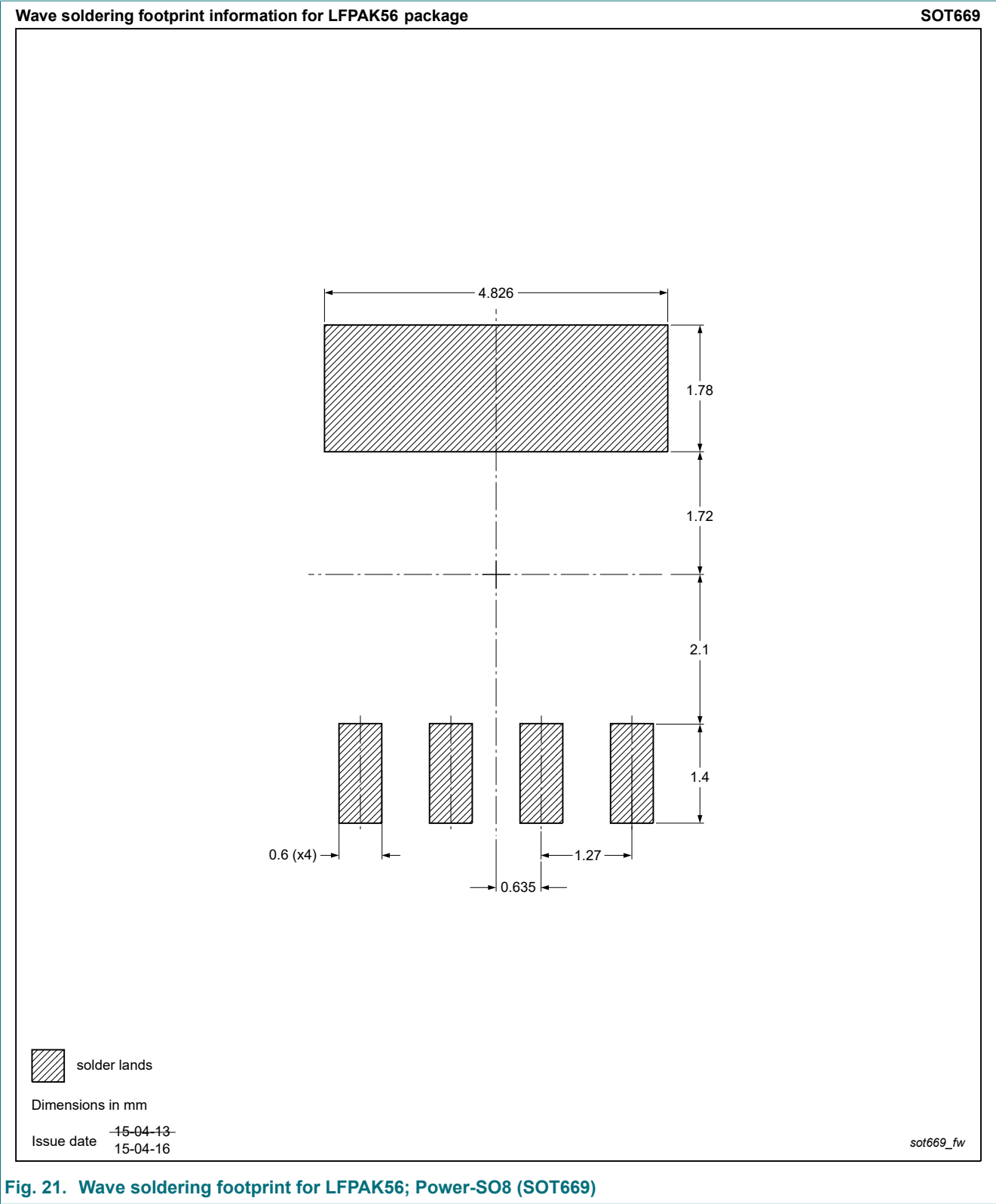


Fig. 21. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

### 13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Applications..... 1

4. Quick reference data..... 1

5. Pinning information.....2

6. Ordering information.....2

7. Marking.....2

8. Limiting values..... 2

9. Thermal characteristics..... 4

10. Characteristics..... 5

11. Package outline..... 9

12. Soldering..... 10

13. Legal information.....12

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