



PSMNR70-40YSN

N-channel 40 V, 0.81 mOhm, 360 A standard level MOSFET in LFAK56E using NextPower-S3 Schottky-Plus technology

20 May 2024

Preliminary data sheet

1. General description

360 Amp, standard level gate drive N-channel enhancement mode MOSFET in 175 °C LFAK56E package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- 360 A continuous $I_{D(max)}$
- Avalanche rated, 100% tested at $I_{AS} = 190$ A
- Low spiking, allowing for high system efficiency and low EMI designs
- NextPower-S3 technology delivers 'superfast switching with soft body-diode recovery
- Low Q_{rr} , spiking, ringing, and oscillation for high system efficiency and low EMI designs
- Schottky-Plus body-diode with low V_{SD} , and low I_{DSS} leakage
- High reliability LFAK (Power SO8) package, with copper-clip and solder die attach, qualified to 175 °C
- Exposed leads for enhanced visual solder joint inspection and high-quality solder joints for ultimate reliability
- Low parasitic inductance and resistance

3. Applications

- High-performance synchronous rectification
- DC-to-DC converters
- High performance and high efficiency server power supply
- Brushless DC motor control
- Battery protection
- Load-switch
- eFuse

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	360	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	333	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	0.5	0.72	0.81	mΩ
		$V_{GS} = 10\text{ V}$; $I_D = 25\text{ A}$; $T_j = 125\text{ °C}$; Fig. 13	0.75	1.12	1.33	mΩ

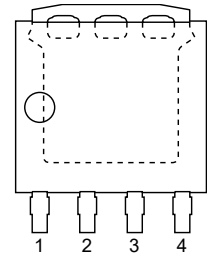
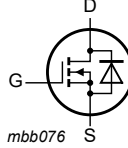
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 20\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 14; Fig. 15	14	46	77	nC
$Q_{G(\text{tot})}$	total gate charge		101	168	235	nC
Avalanche ruggedness						
$E_{DS(\text{AL})S}$	non-repetitive drain-source avalanche energy	$I_D = 80.75\text{ A}$; $V_{\text{sup}} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped; $t_p = 304\text{ }\mu\text{s}$; Fig. 4	[2]	-	638	mJ
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 18	[3]	-	30	nC

- [1] 360A Continuous current will be demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
 [2] Protected by 100% test
 [3] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56E; Power-SO8 (SOT1023)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR70-40YSN	LPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LPAK56E); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR70-40YSN	N9040S

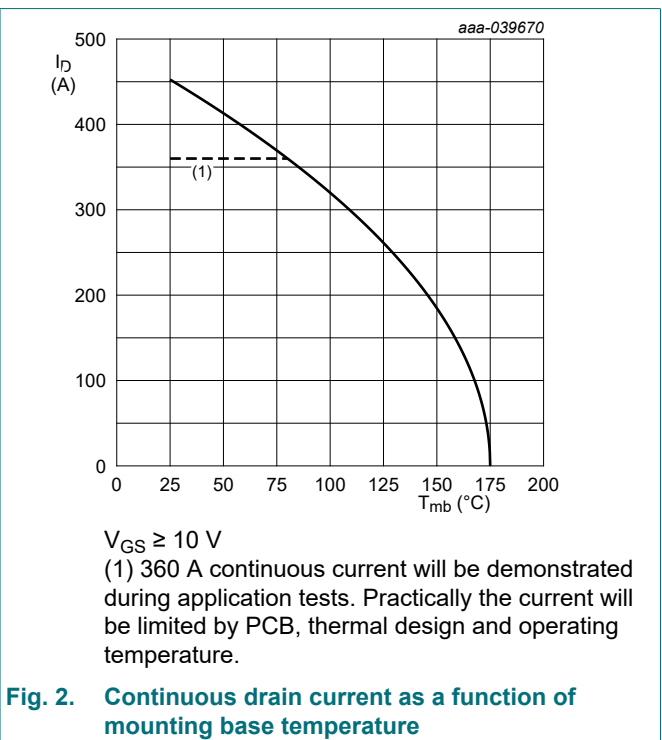
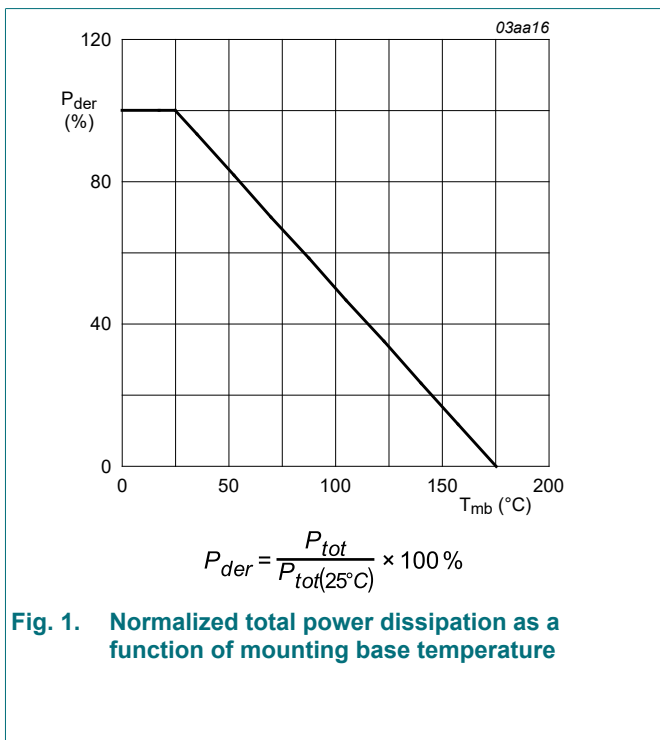
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). $T_j = 25\text{ °C}$ unless otherwise stated

Symbol	Parameter	Conditions	Min	Max	Unit	
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	40	V	
V_{DSM}	peak drain-source voltage	$t_p \leq 20\text{ ns}$; $f \leq 500\text{ kHz}$; $E_{DS(AL)} \leq 200\text{ nJ}$; pulsed	-	45	V	
V_{GS}	gate-source voltage		-20	20	V	
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	333	W	
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	360	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2		-	320	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	1810	A	
T_{stg}	storage temperature		-55	175	°C	
T_j	junction temperature		-55	175	°C	
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	-	333	A	
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	1810	A	
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 80.75\text{ A}$; $V_{sup} \leq 40\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 304\text{ }\mu\text{s}$; Fig. 4	[2]	-	638	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 4	[2]	-	190	A

- [1] 360A Continuous current will be demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test



N-channel 40 V, 0.81 mOhm, 360 A standard level MOSFET in LPAK56E using NextPower-S3 Schottky-Plus technology

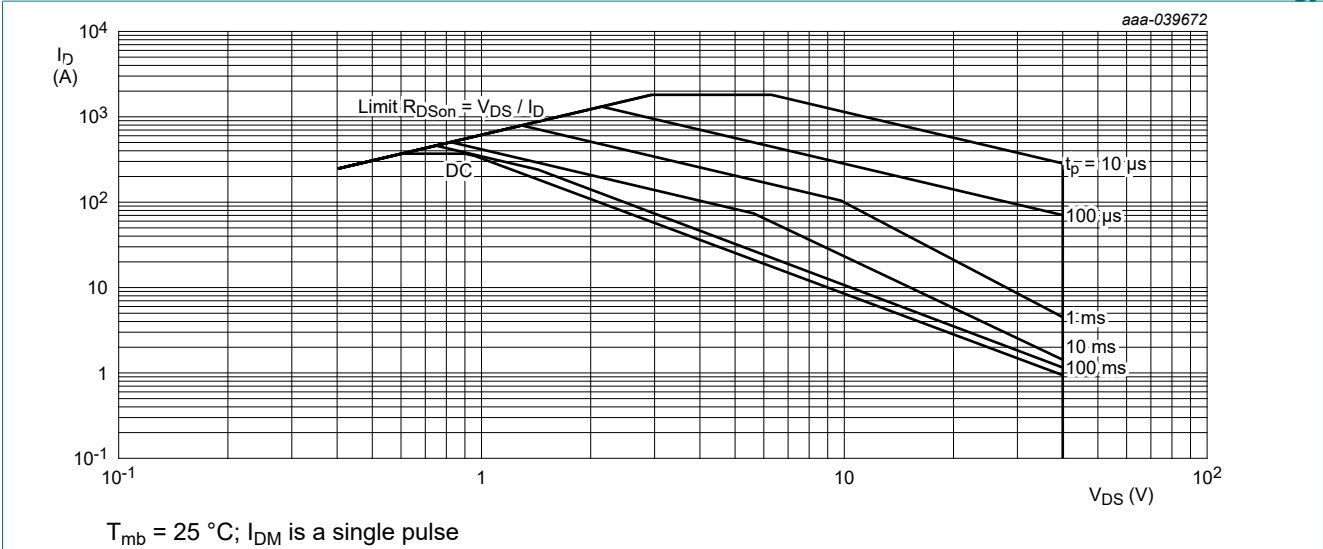


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

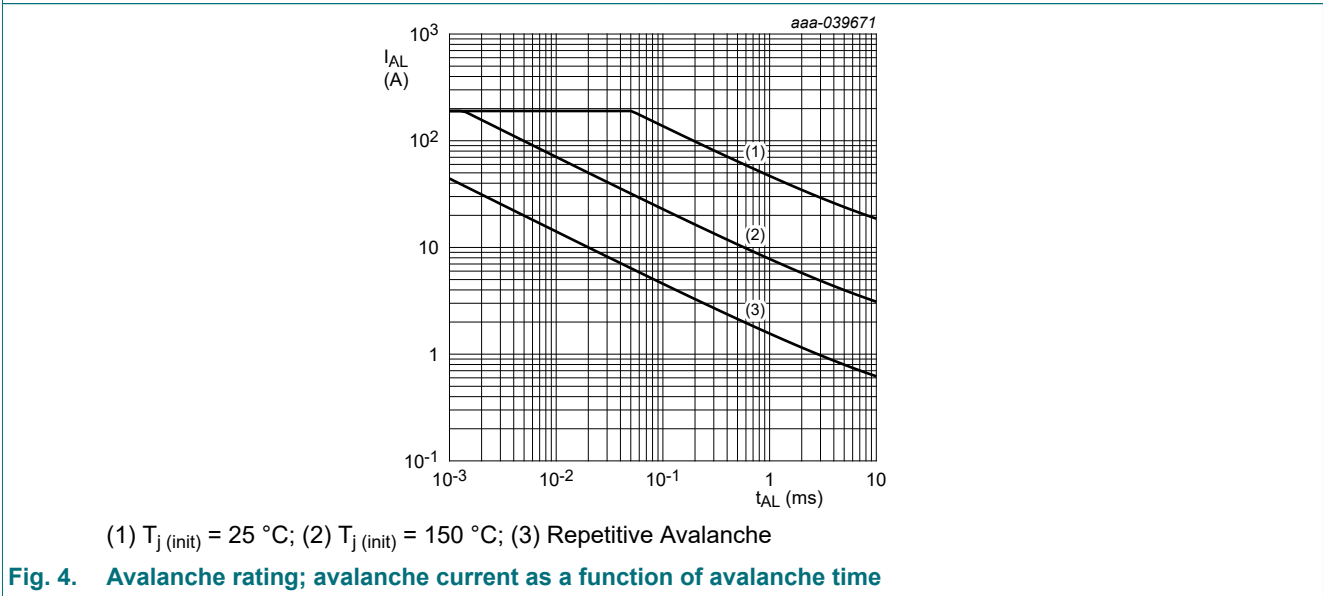


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.4	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6	-	42	-	K/W
		Fig. 7	-	85	-	K/W

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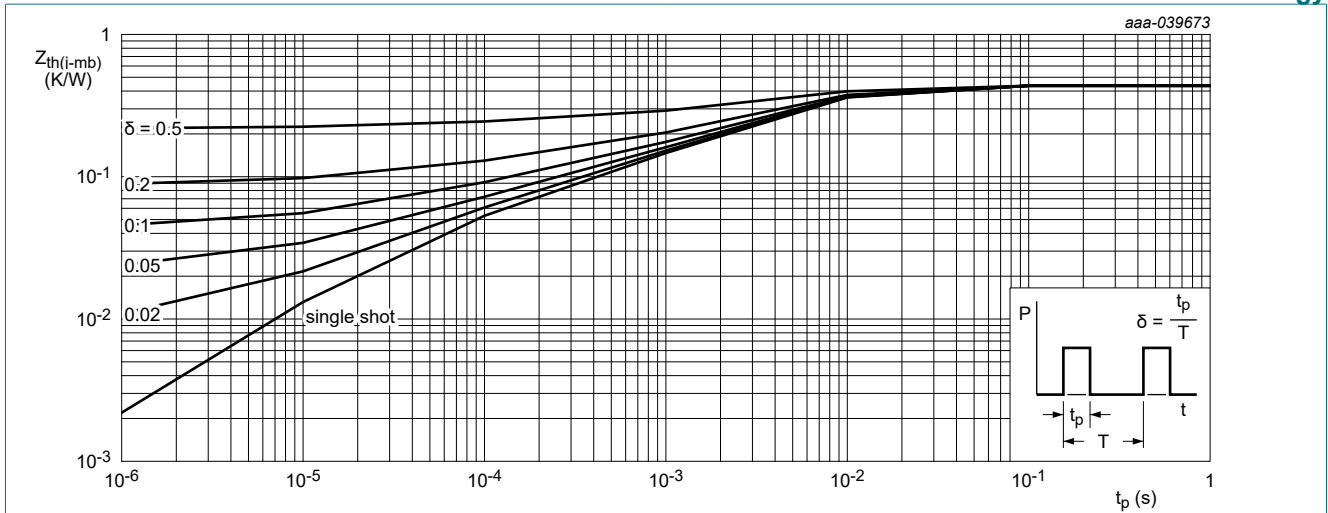


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

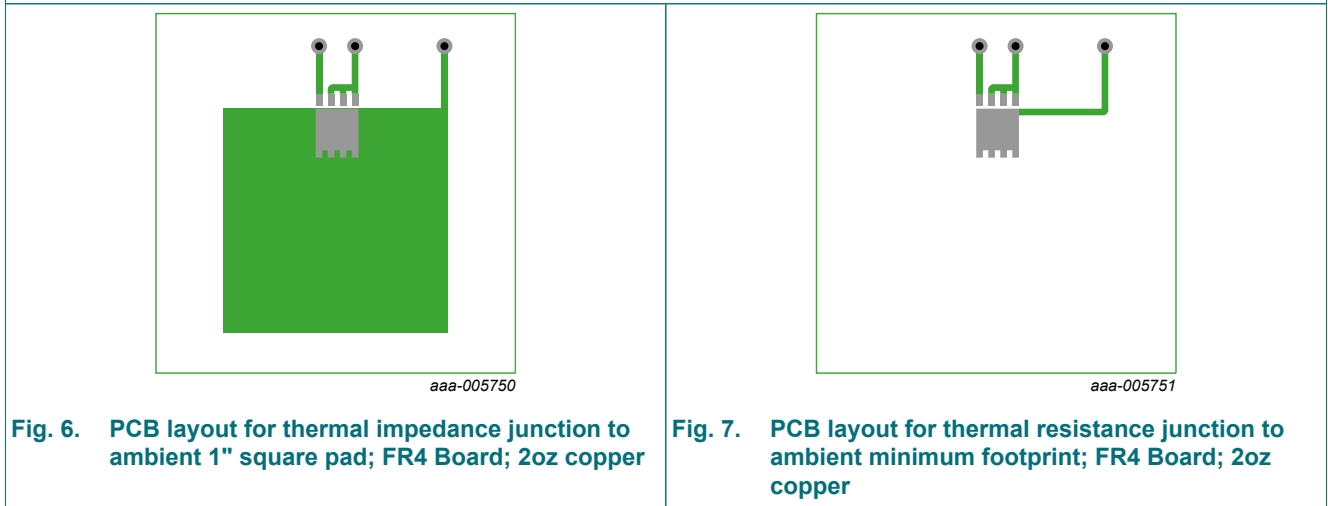


Fig. 6. PCB layout for thermal impedance junction to ambient 1" square pad; FR4 Board; 2oz copper

Fig. 7. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	43	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	41	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}$	2.4	2.9	3.6	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.4	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.9	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 175 \text{ }^\circ C$	-	-7.4	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.1	1	μA
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	1.2	10	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _J = 25 °C; Fig. 12	0.5	0.72	0.81	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 105 °C; Fig. 13	0.69	1.03	1.22	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 125 °C; Fig. 13	0.75	1.12	1.33	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _J = 175 °C; Fig. 13	0.89	1.38	1.8	mΩ
R _G	gate resistance	f = 1 MHz; T _J = 25 °C	0.32	0.81	2.03	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 20 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15	101	168	235	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _J = 25 °C	-	136	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 20 V; V _{GS} = 10 V; T _J = 25 °C; Fig. 14 ; Fig. 15	20	37	52	nC
Q _{GS(th)}	pre-threshold gate-source charge		14	25	36	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		6	11	15	nC
Q _{GD}	gate-drain charge		14	46	77	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 20 V; T _J = 25 °C; Fig. 14 ; Fig. 15	-	4.2	-	V
C _{iss}	input capacitance	V _{DS} = 20 V; V _{GS} = 0 V; f = 1 MHz; T _J = 25 °C; Fig. 16	5926	9877	13828	pF
C _{oss}	output capacitance		1518	2169	2820	pF
C _{rss}	reverse transfer capacitance		340	849	1359	pF
t _{d(on)}	turn-on delay time	V _{DS} = 30 V; R _L = 1.2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω; T _J = 25 °C	-	30	-	ns
t _r	rise time		-	52	-	ns
t _{d(off)}	turn-off delay time		-	100	-	ns
t _f	fall time		-	68	-	ns
Q _{oss}	output charge	V _{GS} = 0 V; V _{DS} = 20 V; f = 1 MHz; T _J = 25 °C	-	66	-	nC
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _J = 25 °C; Fig. 17	-	0.78	1	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _J = 25 °C; Fig. 18	-	37	-	ns
Q _r	recovered charge		[1]	30	-	nC

[1] includes capacitive recovery

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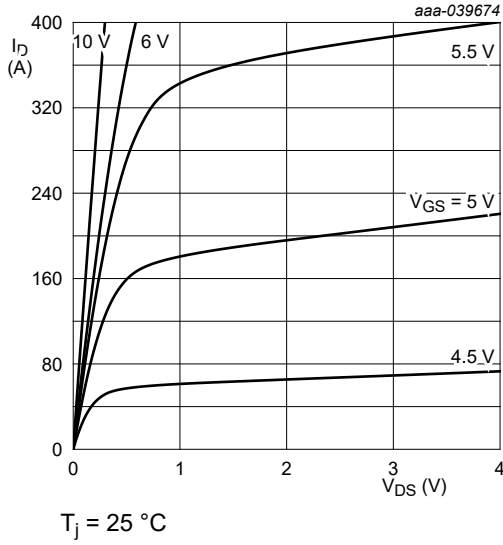


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

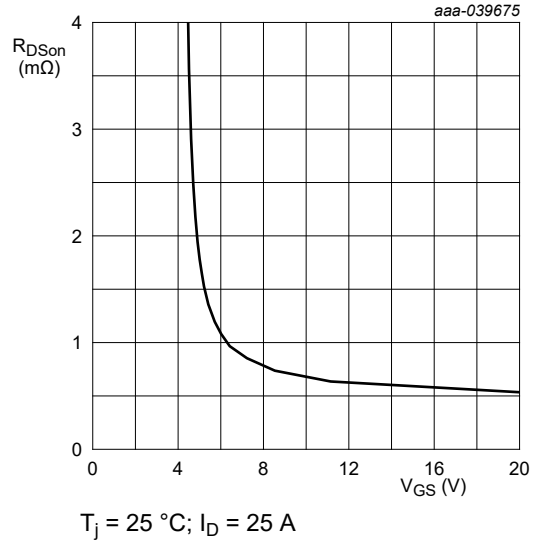


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

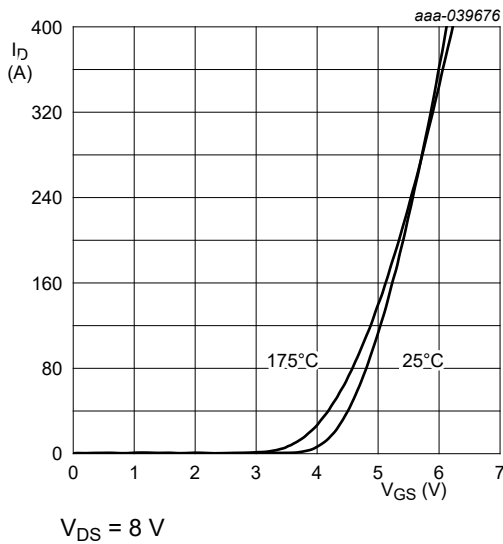


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

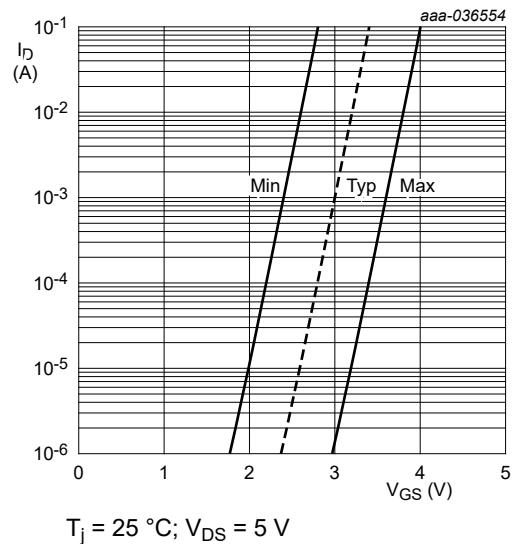


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

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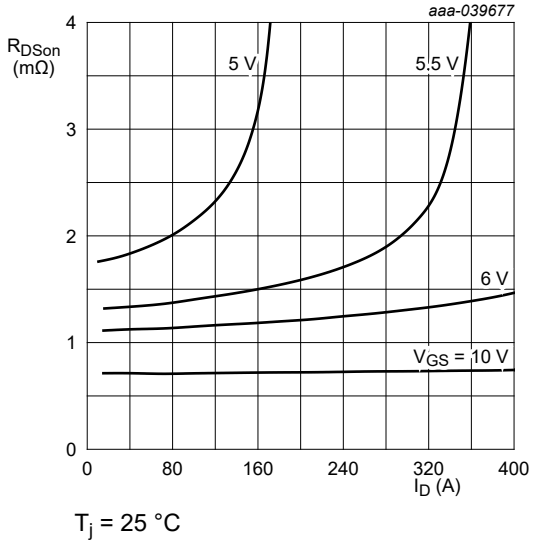
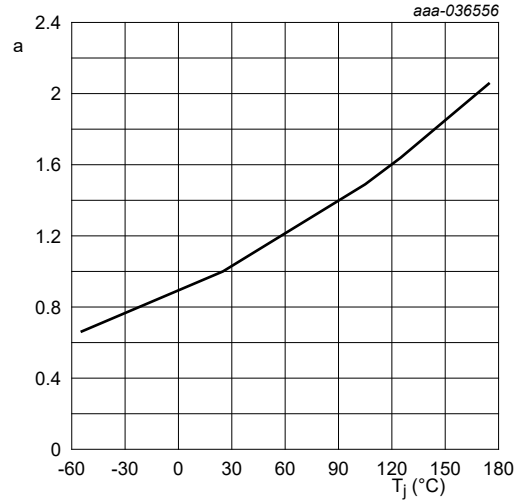


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

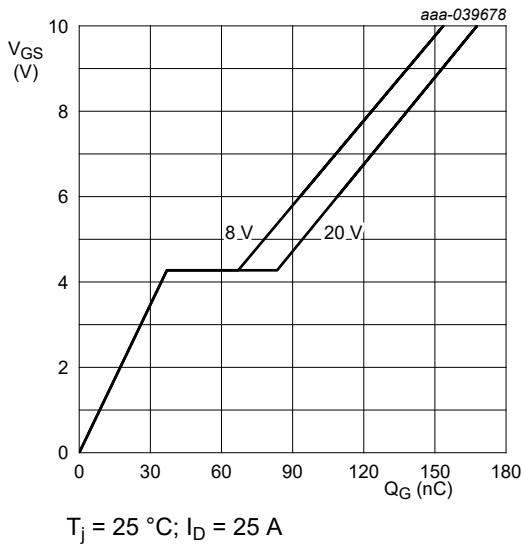


Fig. 14. Gate-source voltage as a function of gate charge; typical values

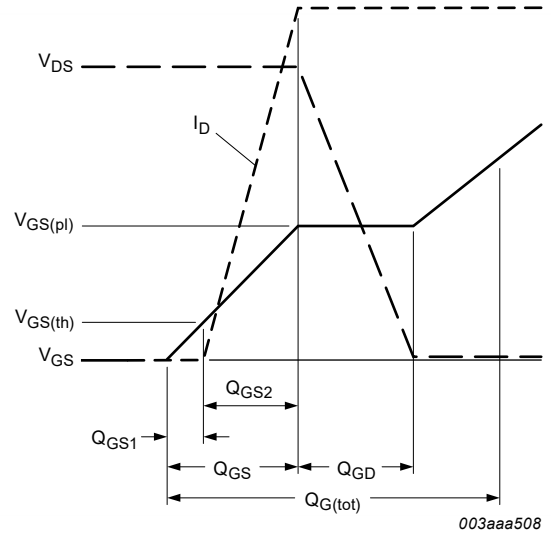


Fig. 15. Gate charge waveform definitions

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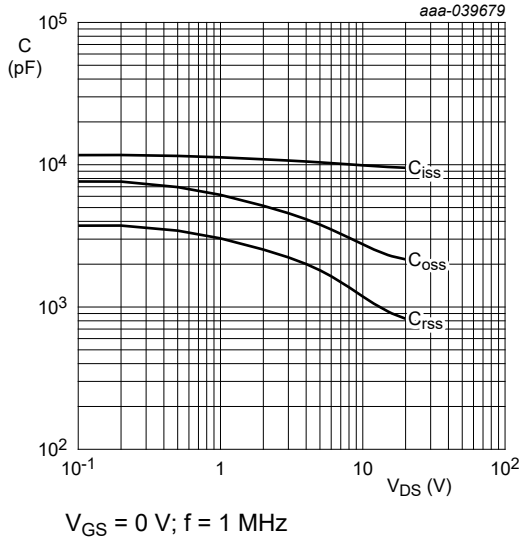


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

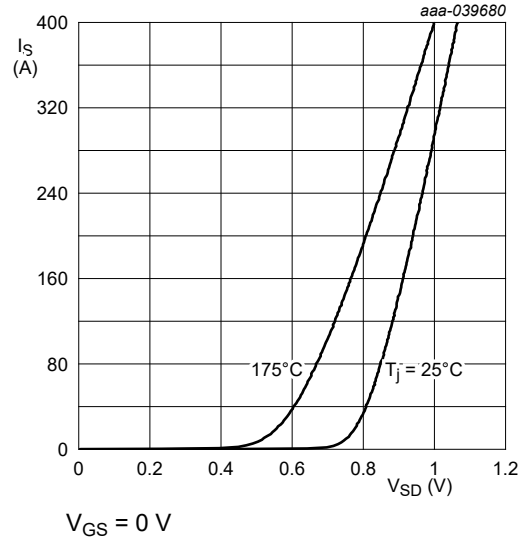


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

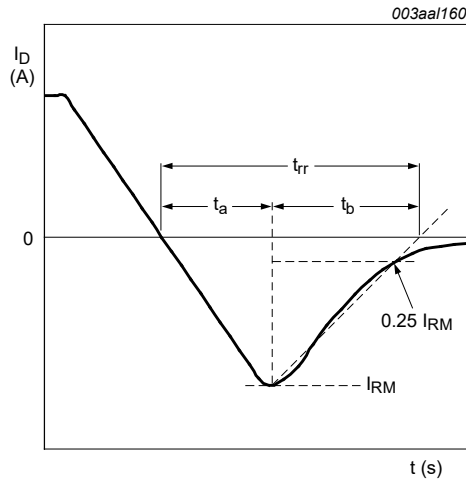


Fig. 18. Reverse recovery timing definition

11. Package outline

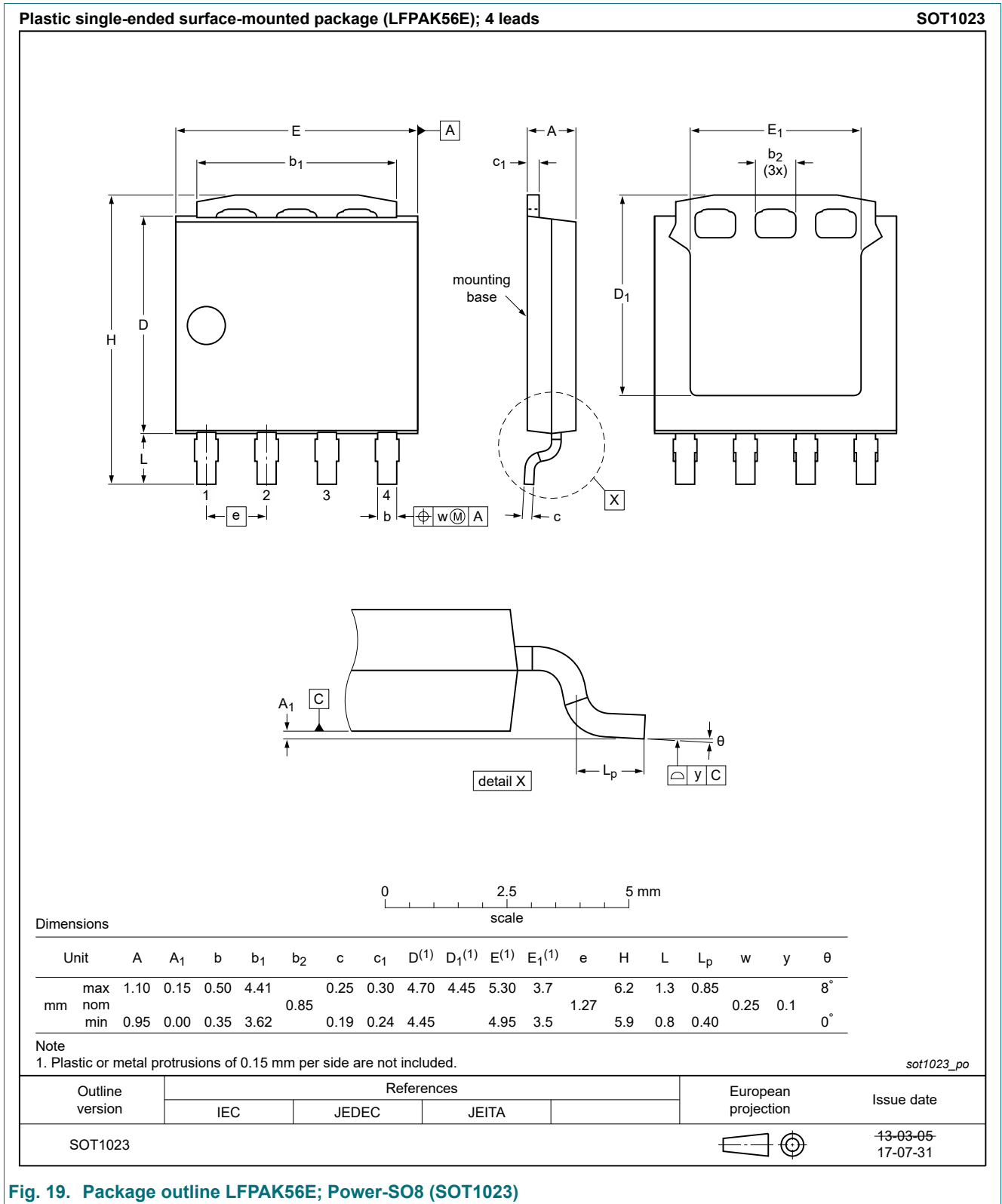


Fig. 19. Package outline LPAK56E; Power-SO8 (SOT1023)

12. Soldering

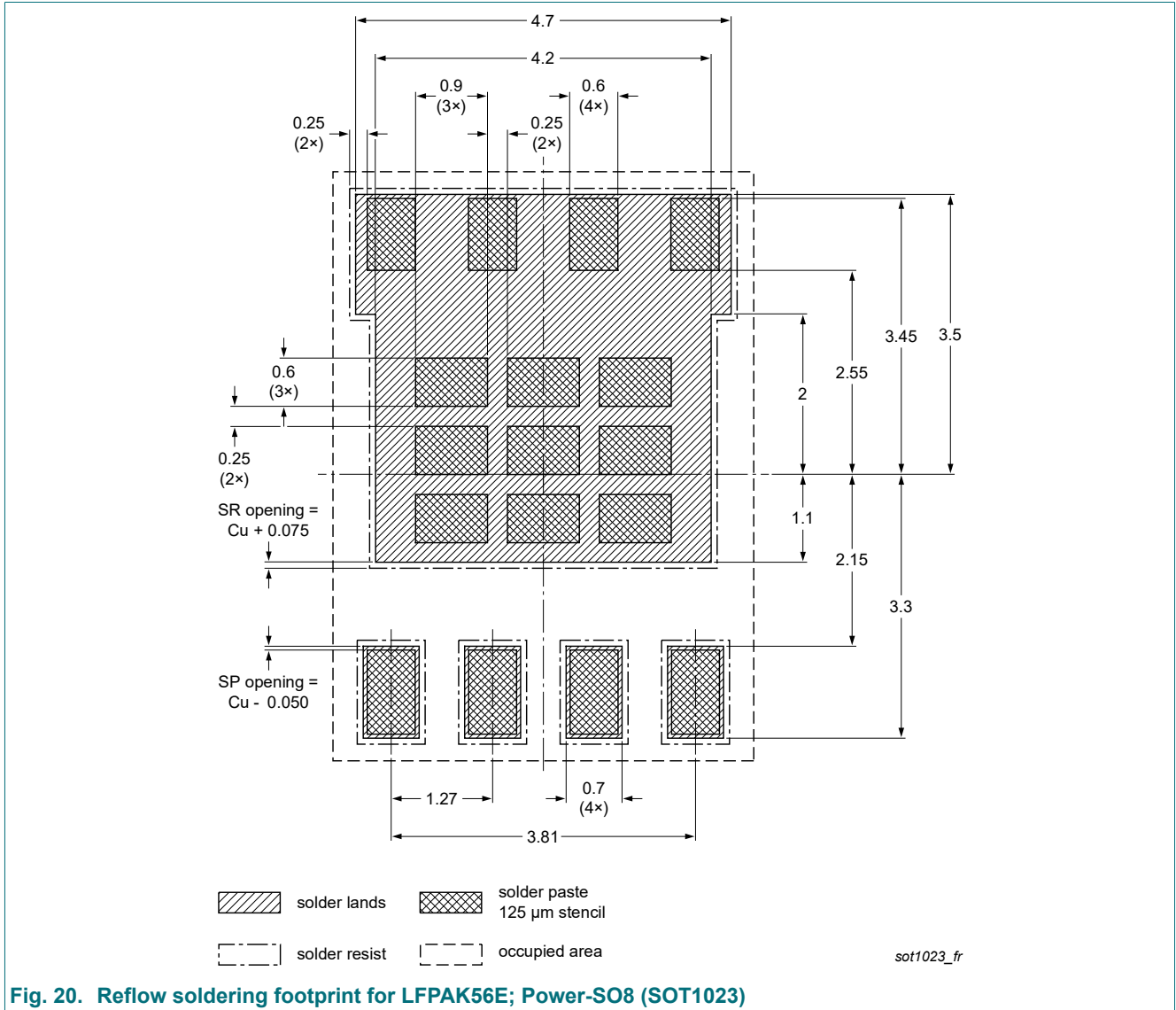


Fig. 20. Reflow soldering footprint for LPAK56E; Power-SO8 (SOT1023)

N-channel 40 V, 0.81 mOhm, 360 A standard level MOSFET in LPAK56E using NextPower-S3 Schottky-Plus technology

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	3
9. Thermal characteristics.....	4
10. Characteristics.....	5
11. Package outline.....	10
12. Soldering.....	11
13. Legal information.....	12

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