1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK56 package optimized for low $R_{\text{DSon}}$. Low $I_{\text{DSS}}$ leakage even when hot, high efficiency and high current. Rated to 300 A, optimized for DC load switch and hot-swap applications.

2. Features and benefits

- 100% avalanche tested at $I_{\text{AS}} = 190$ A
- Optimized for low $R_{\text{DSon}}$
- Low leakage < 1 μA at 25 °C
- Low spiking and ringing for low EMI designs
- Optimized for 4.5 V gate drive
- Copper-clip for low parasitic inductance and resistance
- High reliability LFPAK package, qualified to 175 °C
- Wave solderable; exposed leads for optimal solder coverage and visual solder inspection

3. Applications

- Hot swap
- e-Fuse
- Power OR-ing
- DC switch / Load switch
- Battery protection
- Brushed and BLDC (brushless) motor control
- Synchronous rectification in AC-DC and DC-DC applications

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{DS}}$</td>
<td>drain-source voltage</td>
<td>$25 ^\circ \text{C} \leq T_{\text{j}} \leq 175 ^\circ \text{C}$</td>
<td>-</td>
<td>-</td>
<td>25</td>
<td>V</td>
</tr>
<tr>
<td>$I_{\text{D}}$</td>
<td>drain current</td>
<td>$V_{\text{GS}} = 10 \text{ V}; T_{\text{mb}} = 25 ^\circ \text{C}; \text{Fig. 2}$</td>
<td>[1]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_{\text{tot}}$</td>
<td>total power dissipation</td>
<td>$T_{\text{mb}} = 25 ^\circ \text{C}; \text{Fig. 1}$</td>
<td>-</td>
<td>-</td>
<td>268</td>
<td>W</td>
</tr>
<tr>
<td>$T_{\text{j}}$</td>
<td>junction temperature</td>
<td></td>
<td>-55</td>
<td></td>
<td>175</td>
<td>°C</td>
</tr>
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</table>

**Static characteristics**

- $R_{\text{DSon}}$ drain-source on-state resistance
  - $V_{\text{GS}} = 10 \text{ V}; I_{\text{D}} = 25 \text{ A}; T_{\text{j}} = 25 ^\circ \text{C}; \text{Fig. 10}$
  - $V_{\text{GS}} = 4.5 \text{ V}; I_{\text{D}} = 25 \text{ A}; T_{\text{j}} = 25 ^\circ \text{C}; \text{Fig. 10}$
  - 0.59 mΩ
  - 0.7 mΩ
  - 0.82 mΩ
  - 1.02 mΩ

**Dynamic characteristics**

- $Q_{\text{GD}}$ gate-drain charge
  - $I_{\text{D}} = 25 \text{ A}; V_{\text{DS}} = 12 \text{ V}; V_{\text{GS}} = 4.5 \text{ V}; \text{Fig. 12; Fig. 13}$
  - 2.7 nC
  - 15 nC
  - 30 nC
  - 19 nC
  - 43 nC
  - 71 nC

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Nexperia

PSMNR60-25YLH

N-channel 25 V, 0.7 mΩ, 300 A logic level MOSFET in LFPAK56 using NextPowerS3 technology

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
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<tr>
<td>1</td>
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<td>source</td>
<td>mb</td>
</tr>
<tr>
<td>2</td>
<td>S</td>
<td>source</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>S</td>
<td>source</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>G</td>
<td>gate</td>
<td></td>
</tr>
<tr>
<td>mb</td>
<td>D</td>
<td>mounting base; connected to drain</td>
<td>LFPAK56; Power-SO8 (SOT669)</td>
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6. Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
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<tbody>
<tr>
<td>PSMNR60-25YLH</td>
<td>LFPAK56; Power-SO8</td>
<td>plastic, single-ended surface-mounted package; 4 terminals</td>
<td>SOT669</td>
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7. Marking

Table 4. Marking codes

<table>
<thead>
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<td>PSMNR60-25YLH</td>
<td>H6025L</td>
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8. Limiting values

Table 5. Limiting values

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<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
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</thead>
<tbody>
<tr>
<td>V_DS</td>
<td>drain-source voltage</td>
<td>25 °C ≤ T_j ≤ 175 °C</td>
<td>-</td>
<td>25</td>
<td>V</td>
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<tr>
<td>V_DGR</td>
<td>drain-gate voltage</td>
<td>25 °C ≤ T_j ≤ 175 °C; R_GS = 20 kΩ</td>
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<td>25</td>
<td>V</td>
</tr>
<tr>
<td>V_GS</td>
<td>gate-source voltage</td>
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<td>-20</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>P_tot</td>
<td>total power dissipation</td>
<td>T_mb = 25 °C; Fig. 1</td>
<td>-</td>
<td>268</td>
<td>W</td>
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<tr>
<td>I_D</td>
<td>drain current</td>
<td>V_GS = 10 V; T_mb = 25 °C; Fig. 2</td>
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<td>300</td>
<td>A</td>
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<tr>
<td>I_DM</td>
<td>peak drain current</td>
<td>pulsed; t_p ≤ 10 µs; T_mb = 25 °C; Fig. 3</td>
<td>-</td>
<td>1758</td>
<td>A</td>
</tr>
<tr>
<td>T_stg</td>
<td>storage temperature</td>
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<td>175</td>
<td>°C</td>
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<td>T_j</td>
<td>junction temperature</td>
<td></td>
<td>-55</td>
<td>175</td>
<td>°C</td>
</tr>
</tbody>
</table>

[1] 300A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
Nexperia

**PSMNR60-25YLH**

N-channel 25 V, 0.7 mΩ, 300 A logic level MOSFET in LFPAK56 using NextPowerS3 technology

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
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<tr>
<td>$T_{sld(M)}$</td>
<td>peak soldering temperature</td>
<td></td>
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**Source-drain diode**

<table>
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<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$</td>
<td>source current</td>
<td>$T_{mb} = 25$ °C</td>
<td>-</td>
<td>268</td>
<td>A</td>
</tr>
<tr>
<td>$I_{SM}$</td>
<td>peak source current</td>
<td>pulsed; $t_p ≤ 10$ µs; $T_{mb} = 25$ °C</td>
<td>-</td>
<td>1758</td>
<td>A</td>
</tr>
</tbody>
</table>

**Avalanche ruggedness**

| $E_{DS(\text{AL})S}$ | non-repetitive drain-source avalanche energy | $I_D = 25$ A; $V_{sup} ≤ 25$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped; $t_p = 8.09$ ms | [2] | - | 3.2 J |
| $I_{AS}$ | non-repetitive avalanche current | $V_{sup} ≤ 25$ V; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $R_{GS} = 50$ Ω | [2] | - | 190 A |

[1] 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] Protected by 100% test

---

**Fig. 1.** Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot} - P_{tot(25°C)}}{P_{tot(25°C)}} \times 100\%$$

**Fig. 2.** Continuous drain current as a function of mounting base temperature

$$V_{GS} ≥ 10$$ V

(1) 300A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
9. Thermal characteristics

Table 6. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th(j-mb)}$</td>
<td>thermal resistance from junction to mounting base</td>
<td>Fig. 4</td>
<td>-</td>
<td>0.48</td>
<td>0.56</td>
<td>K/W</td>
</tr>
<tr>
<td>$R_{th(j-a)}$</td>
<td>thermal resistance from junction to ambient</td>
<td>Fig. 5, 6</td>
<td>-</td>
<td>42</td>
<td>-</td>
<td>K/W</td>
</tr>
</tbody>
</table>

Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration
Nexperia

PSMNR60-25YLH

N-channel 25 V, 0.7 mΩ, 300 A logic level MOSFET in LFPAK56 using NextPowerS3 technology

Table 7. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Static characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{(BR)DSS}$</td>
<td>drain-source breakdown voltage</td>
<td>$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \degree C$</td>
<td>25</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \degree C$</td>
<td>22.5</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS(th)}$</td>
<td>gate-source threshold voltage</td>
<td>$I_D = 2 mA; V_{DS} = V_{GS}; T_j = 25 \degree C$</td>
<td>1.2</td>
<td>1.64</td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{GS(th)}$</td>
<td>gate-source threshold voltage variation with temperature</td>
<td>$25 \degree C \leq T_j \leq 150 \degree C$</td>
<td>-</td>
<td>-4.7</td>
<td>-</td>
<td>mV/K</td>
</tr>
<tr>
<td>$I_DSS$</td>
<td>drain leakage current</td>
<td>$V_{DS} = 20 V; V_{GS} = 0 V; T_j = 25 \degree C$</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = 20 V; V_{GS} = 0 V; T_j = 125 \degree C$</td>
<td>-</td>
<td>5.4</td>
<td>-</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{GSS}$</td>
<td>gate leakage current</td>
<td>$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \degree C$</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \degree C$</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>drain-source on-state resistance</td>
<td>$V_{GS} = 10 V; I_D = 25 A; T_j = 25 \degree C$; Fig. 10</td>
<td>-</td>
<td>0.59</td>
<td>0.7</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 10 V; I_D = 25 A; T_j = 150 \degree C$; Fig. 11</td>
<td>-</td>
<td>-</td>
<td>1.25</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 \degree C$; Fig. 10</td>
<td>-</td>
<td>0.82</td>
<td>1.02</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 4.5 V; I_D = 25 A; T_j = 150 \degree C$; Fig. 11</td>
<td>-</td>
<td>-</td>
<td>1.82</td>
<td>mΩ</td>
</tr>
<tr>
<td>$R_G$</td>
<td>gate resistance</td>
<td>$f = 1 MHz; T_j = 25 \degree C$</td>
<td>0.56</td>
<td>1.4</td>
<td>3.5</td>
<td>Ω</td>
</tr>
</tbody>
</table>

Dynamic characteristics

<table>
<thead>
<tr>
<th>$Q_{G(tot)}$</th>
<th>total gate charge</th>
<th>$I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V$; Fig. 12; Fig. 13</th>
<th>19</th>
<th>43</th>
<th>71</th>
<th>nC</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>$I_D = 25 A; V_{DS} = 12 V; V_{GS} = 10 V$; Fig. 12; Fig. 13</td>
<td>40</td>
<td>89</td>
<td>147</td>
<td>nC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$</td>
<td>-</td>
<td>45</td>
<td>-</td>
<td>nC</td>
</tr>
</tbody>
</table>

Fig. 5. PCB layout for thermal resistance from junction to ambient

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics
## Symbol | Parameter | Conditions | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | --- | ---
Q_{GS} | gate-source charge | I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Fig. 12, Fig. 13 | 3.2 | 12 | 23 | nC
Q_{GS(th)} | pre-threshold gate-source charge | | 2.1 | 8 | 15 | nC
Q_{GS(th-pl)} | post-threshold gate-source charge | | 1.1 | 4.1 | 7.8 | nC
Q_{GD} | gate-drain charge | I_D = 25 A; V_{DS} = 12 V; V_{GS} = 4.5 V; Fig. 12, Fig. 13 | 2.7 | 15 | 30 | nC
V_{GS(pl)} | gate-source plateau voltage | I_D = 25 A; V_{DS} = 12 V; Fig. 12, Fig. 13 | - | 2.5 | - | V
C_{iss} | input capacitance | V_{DS} = 12 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C | 3247 | 5411 | 8117 | pF
C_{oss} | output capacitance | | 2047 | 3412 | 5118 | pF
C_{rss} | reverse transfer capacitance | | 166 | 616 | 1478 | pF
I_{d(on)} | turn-on delay time | V_{DS} = 12 V; R_L = 0.4 Ω; V_{GS} = 4.5 V; R_{G(ext)} = 5 Ω | - | 32 | - | ns
I_r | rise time | | - | 61 | - | ns
I_{d(off)} | turn-off delay time | | - | 50 | - | ns
I_f | fall time | | - | 44 | - | ns
Q_{oss} | output charge | V_{GS} = 0 V; V_{DS} = 12 V; f = 1 MHz; T_j = 25 °C | - | 53 | - | nC

### Source-drain diode

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
--- | --- | --- | --- | --- | --- | ---
V_{SD} | source-drain voltage | I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 15 | - | 0.76 | 1 | V
I_{rr} | reverse recovery time | I_S = 25 A; dI_S/dt = -100 A/μs; V_{GS} = 0 V; V_{DS} = 12 V; Fig. 16 | - | 42 | - | ns
Q_r | recovered charge | | [1] | - | 41 | - | nC
I_a | reverse recovery rise time | | - | 21 | - | ns
I_b | reverse recovery fall time | | - | 21 | - | ns
S | softness factor | | - | 1 | - | |

[1] includes capacitive recovery

---

**Fig. 7.** Output characteristics; drain current as a function of drain-source voltage; typical values

**Fig. 8.** Drain-source on-state resistance as a function of gate-source voltage; typical values
N-channel 25 V, 0.7 mΩ, 300 A logic level MOSFET in LFPAK56 using NextPowerS3 technology

**Fig. 9.** Transfer characteristics; drain current as a function of gate-source voltage; typical values

\[ V_{DS} = 8 \text{ V} \]

**Fig. 10.** Drain-source on-state resistance as a function of drain current; typical values

\[ T_J = 25 \degree \text{C} \]

**Fig. 11.** Normalized drain-source on-state resistance factor as a function of junction temperature

\[ a = \frac{R_{DSon}}{R_{DSon} (25 \degree \text{C})} \]

**Fig. 12.** Gate-source voltage as a function of gate charge; typical values

\[ T_J = 25 \degree \text{C}; I_D = 25 \text{ A} \]
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PSMNR60-25YLH

N-channel 25 V, 0.7 mΩ, 300 A logic level MOSFET in LFPAK56 using NextPowerS3 technology

Fig. 13. Gate charge waveform definitions

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

Fig. 16. Reverse recovery timing definition
11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads

Dimensions (mm are the original dimensions)

<table>
<thead>
<tr>
<th>Unit(1)</th>
<th>A</th>
<th>A_1</th>
<th>A_2</th>
<th>A_3</th>
<th>b</th>
<th>b_2</th>
<th>b_3</th>
<th>b_4</th>
<th>c</th>
<th>c_2</th>
<th>D(1)</th>
<th>D_1(1)</th>
<th>E(1)</th>
<th>E_1(1)</th>
<th>e</th>
<th>H</th>
<th>L</th>
<th>L_1</th>
<th>L_2</th>
<th>w</th>
<th>y</th>
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<td>1.10</td>
<td>0.50</td>
<td>4.41</td>
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<td>5.0</td>
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<td>0.1</td>
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</tr>
<tr>
<td>min</td>
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<td>0.00</td>
<td>0.95</td>
<td>0.25</td>
<td>3.62</td>
<td>2.0</td>
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<td>0.8</td>
<td>0.25</td>
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Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)
12. Soldering

Footprint information for reflow soldering

Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT669)
Fig. 19. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)
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PSMNR60-25YLH

N-channel 25 V, 0.7 mΩ, 300 A logic level MOSFET in LFPAK56 using NextPowerS3 technology

13. Legal information

Data sheet status

<table>
<thead>
<tr>
<th></th>
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<tbody>
<tr>
<td>Objective [short] data sheet</td>
<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Preliminary [short] data sheet</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Product [short] data sheet</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
</table>

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term "short data sheet" is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

Definitions

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