



# PSMN9R8-100YSF

NextPower 100 V, 10.2 mOhm N-channel MOSFET in LFPAK56 package

20 June 2023

Product data sheet

## 1. General description

NextPower 100 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

## 2. Features and benefits

- Low  $Q_{rr}$  for higher efficiency and lower spiking
- Low  $Q_G \times R_{DSon}$  FOM for high efficiency switching applications
- Strong avalanche energy rating ( $E_{AS}$ )
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFPAK56 package
- Wave-solderable LFPAK56 package

## 3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in 48 V DC-DC
- BLDC motor control
- USB-PD and mobile fast-charge adapters
- Flyback and resonant topologies

## 4. Quick reference data

Table 1. Quick reference data

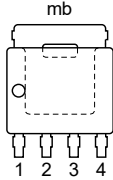
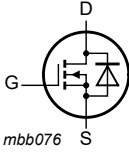
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	-	-	80	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>	-	-	147	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 20\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 12</a>	-	8.3	10.2	mΩ
		$V_{GS} = 10\text{ V}; I_D = 20\text{ A}; T_j = 100\text{ °C};$ <a href="#">Fig. 13</a>	-	13	16.2	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 20\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ °C};$ <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	1.8	6	13.8	nC
$Q_{G(tot)}$	total gate charge		16.8	34	50.4	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 30.4\text{ A}; V_{sup} \leq 100\text{ V}; R_{GS} = 50\text{ Ω};$ $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C};$ unclamped; $t_p = 56\text{ μs};$ <a href="#">Fig. 4</a>	[1]	-	111	mJ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 50\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 18</a>	-	22	-	nC

[1] Protected by 100% test

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p><b>LFAK56; Power-SO8 (SOT669)</b></p>	 <p><i>mbb076</i></p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN9R8-100YSF	LFAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN9R8-100YSF	9F8S10Y

## 8. Limiting values

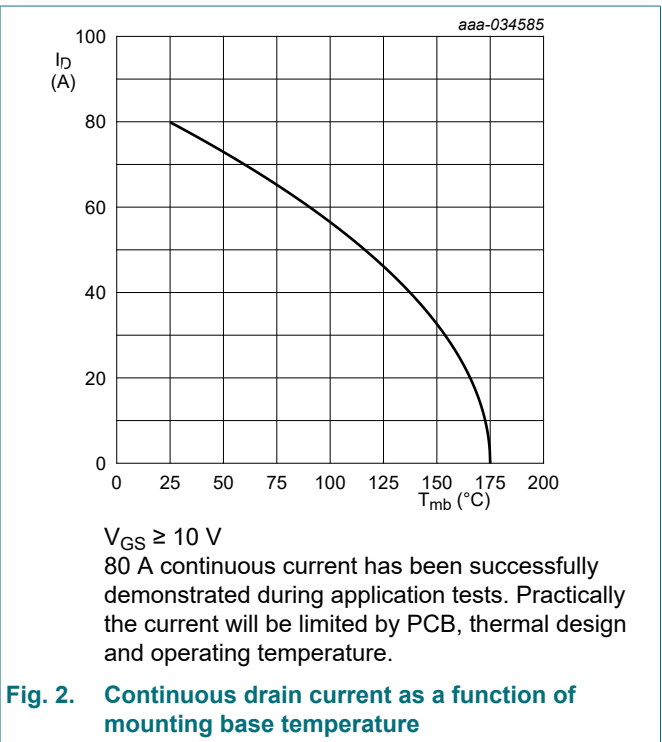
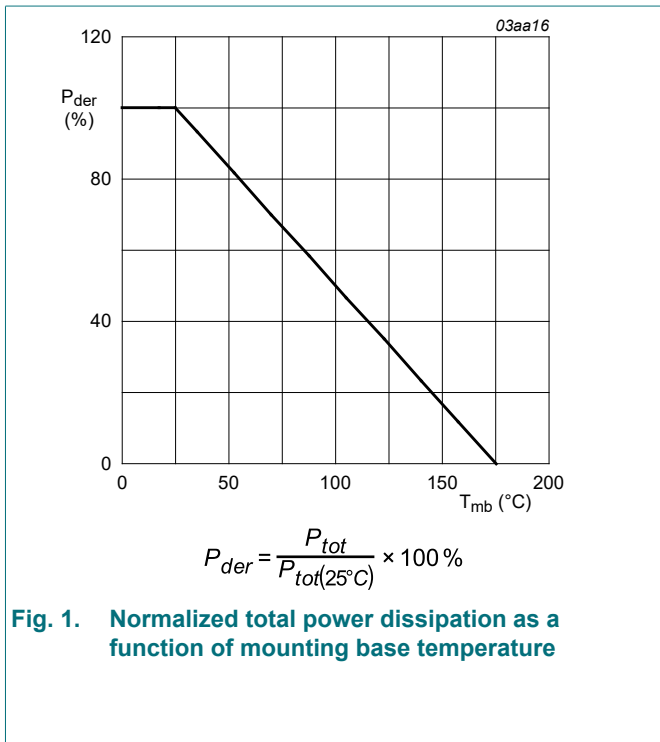
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25\text{ }^\circ\text{C}$  unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	-	100	V
$V_{DGR}$	drain-gate voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>	-	147	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	-	80	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ }^\circ\text{C}$ ; <a href="#">Fig. 2</a>	-	57	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 3</a>	-	320	A
$T_{stg}$	storage temperature		-55	175	$^\circ\text{C}$
$T_j$	junction temperature		-55	175	$^\circ\text{C}$

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{\text{sid(M)}}$	peak soldering temperature		-	260	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{\text{mb}} = 25\text{ °C}$	-	80	A
$I_{\text{SM}}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{\text{mb}} = 25\text{ °C}$	-	320	A
<b>Avalanche ruggedness</b>					
$E_{\text{DS(AL)S}}$	non-repetitive drain-source avalanche energy	$I_D = 30.4\text{ A}$ ; $V_{\text{sup}} \leq 100\text{ V}$ ; $R_{\text{GS}} = 50\text{ }\Omega$ ; $V_{\text{GS}} = 10\text{ V}$ ; $T_{\text{J(init)}} = 25\text{ °C}$ ; unclamped; $t_p = 56\text{ }\mu\text{s}$ ; <a href="#">Fig. 4</a>	[1]	-	111 mJ
$I_{\text{AS}}$	non-repetitive avalanche current	$V_{\text{sup}} \leq 100\text{ V}$ ; $V_{\text{GS}} = 10\text{ V}$ ; $T_{\text{J(init)}} = 25\text{ °C}$ ; $R_{\text{GS}} = 50\text{ }\Omega$ ; <a href="#">Fig. 4</a>	[1]	-	30.4 A

[1] Protected by 100% test



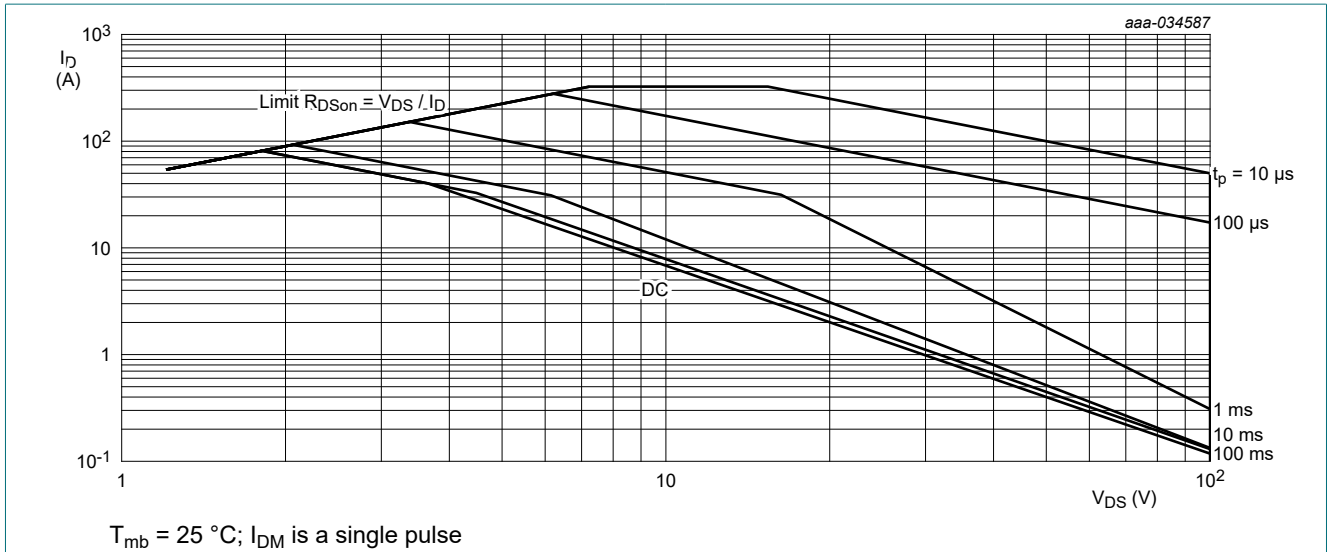


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

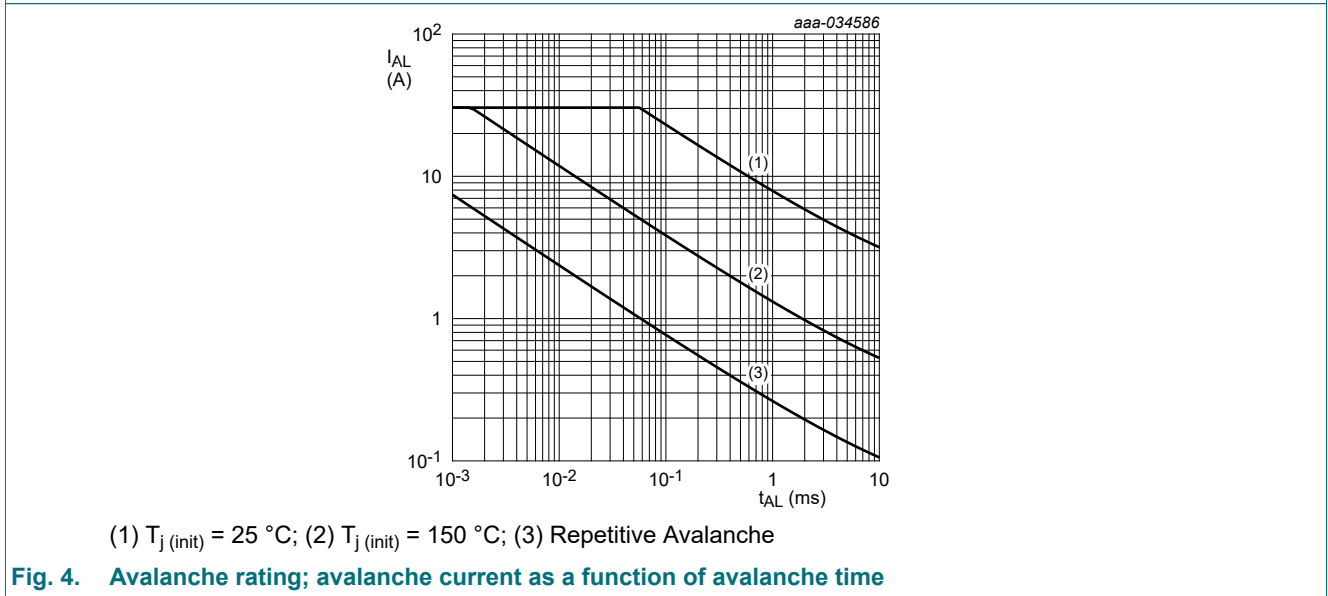


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	0.92	1.02	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 6</a>	-	42	-	K/W
		<a href="#">Fig. 7</a>	-	85	-	K/W

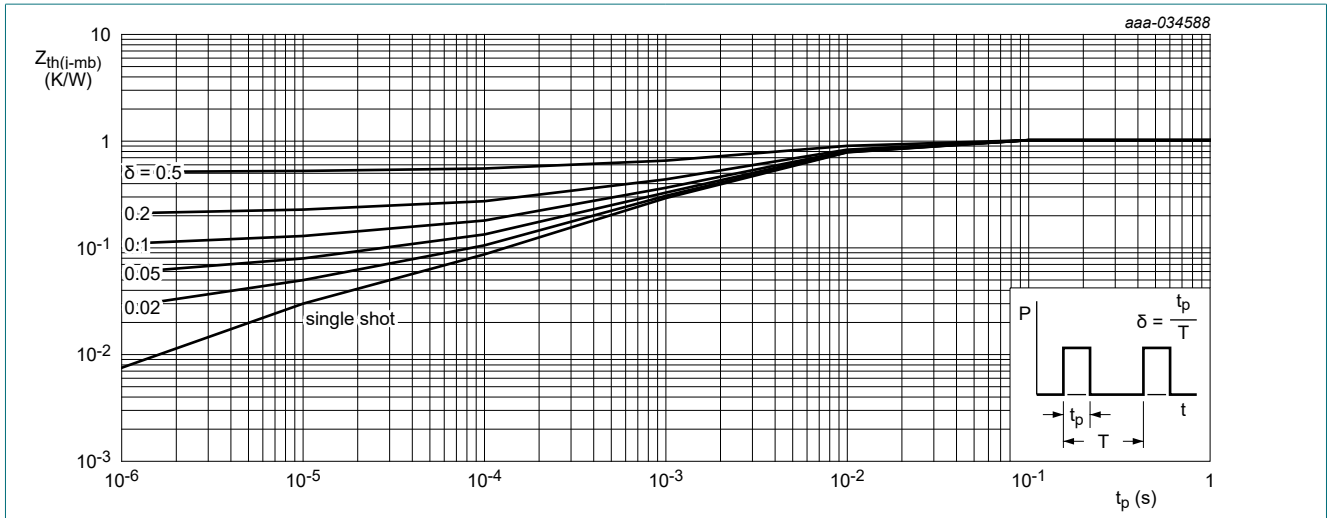


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

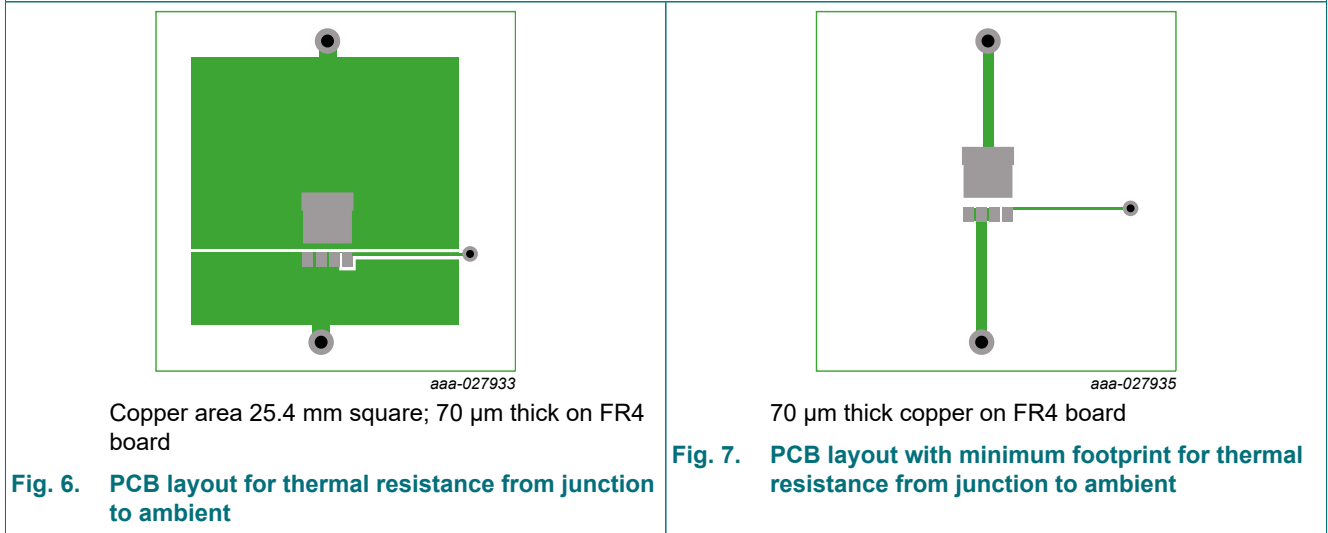


Fig. 6. PCB layout for thermal resistance from junction to ambient

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

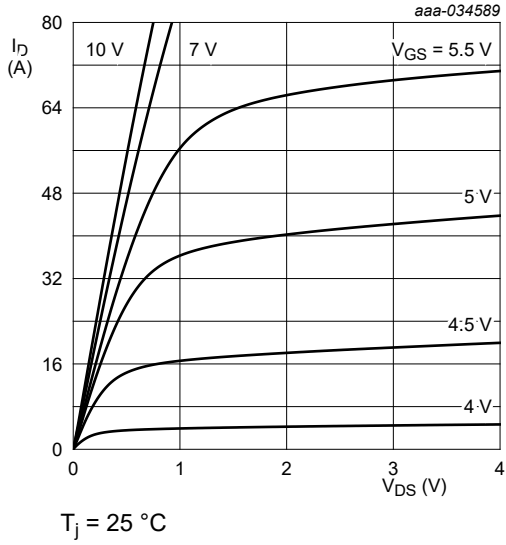
## 10. Characteristics

Table 7. Characteristics

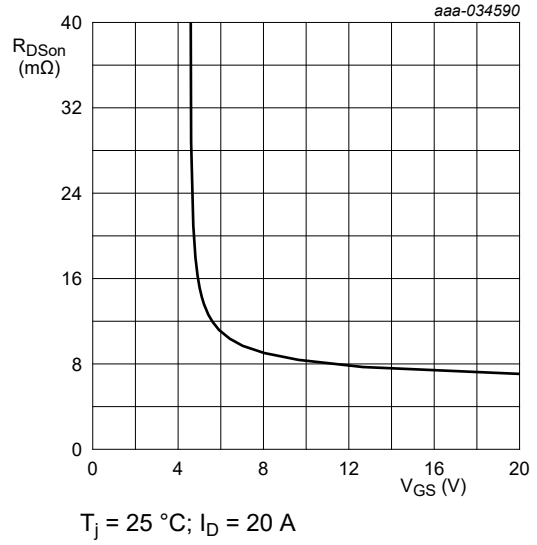
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 11}$	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.8	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.4	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-7.4	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.01	1	$\mu A$
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	5	100	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA

## NextPower 100 V, 10.2 mOhm N-channel MOSFET in LPAK56 package

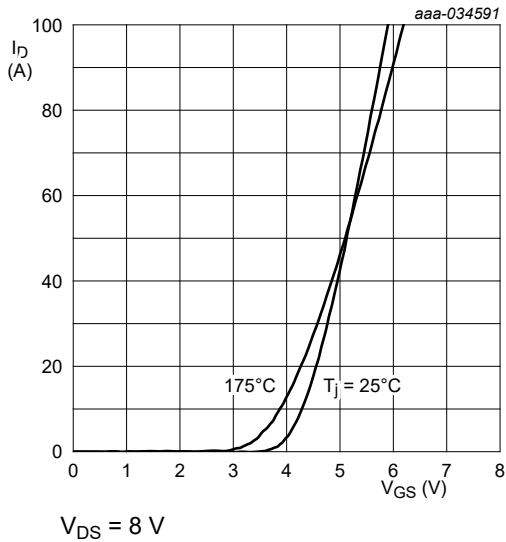
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 20\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a>	-	8.3	10.2	mΩ
		$V_{GS} = 7\text{ V}$ ; $I_D = 20\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 12</a>	-	9.7	15	mΩ
		$V_{GS} = 10\text{ V}$ ; $I_D = 20\text{ A}$ ; $T_j = 100\text{ °C}$ ; <a href="#">Fig. 13</a>	-	13	16.2	mΩ
		$V_{GS} = 10\text{ V}$ ; $I_D = 20\text{ A}$ ; $T_j = 175\text{ °C}$ ; <a href="#">Fig. 13</a>	-	18.4	23.2	mΩ
$R_G$	gate resistance	$f = 1\text{ MHz}$ ; $T_j = 25\text{ °C}$	0.8	1.6	3.2	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 20\text{ A}$ ; $V_{DS} = 50\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	16.8	34	50.4	nC
		$I_D = 0\text{ A}$ ; $V_{DS} = 0\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_j = 25\text{ °C}$	-	17.5	-	nC
$Q_{GS}$	gate-source charge	$I_D = 20\text{ A}$ ; $V_{DS} = 50\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	6.2	10.3	14.4	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	6.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	3.5	-	nC
$Q_{GD}$	gate-drain charge		1.8	6	13.8	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 20\text{ A}$ ; $V_{DS} = 50\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 15</a>	-	4.6	-	V
$C_{iss}$	input capacitance	$V_{DS} = 50\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $f = 1\text{ MHz}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 16</a>	1450	2417	3384	pF
$C_{oss}$	output capacitance		347	579	926	pF
$C_{rss}$	reverse transfer capacitance		2	20	52	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50\text{ V}$ ; $R_L = 2.5\text{ Ω}$ ; $V_{GS} = 10\text{ V}$ ; $R_{G(ext)} = 5\text{ Ω}$ ; $T_j = 25\text{ °C}$	-	10	-	ns
$t_r$	rise time		-	9	-	ns
$t_{d(off)}$	turn-off delay time		-	22	-	ns
$t_f$	fall time		-	12	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 20\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 17</a>	-	0.83	1	V
$t_{rr}$	reverse recovery time	$I_S = 20\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 50\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 18</a>	-	31	-	ns
$Q_r$	recovered charge		-	22	-	nC



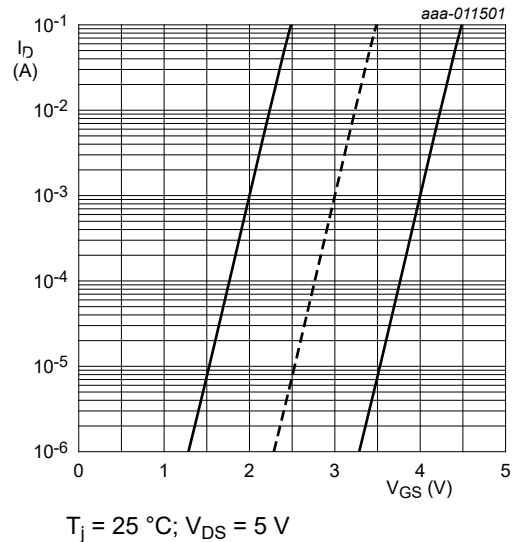
**Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values**



**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



**Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values**



**Fig. 11. Sub-threshold drain current as a function of gate-source voltage**

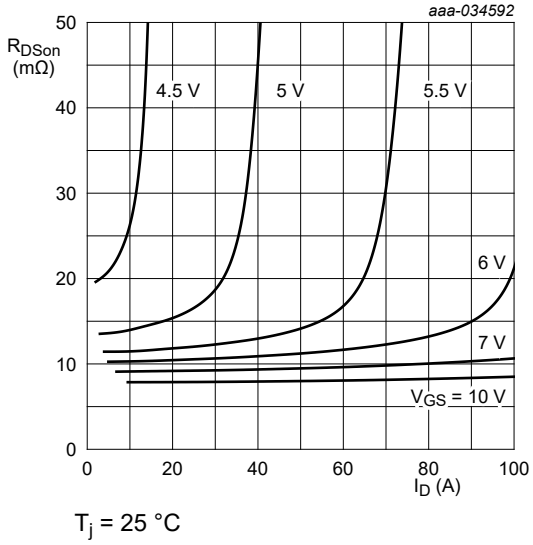
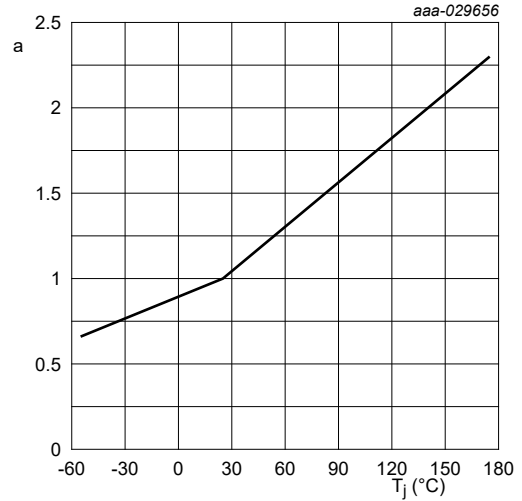


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

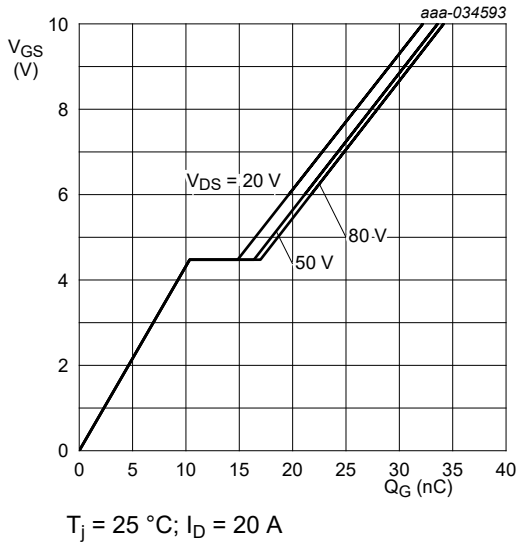


Fig. 14. Gate-source voltage as a function of gate charge; typical values

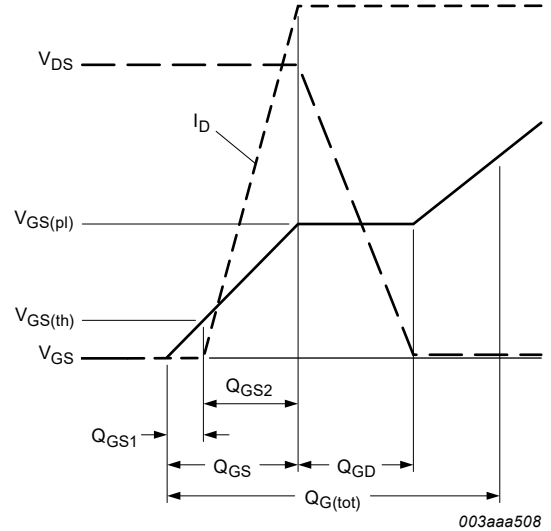


Fig. 15. Gate charge waveform definitions



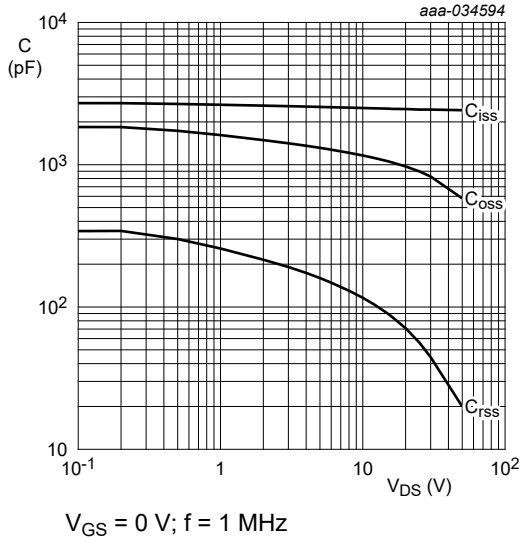


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

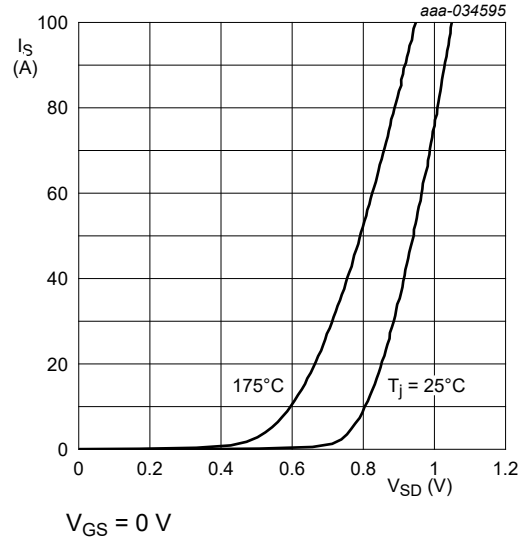


Fig. 17. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

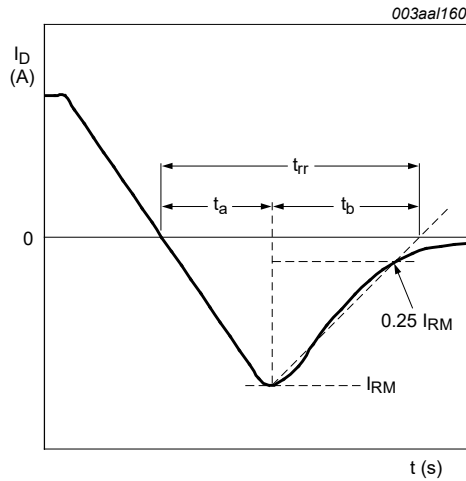


Fig. 18. Reverse recovery timing definition

### 11. Package outline

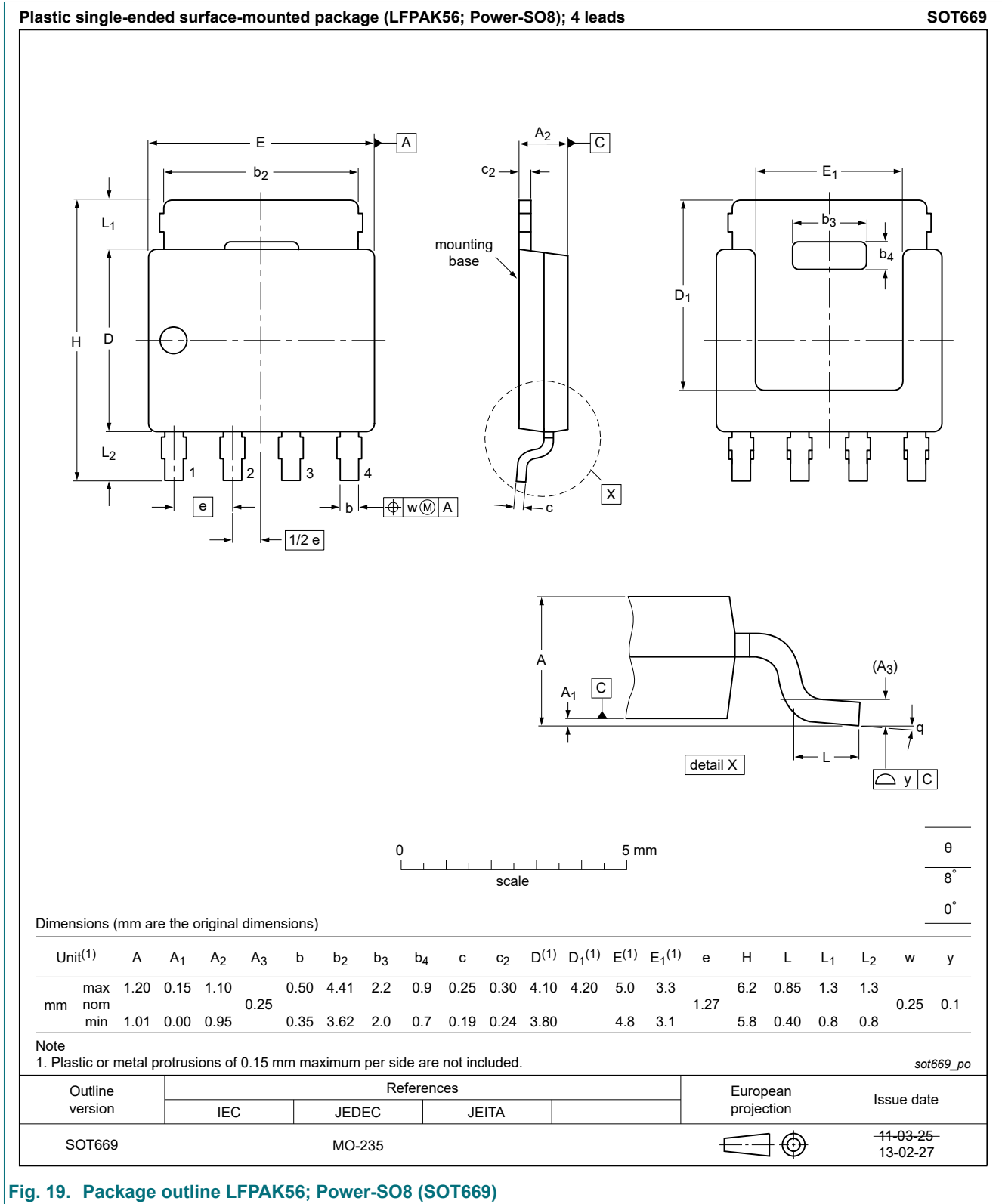
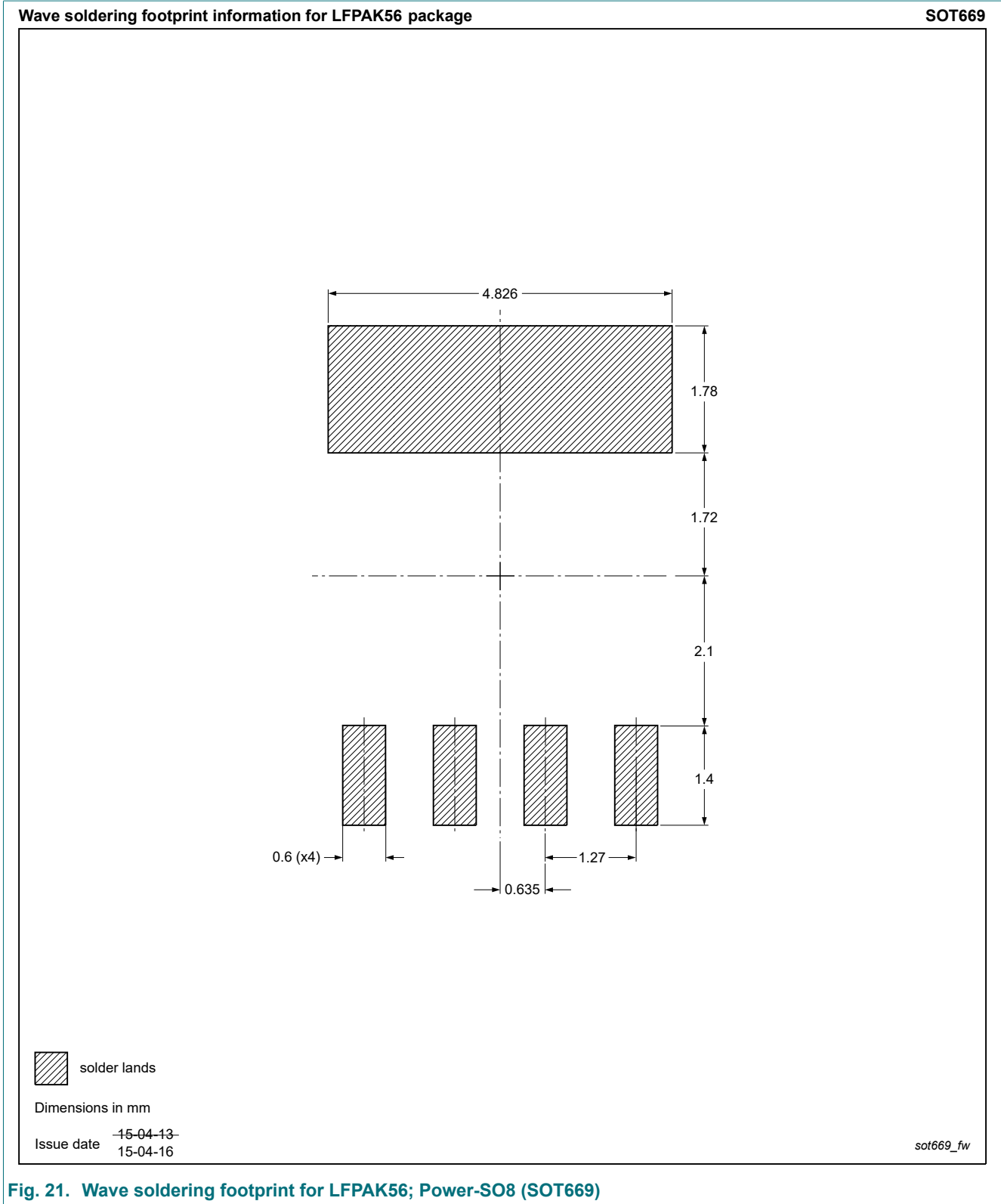


Fig. 19. Package outline LPAK56; Power-SO8 (SOT669)





## 13. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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For more information, please visit: <http://www.nexperia.com>  
For sales office addresses, please send an email to: [salesaddresses@nexperia.com](mailto:salesaddresses@nexperia.com)  
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