1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK56 package. NextPowerS3 portfolio utilising Nexperia’s unique “SchottkyPlus” technology delivers high efficiency, low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

2. Features and benefits

- Ultra low $Q_G$, $Q_{GD}$ and $Q_{OSS}$ for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor > 1
- Low spiking and ringing for low EMI designs
- Unique “SchottkyPlus” technology; Schottky-like performance with $< 1 \, \mu A$ leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Wave solderable; exposed leads for optimal visual solder inspection

3. Applications

- On-board DC-to-DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
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<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 , ^\circ C \leq T_j \leq 175 , ^\circ C$</td>
<td>-</td>
<td>-</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>drain current</td>
<td>$T_{mb} = 25 , ^\circ C; , V_{GS} = 10 , V; , \text{Fig. 2}$</td>
<td>-</td>
<td>-</td>
<td>51</td>
<td>A</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 , ^\circ C; , \text{Fig. 1}$</td>
<td>-</td>
<td>-</td>
<td>34</td>
<td>W</td>
</tr>
</tbody>
</table>
PSMN7R5-30YLD

N-channel 30 V, 7.5 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

Symbol | Parameter | Conditions | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | --- | ---
T_j | junction temperature | -55 | - | 175 | °C

**Static characteristics**

Symbol | Parameter | Conditions | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | --- | ---
R_DSON | drain-source on-state resistance | $V_{GS} = 4.5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \degree \text{C};$ | - | 8.1 | 10.2 | mΩ
$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \degree \text{C};$ | - | 6.1 | 7.5 | mΩ

**Dynamic characteristics**

Symbol | Parameter | Conditions | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | --- | ---
Q_GD | gate-drain charge | $V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; V_{DS} = 15 \text{ V};$ | - | 1.7 | - | nC
$V_{GS} = 4.5 \text{ V}; I_D = 15 \text{ A}; V_{DS} = 15 \text{ V};$ | Fig. 12; Fig. 13 | - | 1.7 | - | nC

S | softness factor | $I_S = 15 \text{ A}; V_{GS} = 0 \text{ V}; dI_S/dt = -100 \text{ A/µs};$ | - | 1.3 | - |
$V_{DS} = 15 \text{ V};$ | Fig. 16 | - | 1.3 | - |

5. **Pinning information**

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
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<td></td>
<td></td>
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<tr>
<td>2</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>G</td>
<td>gate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mb</td>
<td>D</td>
<td>mounting base; connected to drain</td>
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<td></td>
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6. **Ordering information**

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
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<tr>
<td>PSMN7R5-30YLD</td>
<td>LFPAK56; Power-SO8</td>
<td>Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads</td>
<td>SOT669</td>
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7. **Marking**

Table 4. Marking codes

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<th>Type number</th>
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<td>PSMN7R5-30YLD</td>
<td>7D530L</td>
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8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 , ^\circ C \leq T_j \leq 175 , ^\circ C$</td>
<td>-</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DGR}$</td>
<td>drain-gate voltage</td>
<td>$25 , ^\circ C \leq T_j \leq 175 , ^\circ C$; $R_{GS} = 20 , k\Omega$</td>
<td>-</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>gate-source voltage</td>
<td></td>
<td>-20</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 , ^\circ C$; Fig. 1</td>
<td>-</td>
<td>34</td>
<td>W</td>
</tr>
<tr>
<td>$I_D$</td>
<td>drain current</td>
<td>$V_{GS} = 10 , V$; $T_{mb} = 25 , ^\circ C$; Fig. 2</td>
<td>-</td>
<td>51</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DM}$</td>
<td>peak drain current</td>
<td>$V_{GS} = 10 , V$; $T_{mb} = 100 , ^\circ C$; Fig. 2</td>
<td>-</td>
<td>36</td>
<td>A</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>storage temperature</td>
<td>pulsed; $t_p \leq 10 , \mu s$; $T_{mb} = 25 , ^\circ C$; Fig. 3</td>
<td>-</td>
<td>202</td>
<td>A</td>
</tr>
<tr>
<td>$T_j$</td>
<td>junction temperature</td>
<td>$-55$</td>
<td>$175$</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_{sld(M)}$</td>
<td>peak soldering temperature</td>
<td></td>
<td>-</td>
<td>260</td>
<td>°C</td>
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<tr>
<td>$V_{ESD}$</td>
<td>electrostatic discharge voltage</td>
<td>HBM</td>
<td>150</td>
<td>-</td>
<td>V</td>
</tr>
</tbody>
</table>

**Source-drain diode**

| $I_S$    | source current                    | $T_{mb} = 25 \, ^\circ C$                       | -   | 29  | A    |
| $I_{SM}$ | peak source current               | pulsed; $t_p \leq 10 \, \mu s$; $T_{mb} = 25 \, ^\circ C$ | -   | 202 | A    |

**Avalanche ruggedness**

| $E_{DS(AL)}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10 \, V$; $T_j(init) = 25 \, ^\circ C$; $I_D = 15 \, A$; $V_{sup} \leq 30 \, V$; $R_{GS} = 50 \, \Omega$; unclamped; $t_p = 95 \, \mu s$ | [1] | $27.6$ | mJ   |

[1] Protected by 100% test
Fig. 1. Normalized total power dissipation as a function of mounting base temperature

\[ P_{\text{der}} = \frac{P_{\text{tot}}}{P_{\text{tot}}} \times 100 \% \]

Fig. 2. Continuous drain current as a function of mounting base temperature

\[ V_{DS} \geq 10 V \]

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

\[ T_{mb} = 25^\circ C; \quad I_{DM} \text{ is a single pulse} \]

9. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{th(j-mb)}^{\text{on}} )</td>
<td>thermal resistance from junction to mounting base</td>
<td>Fig. 4</td>
<td>-</td>
<td>4.14</td>
<td>4.36</td>
<td>K/W</td>
</tr>
</tbody>
</table>
Nexperia

PSMN7R5-30YLD

N-channel 30 V, 7.5 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th(j-a)}$</td>
<td>thermal resistance from junction to ambient</td>
<td>Fig. 5</td>
<td>-</td>
<td>50</td>
<td>-</td>
<td>K/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fig. 6</td>
<td>-</td>
<td>125</td>
<td>-</td>
<td>K/W</td>
</tr>
</tbody>
</table>

![Graph](image-url)

**Fig. 4.** Transient thermal impedance from junction to mounting base as a function of pulse duration

![PCB layout](image-url)

**Fig. 5.** PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

**Fig. 6.** PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

## 10. Characteristics

### Table 7. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{BR\text{DSS}}$</td>
<td>drain-source breakdown voltage</td>
<td>$I_D = 250$ µA; $V_{GS} = 0$ V; $T_J = 25$ °C</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250$ µA; $V_{GS} = 0$ V; $T_J = -55$ °C</td>
<td>27</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS(th)}$</td>
<td>gate-source threshold voltage</td>
<td>$I_D = 1$ mA; $V_{DS} = V_{GS}$; $T_J = 25$ °C</td>
<td>1.2</td>
<td>1.7</td>
<td>2.2</td>
<td>V</td>
</tr>
</tbody>
</table>
### Symbol \( \Delta V_{GS(th)}/\Delta T \)
- **Parameter**: gate-source threshold voltage variation with temperature
- **Conditions**: \( 25^\circ C < T_j < 150^\circ C \)
- **Min**: -3.8 mV/K

### Symbol \( I_{DSS} \)
- **Parameter**: drain leakage current
- **Conditions**:
  - \( V_{DS} = 24 \, \text{V}; \, V_{GS} = 0 \, \text{V}; \, T_j = 25 \, ^\circ \text{C} \)
  - \( V_{DS} = 24 \, \text{V}; \, V_{GS} = 0 \, \text{V}; \, T_j = 125 \, ^\circ \text{C} \)
- **Min**: -230 \( \mu \text{A} \)
- **Typ**: 1 \( \mu \text{A} \)
- **Max**: 100 \( \text{nA} \)

### Symbol \( I_{GSS} \)
- **Parameter**: gate leakage current
- **Conditions**:
  - \( V_{GS} = 16 \, \text{V}; \, V_{DS} = 0 \, \text{V}; \, T_j = 25 \, ^\circ \text{C} \)
  - \( V_{GS} = -16 \, \text{V}; \, V_{DS} = 0 \, \text{V}; \, T_j = 25 \, ^\circ \text{C} \)
- **Min**: -100 \( \text{nA} \)
- **Typ**: 100 \( \text{nA} \)
- **Max**: 100 \( \text{nA} \)

### Symbol \( R_{DS(on)} \)
- **Parameter**: drain-source on-state resistance
- **Conditions**:
  - \( V_{GS} = 4.5 \, \text{V}; \, I_D = 10 \, \text{A}; \, T_j = 25 \, ^\circ \text{C} \)
  - \( V_{GS} = 4.5 \, \text{V}; \, I_D = 10 \, \text{A}; \, T_j = 150 \, ^\circ \text{C} \)
  - \( V_{GS} = 10 \, \text{V}; \, I_D = 15 \, \text{A}; \, T_j = 25 \, ^\circ \text{C} \)
- **Min**: 8.1 \( \text{m}\Omega \)
- **Typ**: 10.2 \( \text{m}\Omega \)
- **Max**: 16.9 \( \text{m}\Omega \)

### Symbol \( R_G \)
- **Parameter**: gate resistance
- **Conditions**: \( f = 1 \, \text{MHz} \)
- **Min**: 0.25 \( \Omega \)

### Dynamic characteristics

### Symbol \( Q_G(tot) \)
- **Parameter**: total gate charge
- **Conditions**:
  - \( I_D = 15 \, \text{A}; \, V_{DS} = 15 \, \text{V}; \, V_{GS} = 10 \, \text{V} \)
  - \( I_D = 15 \, \text{A}; \, V_{DS} = 15 \, \text{V}; \, V_{GS} = 4.5 \, \text{V} \)
  - \( I_D = 0 \, \text{A}; \, V_{DS} = 0 \, \text{V}; \, V_{GS} = 10 \, \text{V} \)
- **Min**: 11.3 \( \text{nC} \)
- **Typ**: 5.5 \( \text{nC} \)
- **Max**: 10.2 \( \text{nC} \)

### Symbol \( Q_{GS} \)
- **Parameter**: gate-source charge
- **Conditions**:
  - \( I_D = 15 \, \text{A}; \, V_{DS} = 15 \, \text{V}; \, V_{GS} = 4.5 \, \text{V} \)
- **Min**: 1.97 \( \text{nC} \)

### Symbol \( Q_{GS(th)} \)
- **Parameter**: pre-threshold gate-source charge
- **Conditions**: \( V_{DS} = 15 \, \text{V}; \, V_{GS} = 0 \, \text{V}; \, f = 1 \, \text{MHz}; \, T_j = 25 \, ^\circ \text{C} \)
- **Min**: 1.14 \( \text{nC} \)

### Symbol \( Q_{GS(th-pl)} \)
- **Parameter**: post-threshold gate-source charge
- **Conditions**: \( V_{DS} = 15 \, \text{V}; \, V_{GS} = 4.5 \, \text{V}; \, f = 1 \, \text{MHz}; \, R_G = 5 \, \Omega \)
- **Min**: 0.83 \( \text{nC} \)

### Symbol \( Q_{GD} \)
- **Parameter**: gate-drain charge
- **Conditions**: \( V_{DS} = 15 \, \text{V}; \, V_{GS} = 0 \, \text{V}; \, f = 1 \, \text{MHz}; \, T_j = 25 \, ^\circ \text{C} \)
- **Min**: 1.7 \( \text{nC} \)

### Symbol \( V_{GS(pl)} \)
- **Parameter**: gate-source plateau voltage
- **Conditions**: \( I_D = 15 \, \text{A}; \, V_{DS} = 15 \, \text{V}; \, f = 1 \, \text{MHz} \)
- **Min**: 2.9 \( \text{V} \)

### Symbol \( C_{iss} \)
- **Parameter**: input capacitance
- **Conditions**: \( V_{DS} = 15 \, \text{V}; \, f = 1 \, \text{MHz}; \, T_j = 25 \, ^\circ \text{C} \)
- **Min**: 655 \( \text{pF} \)

### Symbol \( C_{oss} \)
- **Parameter**: output capacitance
- **Conditions**: \( T_j = 25 \, ^\circ \text{C} \)
- **Min**: 578 \( \text{pF} \)

### Symbol \( C_{rss} \)
- **Parameter**: reverse transfer capacitance
- **Min**: 50 \( \text{pF} \)

### Symbol \( t_{dl(on)} \)
- **Parameter**: turn-on delay time
- **Conditions**: \( V_{DS} = 15 \, \text{V}; \, R_L = 1 \, \Omega; \, V_{GS} = 4.5 \, \text{V}; \, R_{G(ex)} = 5 \, \Omega \)
- **Min**: 7.1 \( \text{ns} \)

### Symbol \( t_r \)
- **Parameter**: rise time
- **Min**: 10.4 \( \text{ns} \)

### Symbol \( t_{dl(off)} \)
- **Parameter**: turn-off delay time
- **Min**: 8.5 \( \text{ns} \)

### Symbol \( t_f \)
- **Parameter**: fall time
- **Min**: 5.5 \( \text{ns} \)
Nexperia

PSMN7R5-30YLD

N-channel 30 V, 7.5 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

Symbol | Parameter | Conditions | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | --- | ---
Q_{oss} | output charge | $V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \degree \text{ C}$ | - | 11 | - | nC

Source-drain diode

Symbol | Parameter | Conditions | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | --- | ---
$V_{SD}$ | source-drain voltage | $I_S = 10 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \degree \text{ C}; \text{ Fig. 15}$ | - | 0.82 | 1.2 | V
$t_{rr}$ | reverse recovery time | $I_S = 15 \text{ A}; dI_S/dt = -100 \text{ A/µs}; V_{GS} = 0 \text{ V}; V_{DS} = 15 \text{ V}; \text{ Fig. 16}$ | - | 23 | - | ns
$Q_r$ | recovered charge | [1] | - | 11 | - | nC
$t_a$ | reverse recovery rise time | - | 10 | - | ns
$t_b$ | reverse recovery fall time | - | 13 | - | ns
$S$ | softness factor | - | 1.3 | - |

[1] includes capacitive recovery

Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values $T_j = 25\degree \text{ C}$

Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values $T_j = 25\degree \text{ C}; I_D = 15\text{ A}$
PSMN7R5-30YLD

N-channel 30 V, 7.5 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

\[ V_{DS} = 10V \]

Fig. 10. Drain-source on-state resistance as a function of drain current; typical values

\[ T_J = 25^\circ C \]

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature

\[ \alpha = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ C)} \]

Fig. 12. Gate charge waveform definitions
Fig. 13. Gate-source voltage as a function of gate charge; typical values

\[ V_{GS} = 25°C \; V, \; I_D = 15A \]

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

\[ V_{GS} = 0V, \; f = 1MHz \]

Fig. 15. Source current as a function of source-drain voltage; typical values

\[ I_S = 0A \]

Fig. 16. Reverse recovery timing definition
11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads

<table>
<thead>
<tr>
<th>Unit(1)</th>
<th>A</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>b</th>
<th>b2</th>
<th>b3</th>
<th>b4</th>
<th>c</th>
<th>c2</th>
<th>D(1)</th>
<th>D1(1)</th>
<th>E(1)</th>
<th>E1(1)</th>
<th>e</th>
<th>H</th>
<th>L</th>
<th>L1</th>
<th>L2</th>
<th>w</th>
<th>y</th>
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<tbody>
<tr>
<td>max</td>
<td>1.20</td>
<td>0.15</td>
<td>1.10</td>
<td>0.50</td>
<td>4.41</td>
<td>2.2</td>
<td>0.9</td>
<td>0.25</td>
<td>0.30</td>
<td>4.10</td>
<td>4.20</td>
<td>5.0</td>
<td>3.3</td>
<td>1.27</td>
<td>6.2</td>
<td>0.85</td>
<td>1.3</td>
<td>1.3</td>
<td>0.25</td>
<td>0.1</td>
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<td>min</td>
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<td>4.01</td>
<td>3.1</td>
<td>5.8</td>
<td>5.8</td>
<td>0.40</td>
<td>0.8</td>
<td>0.8</td>
<td>0.25</td>
<td>0.1</td>
<td></td>
</tr>
</tbody>
</table>

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)
12. Legal information

12.1 Data sheet status

<table>
<thead>
<tr>
<th>Document status</th>
<th>Product status</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
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<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Preliminary [short] data sheet</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Product [short] data sheet</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
</table>

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term "short data sheet" is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

12.2 Definitions

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