



PSMN3R3-100SSF

NextPower 100 V, 3.3 mΩ, 190 Amp, N-channel MOSFET in LFAK88 package

9 June 2020

Objective data sheet

1. General description

NextPower 100 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- 190 Amps $I_{D(max)}$ continuous current rating
- Low $Q_G \times R_{DS(on)}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFAK88 package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in DC-DC
- BLDC motor control
- Full-bridge and half-bridge applications
- Battery protection

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	190	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	341	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	2.56	3.3	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C}$	-	4.1	5.3	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 10\text{ V}$	[tbd]	20	[tbd]	nC
$Q_{G(tot)}$	total gate charge		[tbd]	101	[tbd]	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 62\text{ A}; V_{sup} \leq 100\text{ V}; R_{GS} = 50\text{ Ω}; V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; \text{unclamped}; \text{Fig. 2}$	[1]	-	478	mJ

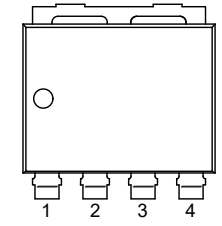
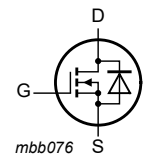
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
Q _r	recovered charge	I _S = 25 A; di _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; Fig. 3	-	57	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LPAK88 (SOT1235)</p>	
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R3-100SSF	LPAK88	plastic, single-ended surface-mounted package (LPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Limiting values

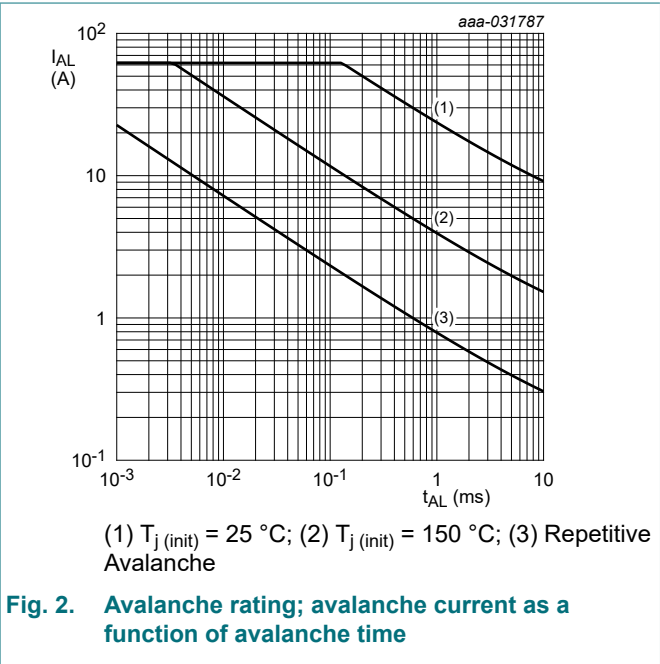
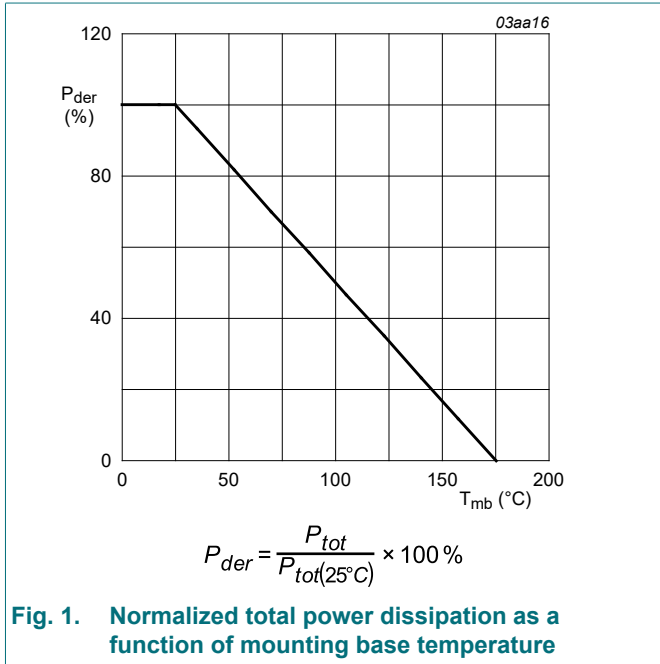
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	100	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	100	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	341	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C	-	190	A
		V _{GS} = 10 V; T _{mb} = 100 °C	-	151	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	760	A
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{sld(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	190	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	760	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 62 \text{ A}$; $V_{sup} \leq 100 \text{ V}$; $R_{GS} = 50 \Omega$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; unclamped; Fig. 2	[1]	-	478	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 100 \text{ V}$; $V_{GS} = 10 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; $R_{GS} = 50 \Omega$; Fig. 2	[1]	-	62	A

[1] Protected by 100% test



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	[tbd]	0.44	K/W

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$; $V_{GS} = 0 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	100	-	-	V
		$I_D = 250 \mu\text{A}$; $V_{GS} = 0 \text{ V}$; $T_j = -55 \text{ }^\circ\text{C}$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$; $V_{DS}=V_{GS}$; $T_j = 25 \text{ }^\circ\text{C}$	2	3	4	V
		$I_D = 1 \text{ mA}$; $V_{DS}=V_{GS}$; $T_j = -55 \text{ }^\circ\text{C}$	-	3.5	-	V
		$I_D = 1 \text{ mA}$; $V_{DS}=V_{GS}$; $T_j = 175 \text{ }^\circ\text{C}$	-	1.6	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C}$	-	-8.4	-	mV/K

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	0.1	25	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 125 °C	-	-	100	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C	-	2.56	3.3	mΩ
		V _{GS} = 7 V; I _D = 25 A; T _j = 25 °C	-	3.6	4.5	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C	-	4.1	5.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C	-	5.8	7.5	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C	[tbd]	0.74	[tbd]	Ω
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V	[tbd]	101	[tbd]	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V	-	55	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 50 V; V _{GS} = 10 V	[tbd]	30	[tbd]	nC
Q _{GS(th)}	pre-threshold gate-source charge		-	20	-	nC
Q _{GS(th-pl)}	post-threshold gate-source charge		-	10	-	nC
Q _{GD}	gate-drain charge		[tbd]	20	[tbd]	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 50 V	-	4.5	-	V
C _{iss}	input capacitance	V _{DS} = 50 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C	[tbd]	7224	[tbd]	pF
C _{oss}	output capacitance		[tbd]	1700	[tbd]	pF
C _{rss}	reverse transfer capacitance		[tbd]	29	[tbd]	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 2 Ω; V _{GS} = 10 V; R _{G(ext)} = 5 Ω	-	27	-	ns
t _r	rise time		-	23	-	ns
t _{d(off)}	turn-off delay time		-	59	-	ns
t _f	fall time		-	32	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C	-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; Fig. 3	-	56	-	ns
Q _r	recovered charge		-	57	-	nC

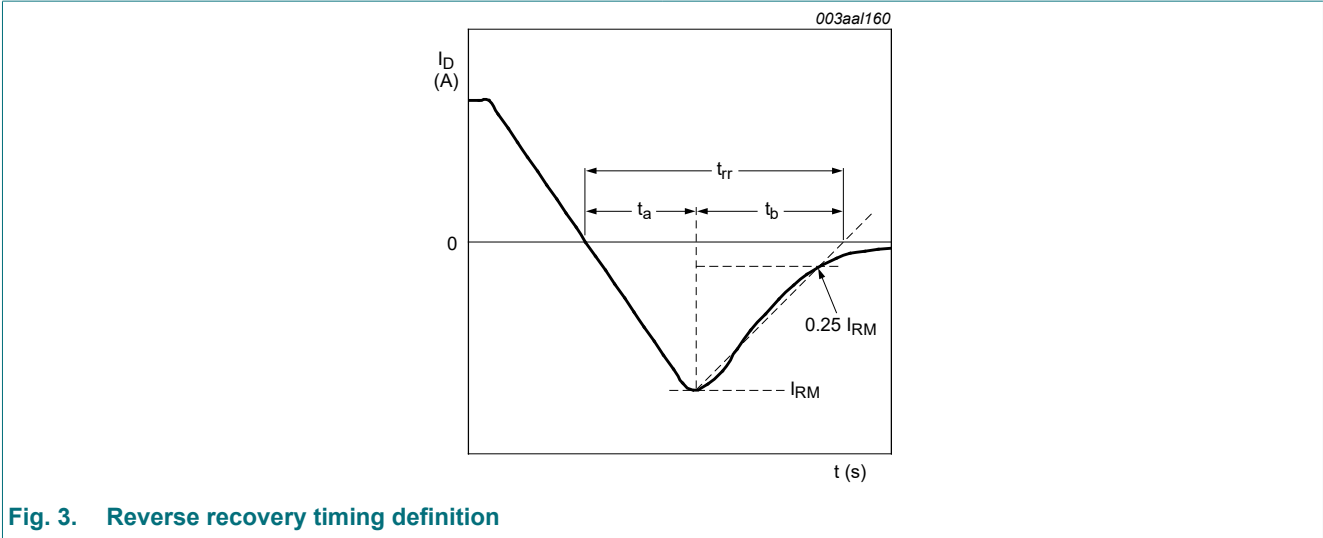


Fig. 3. Reverse recovery timing definition

10. Package outline

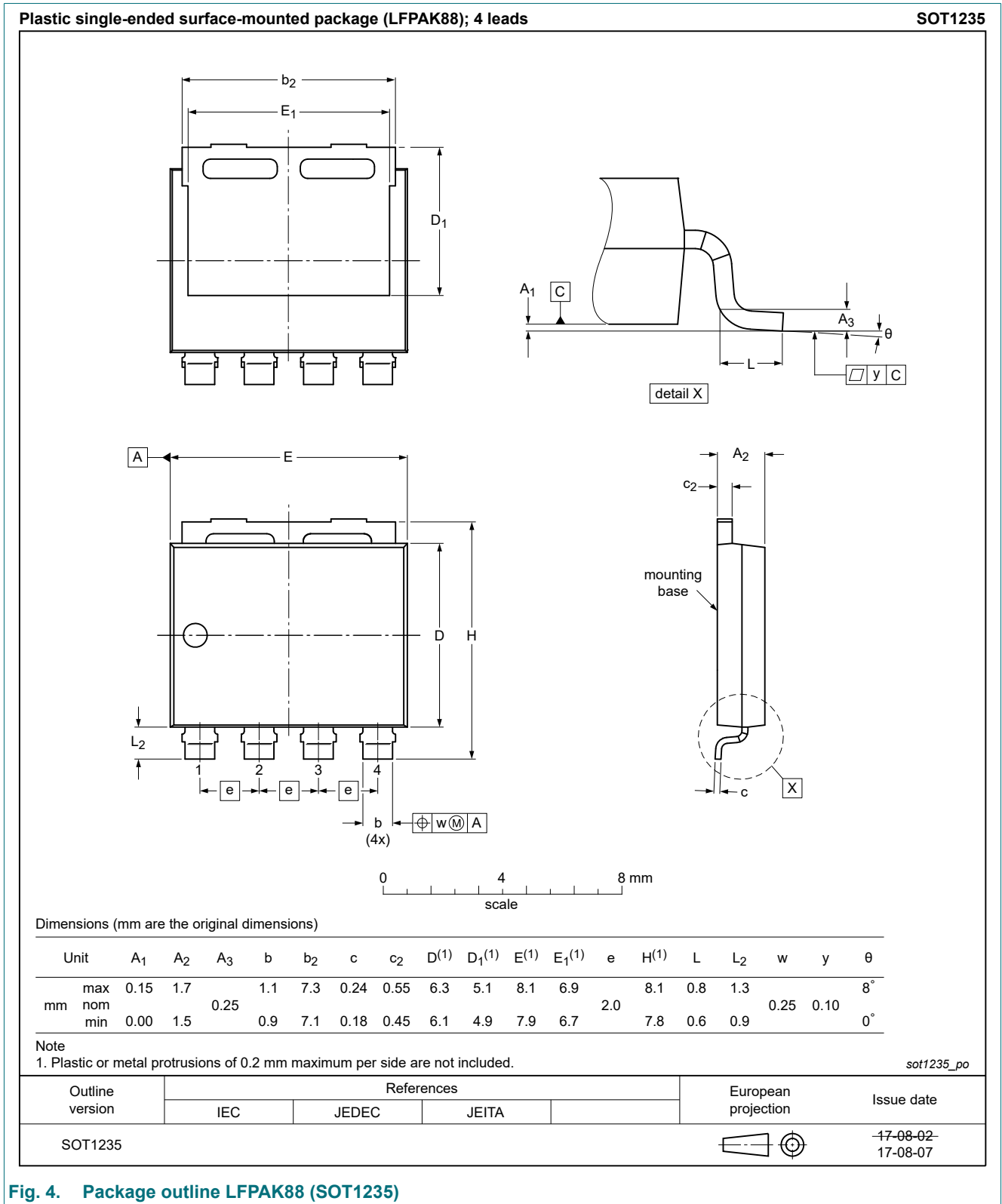


Fig. 4. Package outline LPAK88 (SOT1235)

11. Soldering

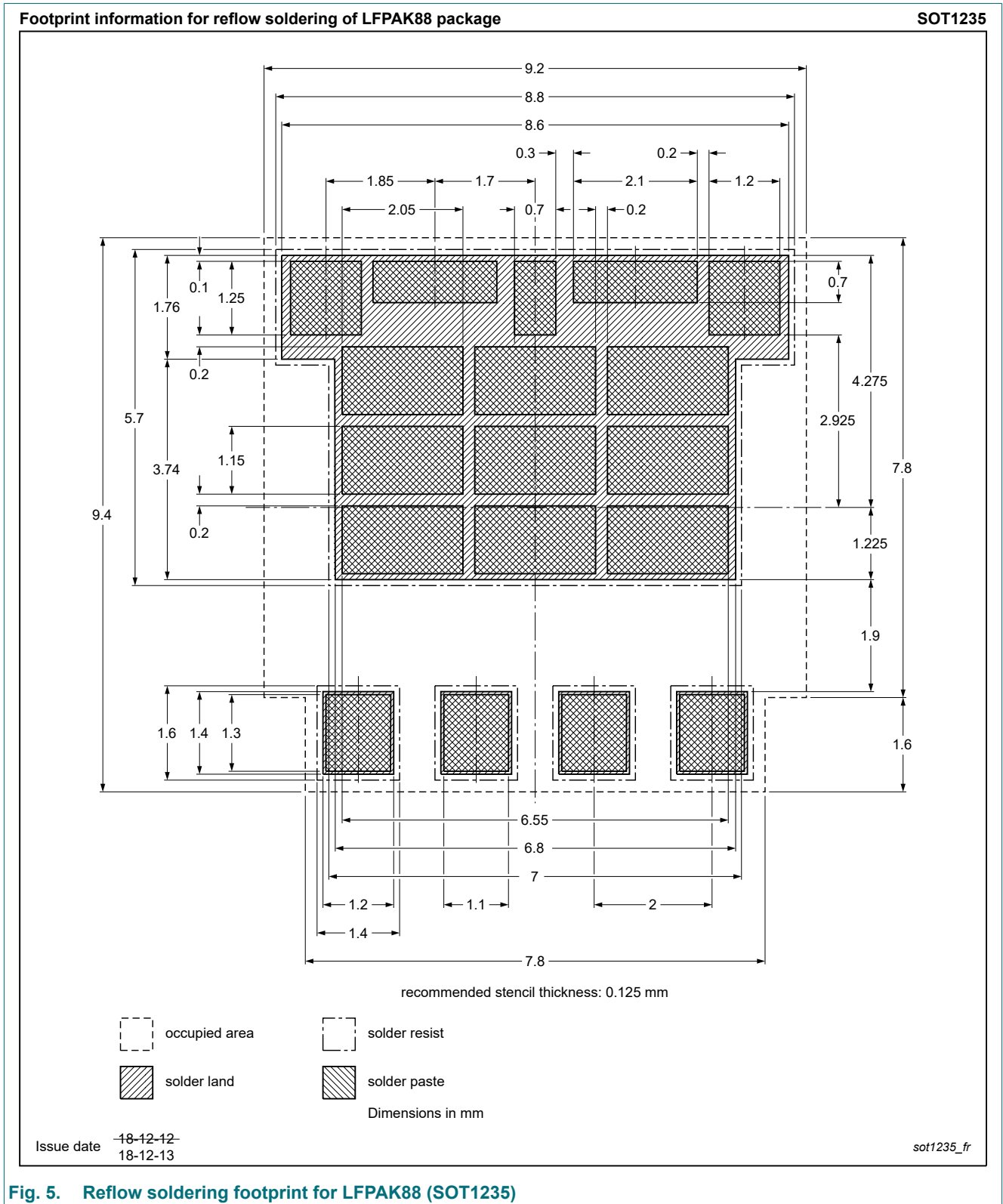


Fig. 5. Reflow soldering footprint for LPAK88 (SOT1235)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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