1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LFPAK56 package. NextPowerS3 portfolio utilising Nexperia’s unique “SchottkyPlus” technology delivers high efficiency, low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

2. Features and benefits

- Ultra low $Q_G$, $Q_{GD}$ and $Q_{OSS}$ for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery; s-factor > 1
- Low spiking and ringing for low EMI designs
- Unique “SchottkyPlus” technology; Schottky-like performance with < 1µA leakage at 25 °C
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to 175 °C
- Wave solderable; exposed leads for optimal visual solder inspection

3. Applications

- On-board DC-to-DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 , ^\circ!C \leq T_j \leq 175 , ^\circ!C$</td>
<td>-</td>
<td>-</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>$I_D$</td>
<td>drain current</td>
<td>$T_{mb} = 25 , ^\circ!C$; $V_{GS} = 10 , V$; [1]</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>A</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 , ^\circ!C$; [Fig. 1]</td>
<td>-</td>
<td>-</td>
<td>106</td>
<td>W</td>
</tr>
</tbody>
</table>
Nexperia

PSMN2R4-30YLD

N-channel 30 V, 2.4 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

Symbol | Parameter | Conditions | Min | Typ | Max | Unit
---|---|---|---|---|---|---
T<sub>j</sub> | junction temperature | -55 | - | 175 | °C

Static characteristics

Symbol | Parameter | Conditions | Min | Typ | Max | Unit
---|---|---|---|---|---|---
R<sub>DSon</sub> | drain-source on-state resistance | V<sub>GS</sub> = 4.5 V; I<sub>D</sub> = 25 A; T<sub>j</sub> = 25 °C; V<sub>GS</sub> = 10 V; I<sub>D</sub> = 25 A; T<sub>j</sub> = 25 °C; | - | 2.7 | 3.1 | mΩ

Dynamic characteristics

Symbol | Parameter | Conditions | Min | Typ | Max | Unit
---|---|---|---|---|---|---
Q<sub>GD</sub> | gate-drain charge | V<sub>GS</sub> = 4.5 V; I<sub>D</sub> = 25 A; V<sub>DS</sub> = 15 V; | - | 4.3 | - | nC
Q<sub>G(tot)</sub> | total gate charge | V<sub>GS</sub> = 4.5 V; I<sub>D</sub> = 25 A; V<sub>DS</sub> = 15 V; | - | 16.2 | - | nC

Source-drain diode

Symbol | Parameter | Conditions | Min | Typ | Max | Unit
---|---|---|---|---|---|---
S | softness factor | I<sub>S</sub> 25 A; V<sub>GS</sub> = 0 V; dI<sub>S</sub>/dt = -100 A/s; V<sub>DS</sub> = 15 V; | - | 1 | - |

[1] Continuous current is limited by package

5. Pinning information

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
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</thead>
<tbody>
<tr>
<td>1</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>G</td>
<td>gate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mb</td>
<td>D</td>
<td>mounting base; connected to drain</td>
<td></td>
<td></td>
</tr>
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6. Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
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</thead>
<tbody>
<tr>
<td>PSMN2R4-30YLD</td>
<td>LFPAK56; Power-SO8</td>
<td>Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads</td>
<td>SOT669</td>
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</tr>
</tbody>
</table>
7. Marking

Table 4. Marking codes

<table>
<thead>
<tr>
<th>Type number</th>
<th>Marking code</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSMN2R4-30YLD</td>
<td>2D430L</td>
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</tbody>
</table>

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 , ^\circ C \leq T_j \leq 175 , ^\circ C$</td>
<td>-</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DGR}$</td>
<td>drain-gate voltage</td>
<td>$25 , ^\circ C \leq T_j \leq 175 , ^\circ C$; $R_{GS} = 20 , k\Omega$</td>
<td>-</td>
<td>30</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>gate-source voltage</td>
<td>$-20$ to $20$ V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$P_{\text{tot}}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 , ^\circ C$; <strong>Fig. 1</strong></td>
<td>-</td>
<td>106</td>
<td>W</td>
</tr>
<tr>
<td>$I_D$</td>
<td>drain current</td>
<td>$V_{GS} = 10 , V$; $T_{mb} = 25 , ^\circ C$; <strong>Fig. 2</strong></td>
<td>-</td>
<td>100</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 10 , V$; $T_{mb} = 100 , ^\circ C$; <strong>Fig. 2</strong></td>
<td>-</td>
<td>100</td>
<td>A</td>
</tr>
<tr>
<td>$I_{DM}$</td>
<td>peak drain current</td>
<td>pulsed; $t_p \leq 10 , \mu s$; $T_{mb} = 25 , ^\circ C$; <strong>Fig. 3</strong></td>
<td>-</td>
<td>625</td>
<td>A</td>
</tr>
<tr>
<td>$T_{\text{slg}}$</td>
<td>storage temperature</td>
<td>$-55$ to $175$ °C</td>
<td>-</td>
<td>175</td>
<td>°C</td>
</tr>
<tr>
<td>$T_J$</td>
<td>junction temperature</td>
<td>$-55$ to $175$ °C</td>
<td>-</td>
<td>175</td>
<td>°C</td>
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<tr>
<td>$T_{\text{sld(M)}}$</td>
<td>peak soldering temperature</td>
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<td>-</td>
<td>260</td>
<td>°C</td>
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<tr>
<td>$V_{\text{ESD}}$</td>
<td>electrostatic discharge voltage</td>
<td>HBM (JEDEC JESD22-A114)</td>
<td>750</td>
<td>-</td>
<td>V</td>
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</table>

**Source-drain diode**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_S$</td>
<td>source current</td>
<td>$T_{mb} = 25 , ^\circ C$</td>
<td>-</td>
<td>88</td>
<td>A</td>
</tr>
<tr>
<td>$I_{SM}$</td>
<td>peak source current</td>
<td>pulsed; $t_p \leq 10 , \mu s$; $T_{mb} = 25 , ^\circ C$</td>
<td>-</td>
<td>625</td>
<td>A</td>
</tr>
</tbody>
</table>

**Avalanche ruggedness**

| $E_{DS(\text{AL})S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10 \, V$; $T_{\text{j(init)}} = 25 \, ^\circ C$; $I_D = 25 \, A$; $V_{sup} \leq 30 \, V$; $R_{GS} = 50 \, \Omega$; unclamped; $t_p = 446 \, \mu s$ | 217 | mJ   |

[1] Continuous current is limited by package
[2] Protected by 100% test
Nexperia

PSMN2R4-30YLD

N-channel 30 V, 2.4 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

---

Fig. 1. Normalized total power dissipation as a function of mounting base temperature

\[ P_{\text{der}} = \frac{P_{\text{tot}}}{P_{\text{tot},25\degree C}} \times 100\% \]

Fig. 2. Continuous drain current as a function of mounting base temperature

(1) Capped at 100A due to package

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

\[ T_{mb} = 25^\circ C; I_{DM} \text{ is a single pulse} \]

9. Thermal characteristics

Table 6. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{\text{th(j-mb)}} )</td>
<td>thermal resistance from junction to mounting base</td>
<td>( \text{Fig. 4} )</td>
<td>-</td>
<td>1.25</td>
<td>1.42</td>
<td>K/W</td>
</tr>
</tbody>
</table>

---

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Product data sheet 7 February 2014
### Table 7. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th(j-a)}$</td>
<td>thermal resistance from junction to ambient</td>
<td>Fig. 5</td>
<td>-</td>
<td>50</td>
<td>-</td>
<td>K/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fig. 6</td>
<td>-</td>
<td>125</td>
<td>-</td>
<td>K/W</td>
</tr>
<tr>
<td>$Z_{th(j-mb)}$ (K/W)</td>
<td></td>
<td>Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{(BR)DSS}$</td>
<td>drain-source breakdown voltage</td>
<td>$I_D = 250 \mu A; \ V_{GS} = 0 \ V; \ T_j = 25 ^\circ C$</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 \mu A; \ V_{GS} = 0 \ V; \ T_j = -55 ^\circ C$</td>
<td>27</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS(th)}$</td>
<td>gate-source threshold voltage</td>
<td>$I_D = 1 \ mA; \ V_{DS} = V_{GS}; \ T_j = 25 ^\circ C$</td>
<td>1.2</td>
<td>1.7</td>
<td>2.2</td>
<td>V</td>
</tr>
</tbody>
</table>
### Symbol | Parameter | Conditions | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | --- | ---
$\Delta V_{GS(\text{th})}/\Delta T$ | gate-source threshold voltage variation with temperature | $25 \, ^\circ\text{C} \leq T_j \leq 150 \, ^\circ\text{C}$ | - | -4.5 | - | mV/K
$I_{DSS}$ | drain leakage current | $V_{DS} = 24 \, \text{V}; V_{GS} = 0 \, \text{V}; T_j = 25 \, ^\circ\text{C}$ | - | - | 1 | µA
 | | $V_{DS} = 24 \, \text{V}; V_{GS} = 0 \, \text{V}; T_j = 125 \, ^\circ\text{C}$ | - | 0.92 | - | µA
$I_{GSS}$ | gate leakage current | $V_{GS} = 16 \, \text{V}; V_{DS} = 0 \, \text{V}; T_j = 25 \, ^\circ\text{C}$ | - | - | 100 | nA
 | | $V_{GS} = -16 \, \text{V}; V_{DS} = 0 \, \text{V}; T_j = 25 \, ^\circ\text{C}$ | - | - | 100 | nA
$R_{DSon}$ | drain-source on-state resistance | $V_{GS} = 4.5 \, \text{V}; I_D = 25 \, \text{A}; T_j = 25 \, ^\circ\text{C}$; Fig. 10 | - | 2.7 | 3.1 | mΩ
 | | $V_{GS} = 4.5 \, \text{V}; I_D = 25 \, \text{A}; T_j = 150 \, ^\circ\text{C}$; Fig. 11; Fig. 10 | - | - | 5.1 | mΩ
 | | $V_{GS} = 10 \, \text{V}; I_D = 25 \, \text{A}; T_j = 25 \, ^\circ\text{C}$; Fig. 11 | - | 2 | 2.4 | mΩ
 | | $V_{GS} = 10 \, \text{V}; I_D = 25 \, \text{A}; T_j = 150 \, ^\circ\text{C}$; Fig. 11; Fig. 10 | - | - | 4 | mΩ
$R_G$ | gate resistance | $f = 1 \, \text{MHz}$ | - | 0.78 | - | Ω

### Dynamic characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | --- | ---
$Q_{G(tot)}$ | total gate charge | $I_D = 25 \, \text{A}; V_{DS} = 15 \, \text{V}; V_{GS} = 10 \, \text{V}$; Fig. 12; Fig. 13 | - | 31.3 | - | nC
 | | $I_D = 25 \, \text{A}; V_{DS} = 15 \, \text{V}; V_{GS} = 4.5 \, \text{V}$; Fig. 12; Fig. 13 | - | 16.2 | - | nC
 | | $I_D = 0 \, \text{A}; V_{DS} = 0 \, \text{V}; V_{GS} = 10 \, \text{V}$ | - | 29.3 | - | nC
$Q_{GS}$ | gate-source charge | $I_D = 25 \, \text{A}; V_{DS} = 15 \, \text{V}; V_{GS} = 4.5 \, \text{V}$; Fig. 12; Fig. 13 | - | 4.8 | - | nC
$Q_{GS(th)}$ | pre-threshold gate-source charge | | - | 3 | - | nC
$Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 1.8 | - | nC
$Q_{GD}$ | gate-drain charge | | - | 4.3 | - | nC
$V_{GS(pl)}$ | gate-source plateau voltage | $I_D = 25 \, \text{A}; V_{DS} = 15 \, \text{V}$; Fig. 12; Fig. 13 | - | 2.6 | - | V
$C_{iss}$ | input capacitance | $V_{DS} = 15 \, \text{V}; V_{GS} = 0 \, \text{V}; f = 1 \, \text{MHz}$; $T_j = 25 \, ^\circ\text{C}$; Fig. 14 | - | 2256 | - | pF
$C_{oss}$ | output capacitance | | - | 1175 | - | pF
$C_{rss}$ | reverse transfer capacitance | | - | 155 | - | pF
$t_{d(on)}$ | turn-on delay time | $V_{DS} = 15 \, \text{V}; R_L = 0.6 \, \Omega; V_{GS} = 4.5 \, \text{V}$; $R_{G(ex)} = 5 \, \Omega$ | - | 16.3 | - | ns
$t_r$ | rise time | | - | 27.5 | - | ns
$t_{d(off)}$ | turn-off delay time | | - | 17.4 | - | ns
$t_f$ | fall time | | - | 13.9 | - | ns
**Nexperia**

**PSMN2R4-30YLD**

N-channel 30 V, 2.4 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Q_{oss}</td>
<td>output charge</td>
<td>V_{GS} = 0 V; V_{DS} = 15 V; f = 1 MHz; T_{j} = 25 °C</td>
<td>-</td>
<td>24.8</td>
<td>-</td>
<td>nC</td>
</tr>
</tbody>
</table>

**Source-drain diode**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{SD}</td>
<td>source-drain voltage</td>
<td>I_S = 25 A; V_{GS} = 0 V; T_{j} = 25 °C; [Fig. 15]</td>
<td>-</td>
<td>0.81</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>t_{rr}</td>
<td>reverse recovery time</td>
<td>I_S = 25 A; dI_S/dt = -100 A/s; V_{GS} = 0 V; V_{DS} = 15 V; [Fig. 15]</td>
<td>-</td>
<td>30.3</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>Q_{r}</td>
<td>recovered charge</td>
<td>V_{DS} = 15 V; [Fig. 15]</td>
<td>[1]</td>
<td>20</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>t_{a}</td>
<td>reverse recovery rise time</td>
<td>-</td>
<td>-</td>
<td>15</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>t_{b}</td>
<td>reverse recovery fall time</td>
<td>-</td>
<td>-</td>
<td>15</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>S</td>
<td>softness factor</td>
<td></td>
<td>-</td>
<td>1</td>
<td>-</td>
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</tbody>
</table>

[1] Includes capacitive recovery

**Fig. 7.** Output characteristics; drain current as a function of drain-source voltage; typical values

**Fig. 8.** Drain-source on-state resistance as a function of gate-source voltage; typical values

\[ I_D = 25^\circ C \]

\[ T_{j} = 25^\circ C; \ I_D = 25 A \]
**Nexperia**

**PSMN2R4-30YLD**

N-channel 30 V, 2.4 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

---

**Fig. 9.** Transfer characteristics; drain current as a function of gate-source voltage; typical values

\[ V_{DS} = 10V \]

**Fig. 10.** Drain-source on-state resistance as a function of drain current; typical values

\[ T_J = 25^\circ C \]

**Fig. 11.** Normalized drain-source on-state resistance factor as a function of junction temperature

\[ \eta = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ C)} \]

**Fig. 12.** Gate charge waveform definitions
**PSMN2R4-30YLD**

N-channel 30 V, 2.4 mΩ logic level MOSFET in LFPAK56 using NextPowerS3 Technology

---

**Fig. 13.** Gate-source voltage as a function of gate charge; typical values

\[ V_{GS} = 25^\circ C, \quad I_D = 25A \]

**Fig. 14.** Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

\[ V_{GS} = 0V, \quad f = 1MHz \]

**Fig. 15.** Source current as a function of source-drain voltage; typical values

\[ V_{GS} = 0V \]
11. Package outline

Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads

Dimensions (mm are the original dimensions)

<table>
<thead>
<tr>
<th>Unit(1)</th>
<th>A</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>b</th>
<th>b2</th>
<th>b3</th>
<th>b4</th>
<th>c</th>
<th>c2</th>
<th>D(1)</th>
<th>D1(1)</th>
<th>E(1)</th>
<th>E1(1)</th>
<th>e</th>
<th>H</th>
<th>L</th>
<th>L1</th>
<th>L2</th>
<th>w</th>
<th>y</th>
</tr>
</thead>
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<tr>
<td>max</td>
<td>1.20</td>
<td>0.15</td>
<td>1.10</td>
<td></td>
<td>0.50</td>
<td>4.41</td>
<td>2.2</td>
<td>0.9</td>
<td>0.25</td>
<td>0.30</td>
<td>4.10</td>
<td>4.20</td>
<td>5.0</td>
<td>3.3</td>
<td>1.27</td>
<td>6.2</td>
<td>0.85</td>
<td>1.3</td>
<td>1.3</td>
<td>0.25</td>
<td>0.1</td>
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<td>nom</td>
<td>1.01</td>
<td>0.00</td>
<td>0.96</td>
<td></td>
<td>0.35</td>
<td>3.62</td>
<td>2.0</td>
<td>0.7</td>
<td>0.19</td>
<td>0.24</td>
<td>3.80</td>
<td>4.8</td>
<td>3.1</td>
<td></td>
<td>5.8</td>
<td>0.40</td>
<td>0.8</td>
<td>0.8</td>
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<td></td>
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</tr>
</tbody>
</table>

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

Fig. 16. Package outline LFPAK56; Power-SO8 (SOT669)
12. Legal information

12.1 Data sheet status

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
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<tbody>
<tr>
<td>Objective [short] data sheet</td>
<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Preliminary [short] data sheet</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Product [short] data sheet</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
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[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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