



PSMN2R3-80SSF

NextPower 80 V, 2.3 mΩ, 190 Amp, N-channel MOSFET in LFPAK88 package

16 April 2021

Objective data sheet

1. General description

NextPower 80 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- 190 Amps $I_{D(max)}$ continuous current rating
- Low $Q_G \times R_{DS(on)}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFPAK88 package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in DC-DC
- BLDC motor control
- Full-bridge and half-bridge applications
- Battery protection

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	190	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	341	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	1.84	2.3	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C}$	-	2.91	3.7	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 40\text{ V}; V_{GS} = 10\text{ V}; \text{Fig. 4}$	[tbd]	25	[tbd]	nC
$Q_{G(tot)}$	total gate charge		[tbd]	131	[tbd]	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 80\text{ A}; V_{sup} \leq 80\text{ V}; R_{GS} = 50\text{ Ω}; V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; \text{unclamped}$	[1]	-	739	mJ

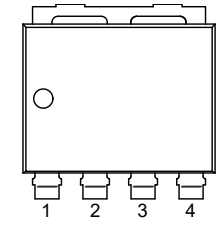
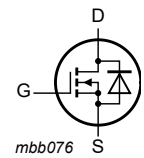
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
Q _r	recovered charge	I _S = 25 A; di _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 40 V	-	56	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LFAK88 (SOT1235)</p>	
2	S	Source		
3	S	Source		
4	S	Source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R3-80SSF	LFAK88	plastic, single-ended surface-mounted package (LFAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R3-80SSF	X2F3S80S

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	80	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	80	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	341	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C	-	190	A
		V _{GS} = 10 V; T _{mb} = 100 °C	-	135	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	760	A
T _{stg}	storage temperature		-55	175	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	175	°C
T _{slid(M)}	peak soldering temperature			-	260	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	190	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	760	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 80 A; V _{sup} ≤ 80 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped	[1]	-	739	mJ
I _{AS}	non-repetitive avalanche current	V _{sup} ≤ 100 V; V _{GS} = 10 V; T _{j(init)} = 25 °C; R _{GS} = 50 Ω	[1]	-	80	A

[1] Protected by 100% test

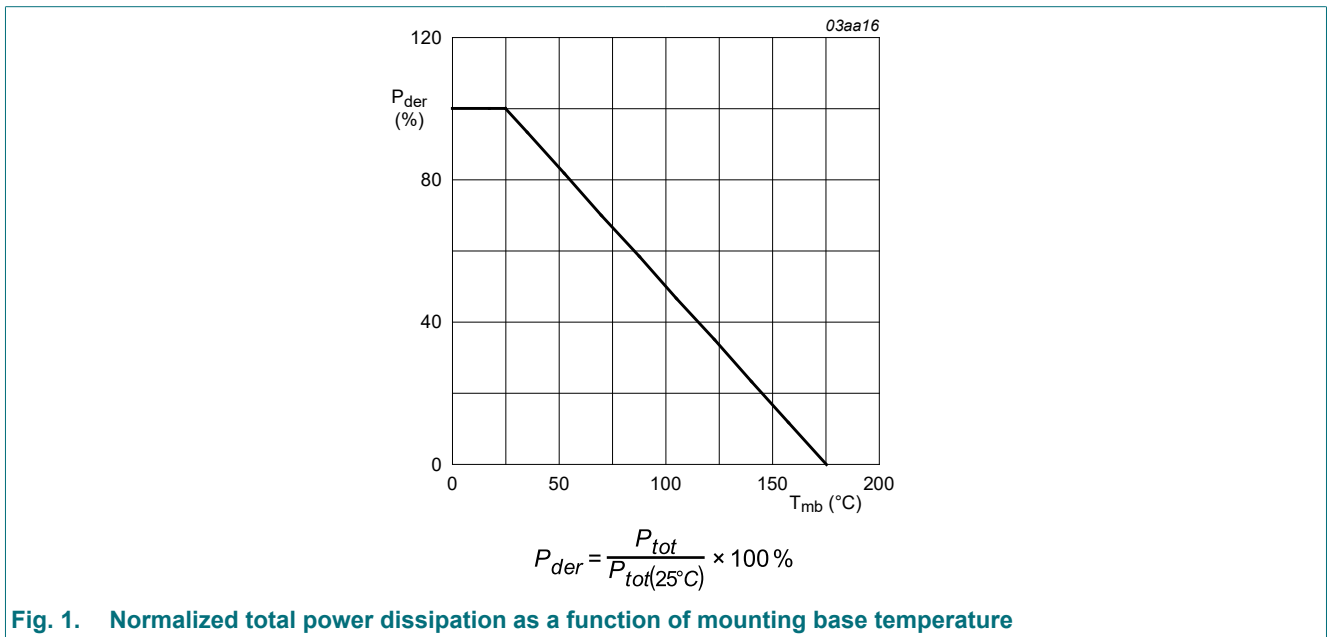
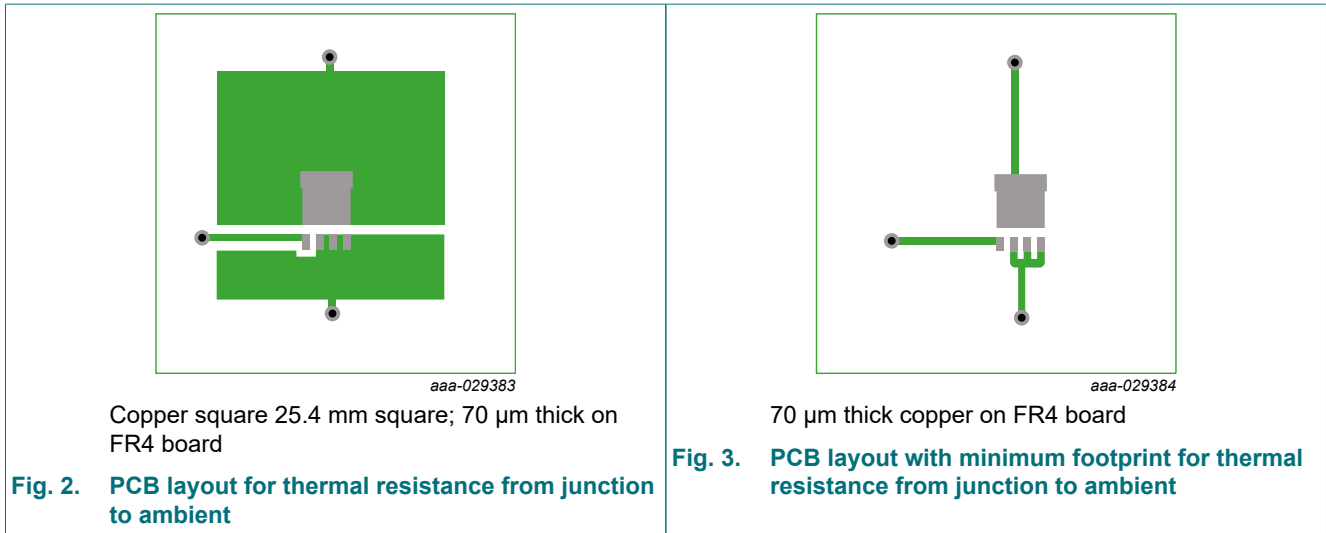


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base			-	[tbd]	0.44	K/W
R _{th(j-a)}	thermal resistance from junction to ambient	Fig. 2		-	35	-	K/W
		Fig. 3		-	70	-	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.5	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.6	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	[tbd]	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.06	25	μA
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.7	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.7	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$	-	1.84	2.3	mΩ
		$V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$	-	[tbd]	[tbd]	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C$	-	2.91	3.7	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$	-	4.07	5.2	mΩ
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	[tbd]	[tbd]	[tbd]	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 4	[tbd]	131	[tbd]	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 4	-	69	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ Fig. 4	[tbd]	41	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		[tbd]	27.2	[tbd]	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		[tbd]	14	[tbd]	nC
Q_{GD}	gate-drain charge		[tbd]	25	[tbd]	nC

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\text{ A}$; $V_{DS} = 40\text{ V}$; Fig. 4	-	4.5	-	V
C_{iss}	input capacitance	$V_{DS} = 40\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_j = 25\text{ °C}$	[tbd]	10057	[tbd]	pF
C_{oss}	output capacitance		[tbd]	2969	[tbd]	pF
C_{rss}	reverse transfer capacitance		[tbd]	54	[tbd]	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40\text{ V}$; $R_L = 1.6\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $R_{G(ext)} = 5\text{ }\Omega$	-	36	-	ns
t_r	rise time		-	31	-	ns
$t_{d(off)}$	turn-off delay time		-	80	-	ns
t_f	fall time		-	43	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$	-	-	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}$; $dI_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 40\text{ V}$	-	62	-	ns
Q_r	recovered charge		-	56	-	nC

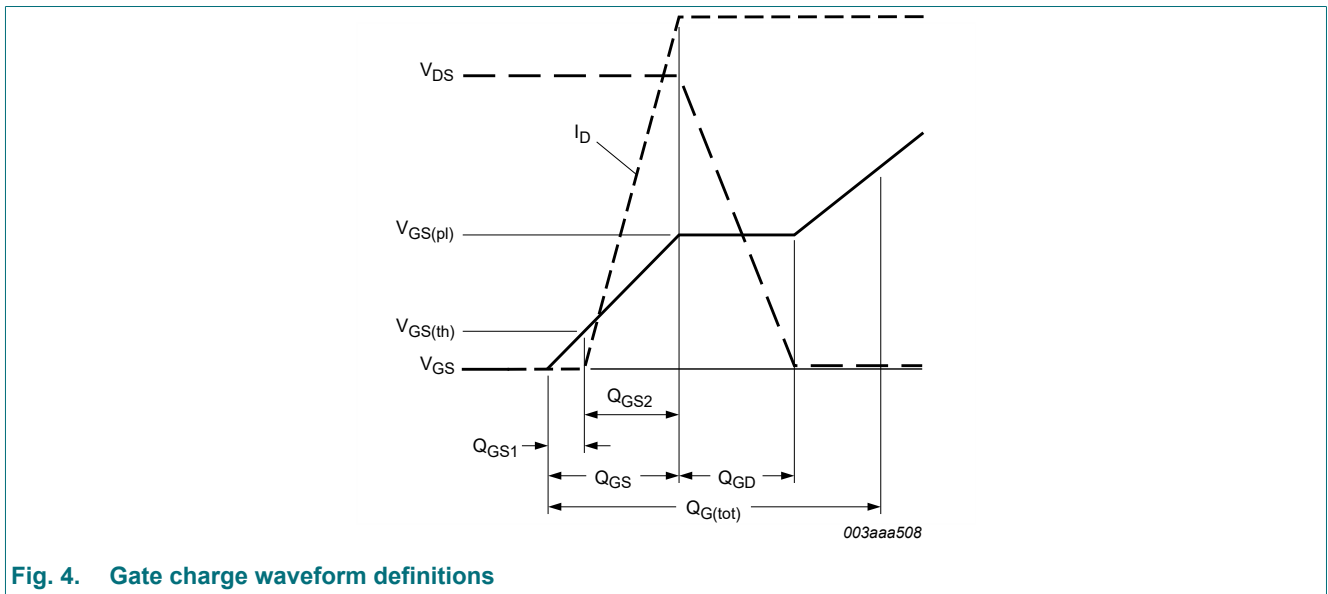


Fig. 4. Gate charge waveform definitions

11. Package outline

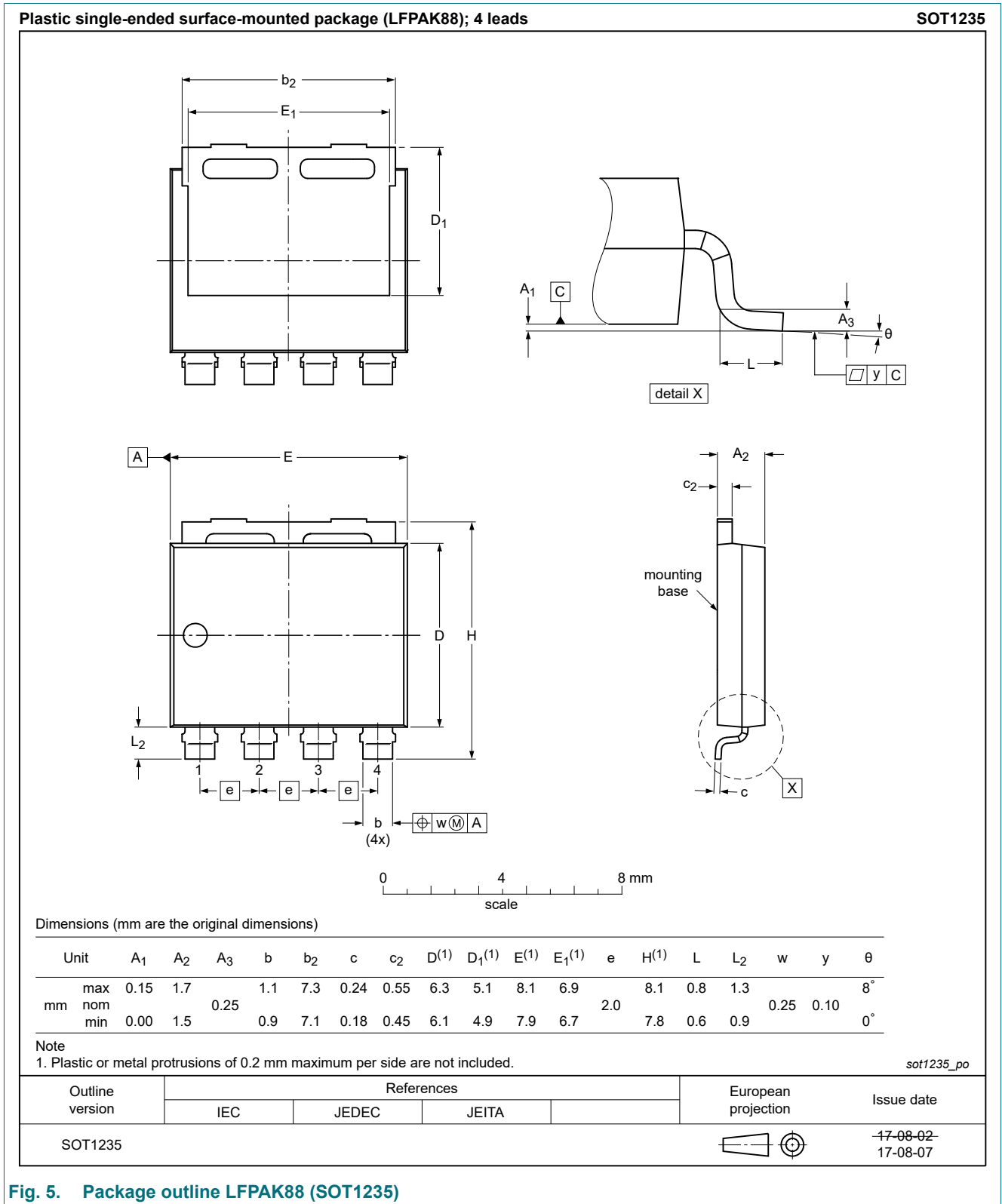


Fig. 5. Package outline LPAK88 (SOT1235)

12. Soldering

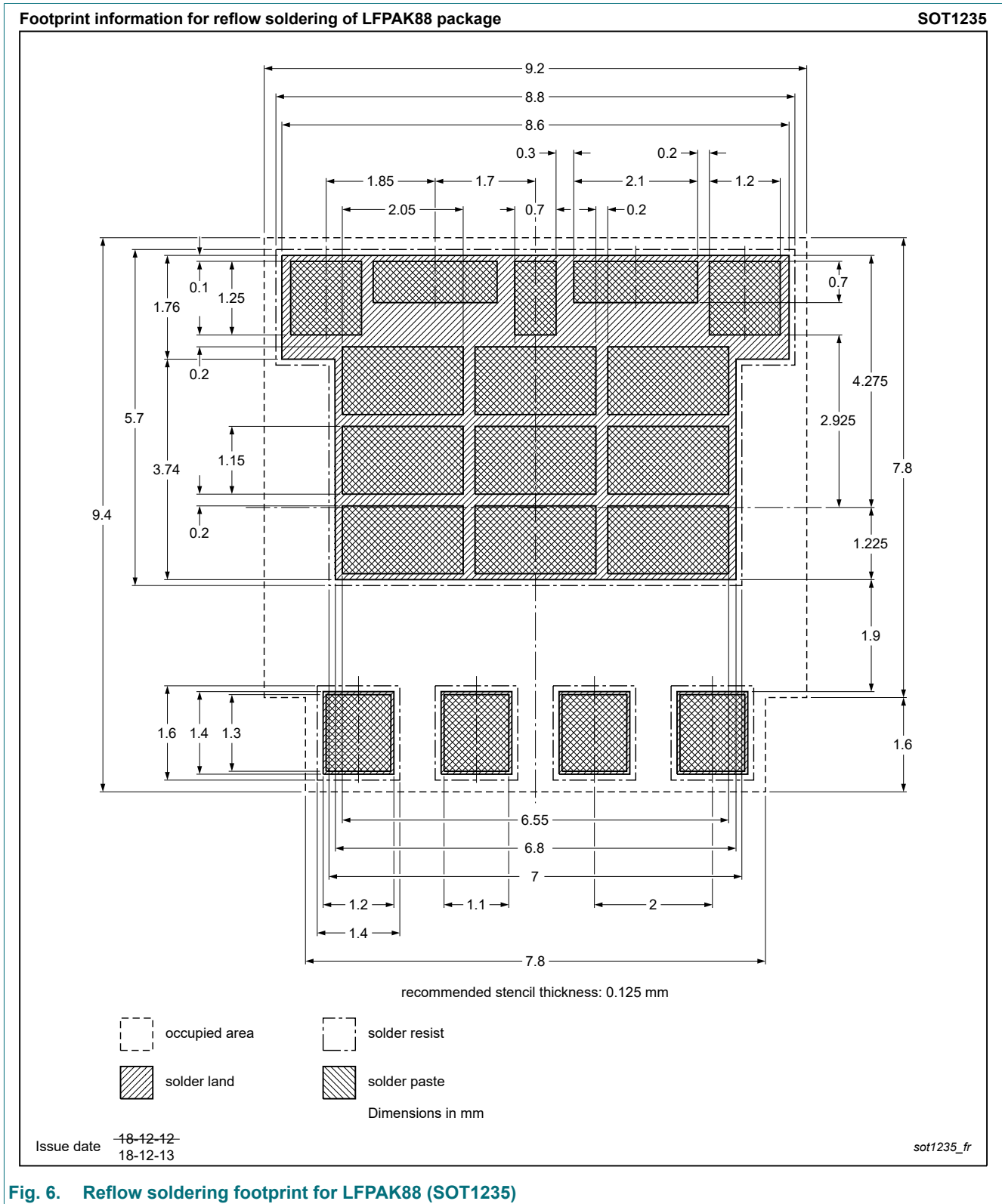


Fig. 6. Reflow soldering footprint for LPAK88 (SOT1235)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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