1. General description

N-channel enhancement mode MOSFET in a LFPAK88 package qualified to 175 °C. Part of Nexperia's Application Specific MOSFETs (ASFETs) for Hotswap and Soft Start. The PSMN2R3-100SSE delivers very low $R_{DSon}$ and enhanced safe operating area performance in a high-reliability copper-clip LFPAK88 package.

PSMN2R3-100SSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn-on, low $R_{DSon}$ to minimize $I^2R$ losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low $R_{DSon}$ for low $I^2R$ conduction losses
- LFPAK88 package for applications that demand the highest performance and reliability

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

<table>
<thead>
<tr>
<th>Table 1. Quick reference data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol</td>
</tr>
<tr>
<td>$V_{DS}$</td>
</tr>
<tr>
<td>$I_D$</td>
</tr>
<tr>
<td>$P_{tot}$</td>
</tr>
<tr>
<td>$T_j$</td>
</tr>
</tbody>
</table>

Static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS} = 10 \text{V}; I_D = 25 \text{A}; T_j = 25 \degree C$; [Fig. 11] | - | 1.8 | 2.28 | mΩ |

Dynamic characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
| $Q_{GD}$ | gate-drain charge | $I_D = 25 \text{A}; V_{DS} = 50 \text{V}; V_{GS} = 10 \text{V}$; [Fig. 14; Fig. 13] | 8 | 27 | 62 | nC |
| $Q_{G(tot)}$ | total gate charge | $I_D = 25 \text{A}; V_{DS} = 50 \text{V}; V_{GS} = 10 \text{V}$; [Fig. 13] | 80 | 161 | 242 | nC |
PSMN2R3-100SSE
N-channel 100 V, 2.3 mOhm MOSFET with enhanced SOA in LFPAK88

### Symbol | Parameter | Conditions | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | --- | ---

#### Avalanche ruggedness

**$E_{DS(AlS)}$**
non-repetitive drain-source avalanche energy

$I_D = 82 A; V_{sup} \leq 100 V; R_{GS} = 50 \Omega; V_{GS} = 10 V; T_{j(init)} = 25 ^\circ C; \text{unclamped}; t_p = 137 \mu s; \text{Fig. 4}$

[1] - - 732 mJ

#### Source-drain diode

**$Q_r$**
recovered charge

$\frac{dI_S}{dt} = -100 A/\mu s; V_{GS} = 0 V; V_{DS} = 50 V; \text{Fig. 18}$


[1] Protected by 100% test
[2] includes capacitive recovery

### 5. Pinning information

#### Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
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<tr>
<td>1</td>
<td>G</td>
<td>gate</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>S</td>
<td>source</td>
<td></td>
<td></td>
</tr>
<tr>
<td>mb</td>
<td>D</td>
<td>mounting base; connected to drain</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 6. Ordering information

#### Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
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</thead>
<tbody>
<tr>
<td>PSMN2R3-100SSE</td>
<td>LFPAK88</td>
<td>plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body</td>
<td>SOT1235</td>
<td></td>
</tr>
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### 7. Marking

#### Table 4. Marking codes

<table>
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<th>Type number</th>
<th>Marking code</th>
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</thead>
<tbody>
<tr>
<td>PSMN2R3-100SSE</td>
<td>X2E3S10S</td>
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</tbody>
</table>

### 8. Limiting values

#### Table 5. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 ^\circ C \leq T_j \leq 175 ^\circ C$</td>
<td>-</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DGR}$</td>
<td>drain-gate voltage</td>
<td>$25 ^\circ C \leq T_j \leq 175 ^\circ C; R_{GS} = 20 k\Omega$</td>
<td>-</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>gate-source voltage</td>
<td></td>
<td>-20</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 ^\circ C; \text{Fig. 1}$</td>
<td>-</td>
<td>341</td>
<td>W</td>
</tr>
</tbody>
</table>
**Symbol | Parameter | Conditions | Min | Max | Unit**
--- | --- | --- | --- | --- | ---
$I_D$ | drain current | $V_{GS} = 10 \text{ V}; T_{mb} = 25 ^\circ \text{C}; \text{Fig. 2}$ | - | 255 | A

|  |  | $V_{GS} = 10 \text{ V}; T_{mb} = 100 ^\circ \text{C}; \text{Fig. 2}$ | - | 180 | A

$I_{DM}$ | peak drain current | pulsed; $t_p \leq 10 \mu \text{s}; T_{mb} = 25 ^\circ \text{C}; \text{Fig. 3}$ | - | 1020 | A

$T_{stg}$ | storage temperature |  | -55 | 175 | °C

$T_j$ | junction temperature |  | -55 | 175 | °C

$T_{sld(M)}$ | peak soldering temperature |  | - | 260 | °C

| Symbol | Parameter | Conditions | Min | Max | Unit |
--- | --- | --- | --- | --- | --- |
$V_{GS}$ | source current | $T_{mb} = 25 ^\circ \text{C}$ | - | 255 | A

$V_{GS}$ | peak source current | pulsed; $t_p \leq 10 \mu \text{s}; T_{mb} = 25 ^\circ \text{C}$ | - | 1020 | A

**Avalanche ruggedness**

$E_{DS(AL)}$ | non-repetitive drain-source avalanche energy | $I_D = 82 \text{ A}; V_{sup} \leq 100 \text{ V}; R_{GS} = 50 \text{ Ω}; V_{GS} = 10 \text{ V}; T_{j(init)} = 25 ^\circ \text{C};$ unclamped; $t_p = 137 \mu \text{s}; \text{Fig. 4}$ | [1] | - | 732 | mJ

$E_{DS(AL)S}$ | non-repetitive avalanche energy | $V_{sup} \leq 100 \text{ V}; V_{GS} = 10 \text{ V}; T_{j(init)} = 25 ^\circ \text{C};$ | [1] | - | 82 | A

[1] Protected by 100% test

---

**Fig. 1.** Normalized total power dissipation as a function of mounting base temperature

\[
P_{der} = \frac{P_{tot}}{P_{tot(25^\circ \text{C})}} \times 100 \%
\]

---

**Fig. 2.** Continuous drain current as a function of mounting base temperature

$V_{GS} \geq 10 \text{ V}$

(1) 255A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

---

**Figure 1.** Normalized total power dissipation as a function of mounting base temperature

**Figure 2.** Continuous drain current as a function of mounting base temperature
T_{mb} = 25 °C (solid black line); T_{mb} = 125 °C (red dashed line); I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

(1) T_j (init) = 25 °C; (2) T_j (init) = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{th(j-m-b)}</td>
<td>thermal resistance from junction to mounting base</td>
<td>Fig. 5</td>
<td>-</td>
<td>0.2</td>
<td>0.44</td>
<td>K/W</td>
</tr>
<tr>
<td>R_{th(j-a)}</td>
<td>thermal resistance from junction to ambient</td>
<td>Fig. 6</td>
<td>-</td>
<td>35</td>
<td>-</td>
<td>K/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>-</td>
<td>70</td>
<td>-</td>
<td>K/W</td>
</tr>
</tbody>
</table>
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

Fig. 6. PCB layout for resistance from junction to ambient
Copper square 25.4 mm x 25.4 mm; 70 μm thick on FR4 board

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient
70 μm thick copper on FR4 board

10. Characteristics

Table 7. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{(BR)DSS}</td>
<td>drain-source breakdown voltage</td>
<td>I_D = 250 μA; V_GS = 0 V; T_J = 25 °C</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_D = 250 μA; V_GS = 0 V; T_J = -55 °C</td>
<td>90</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>V_{GS(th)}</td>
<td>gate-source threshold voltage</td>
<td>I_D = 1 mA; V_DS=V_GS; T_J = 25 °C</td>
<td>2</td>
<td>2.6</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_D = 1 mA; V_DS=V_GS; T_J = -55 °C</td>
<td>-</td>
<td>3</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_D = 1 mA; V_DS=V_GS; T_J = 175 °C</td>
<td>-</td>
<td>1.6</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>ΔV_{GS(th)}/ΔT</td>
<td>gate-source threshold voltage variation with temperature</td>
<td>25 °C ≤ T_J ≤ 150 °C</td>
<td>-</td>
<td>-6.2</td>
<td>-</td>
<td>mV/K</td>
</tr>
<tr>
<td>I_{DSS}</td>
<td>drain leakage current</td>
<td>V_DS = 100 V; V_GS = 0 V; T_J = 25 °C</td>
<td>-</td>
<td>0.1</td>
<td>1</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_DS = 100 V; V_GS = 0 V; T_J = 125 °C</td>
<td>-</td>
<td>20</td>
<td>100</td>
<td>μA</td>
</tr>
<tr>
<td>I_{GSS}</td>
<td>gate leakage current</td>
<td>V_GS = 20 V; V_DS = 0 V; T_J = 25 °C</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V_GS = -20 V; V_DS = 0 V; T_J = 25 °C</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>Symbol</td>
<td>Parameter</td>
<td>Conditions</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>---------</td>
<td>----------------------------------</td>
<td>-----------------------------------------------------------------------------</td>
<td>------</td>
<td>------</td>
<td>------</td>
<td>------</td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>drain-source on-state resistance</td>
<td>$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ °C};$ [Fig. 11]</td>
<td>-</td>
<td>1.8</td>
<td>2.28</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ °C};$ [Fig. 12]</td>
<td>-</td>
<td>2.9</td>
<td>3.6</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ °C};$ [Fig. 12]</td>
<td>-</td>
<td>3.7</td>
<td>5.2</td>
<td>mΩ</td>
</tr>
<tr>
<td>$R_G$</td>
<td>gate resistance</td>
<td>$f = 1 \text{ MHz}; T_j = 25 \text{ °C}$</td>
<td>0.7</td>
<td>1.4</td>
<td>2.8</td>
<td>Ω</td>
</tr>
</tbody>
</table>

**Dynamic characteristics**

- **$Q_{G(tot)}$** total gate charge
  - $I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ [Fig. 13]
  - $I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ [Fig. 14]

- **$Q_{GS}$** gate-source charge
  - $I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V};$ [Fig. 14, Fig. 13]
  - Min: 32 nC, Typ: 54 nC, Max: 76 nC

- **$Q_{GS(th)}$** pre-threshold gate-source charge
  - Min: -34 nC, Typ: -34 nC, Max: -34 nC

- **$Q_{GS(th-pl)}$** post-threshold gate-source charge
  - Min: -20 nC, Typ: -20 nC, Max: -20 nC

- **$Q_{GD}$** gate-drain charge
  - Min: 8 nC, Typ: 27 nC, Max: 62 nC

- **$V_{GS(pl)}$** gate-source plateau voltage
  - $I_D = 25 \text{ A}; V_{DS} = 50 \text{ V};$ [Fig. 14, Fig. 13]
  - Min: -4.7 V, Typ: -4.7 V, Max: -4.7 V

- **$C_{iss}$** input capacitance
  - $V_{DS} = 50 \text{ V}; V_{GS} = 0 \text{ V}; f = 0.5 \text{ MHz}; T_j = 25 \text{ °C};$ [Fig. 16]
  - Min: 7380 pF, Typ: 12300 pF, Max: 17200 pF

- **$C_{oss}$** output capacitance
  - Min: 1600 pF, Typ: 2670 pF, Max: 4300 pF

- **$C_{rss}$** reverse transfer capacitance
  - Min: 4 pF, Typ: 36 pF, Max: 94 pF

- **$t_{d(on)}$** turn-on delay time
  - $V_{DS} = 50 \text{ V}; R_L = 2 \text{ Ω}; V_{GS} = 10 \text{ V}; R_{G(ext)} = 5 \text{ Ω}$
  - Min: -41 ns, Typ: -41 ns, Max: -41 ns

- **$t_r$** rise time
  - Min: -41 ns, Typ: -41 ns, Max: -41 ns

- **$t_{d(off)}$** turn-off delay time
  - Min: -88 ns, Typ: -88 ns, Max: -88 ns

- **$t_f$** fall time
  - Min: -54 ns, Typ: -54 ns, Max: -54 ns

**Source-drain diode**

- **$V_{SD}$** source-drain voltage
  - $I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ °C};$ [Fig. 17]
  - Min: -0.8 V, Typ: -1 V, Max: -1 V

- **$t_r$** reverse recovery time
  - $I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/µs}; V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V};$ [Fig. 18]
  - Min: -56 ns, Typ: -56 ns, Max: -56 ns

- **$Q_r$** recovered charge
  - Min: -68 nC, Typ: -68 nC, Max: -68 nC

[1] includes capacitive recovery
**Fig. 8.** Output characteristics; drain current as a function of drain-source voltage; typical values

\( T_j = 25 \, ^\circ\text{C} \)

**Fig. 9.** Drain-source on-state resistance as a function of gate-source voltage; typical values

\( T_j = 25 \, ^\circ\text{C}; \, I_D = 25 \, \text{A} \)

**Fig. 10.** Transfer characteristics; drain current as a function of gate-source voltage; typical values

\( V_{DS} = 8 \, \text{V} \)

**Fig. 11.** Drain-source on-state resistance as a function of drain current; typical values

\( T_j = 25 \, ^\circ\text{C} \)
Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

\[ a = \frac{R_{DSon}}{R_{DSon\ (25^°C)}} \]

Fig. 13. Gate charge waveform definitions

Fig. 14. Gate-source voltage as a function of gate charge; typical values

\[ V_{GS}(V) \]

\[ Q_G(nC) \]

\[ T_j = 25^°C; I_D = 25\ A \]

Fig. 15. Gate charge waveform definitions
V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}

**Fig. 16.** Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

V_{GS} = 0 \text{ V}

**Fig. 17.** Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

**Fig. 18.** Reverse recovery timing definition
11. Package outline

Plastic single-ended surface-mounted package (LFPAK88); 4 leads

Dimensions (mm are the original dimensions)

<table>
<thead>
<tr>
<th>Unit</th>
<th>A₁</th>
<th>A₂</th>
<th>A₃</th>
<th>b₁</th>
<th>b₂</th>
<th>c</th>
<th>c₀</th>
<th>D⁽¹⁾</th>
<th>D₁⁽¹⁾</th>
<th>E₁⁽¹⁾</th>
<th>E₂⁽¹⁾</th>
<th>e</th>
<th>H⁽¹⁾</th>
<th>L</th>
<th>L₂</th>
<th>w</th>
<th>y</th>
<th>θ</th>
</tr>
</thead>
<tbody>
<tr>
<td>max</td>
<td>0.15</td>
<td>1.7</td>
<td>1.1</td>
<td>7.3</td>
<td>0.24</td>
<td>0.55</td>
<td>6.3</td>
<td>5.1</td>
<td>8.1</td>
<td>6.9</td>
<td>8.1</td>
<td>0.8</td>
<td>1.3</td>
<td>0.25</td>
<td>0.10</td>
<td>8°</td>
<td></td>
<td></td>
</tr>
<tr>
<td>nom</td>
<td>0.00</td>
<td>1.5</td>
<td>0.9</td>
<td>7.1</td>
<td>0.18</td>
<td>0.45</td>
<td>6.1</td>
<td>4.9</td>
<td>7.9</td>
<td>6.7</td>
<td>7.8</td>
<td>0.6</td>
<td>0.9</td>
<td>0°</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>min</td>
<td>0.00</td>
<td>1.5</td>
<td>0.9</td>
<td>7.1</td>
<td>0.18</td>
<td>0.45</td>
<td>6.1</td>
<td>4.9</td>
<td>7.9</td>
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<td>0.9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note:
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

Fig. 19. Package outline LFPAK88 (SOT1235)
12. Soldering

Footprint information for reflow soldering of LFPAK88 package

SOT1235

occupied area
solder resist
solder land
solder paste

Dimensions in mm

recommended stencil thickness: 0.125 mm

Fig. 20. Reflow soldering footprint for LFPAK88 (SOT1235)
13. Legal information

Data sheet status

<table>
<thead>
<tr>
<th>Document status</th>
<th>Product status</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1][2]</td>
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</tr>
</tbody>
</table>

Objective [short] data sheet Development This document contains data from the respective specification for product development.

Preliminary [short] data sheet Qualification This document contains data from the preliminary specification.

Product [short] data sheet Production This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term "short data sheet" is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com

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