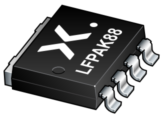

PSMN2R3-100SSE

N-channel 100 V, 2.3 mΩ, SuperSOA MOSFET in LFPAK88

29 October 2020 Objective data sheet

1. General description

SuperSOA N-channel enhancement mode MOSFET in a LFPAK88 package qualified to 175 °C.

Part of Nexperia's "NextPower Live" portfolio, the PSMN2R3-100SSE delivers very low R_{DSon} and a very strong linear-mode (SOA) performance in a high-reliability copper-clip LFPAK88 package.

PSMN2R3-100SSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn on, low R_{DSon} to minimize I^2R losses and deliver optimum efficiency when turned fully ON .

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low R_{DSon} for low I^2R conduction losses
- LFPAK88 package for applications that demand the highest performance and reliability

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	100	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	-	262	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	341	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	1.7	2.2	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C		-	2.7	3.4	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 5		[tbd]	26	[tbd]	nC
$Q_{G(tot)}$	total gate charge			[tbd]	160	[tbd]	nC
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; Fig. 6	[1]	-	32	-	nC

[1] includes capacitive recovery

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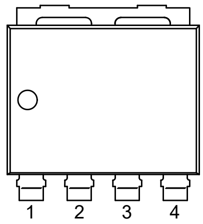
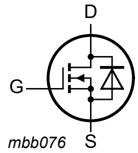
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 LFPAK88 (SOT1235)	
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN2R3-100SSE	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN2R3-100SSE	X2E3S10S

8. Limiting values

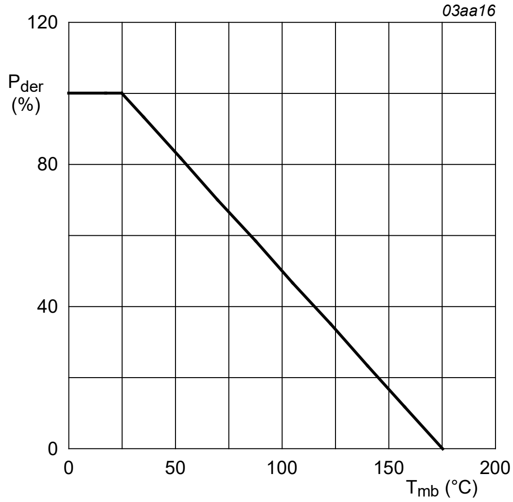
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	100	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	100	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	341	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	262	A
		V_{GS} = 10 V; T_{mb} = 100 °C		-	185	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 2		-	1047	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	262	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1047	A

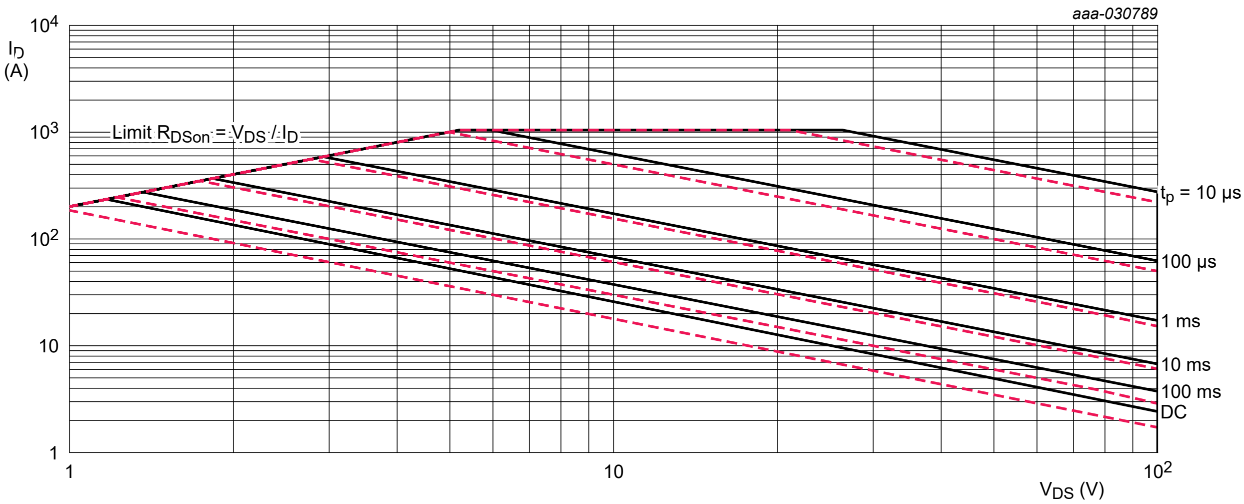
Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 82 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[1]	-	732	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} ≤ 100 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω	[1]	-	82	A

[1] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature



T_{mb} = 25 °C (solid black line);T_{mb} = 125 °C (red dashed line); I_{DM} is a single pulse

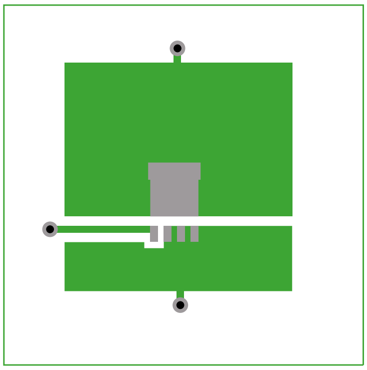
Fig. 2. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	[tbd]	0.44	K/W

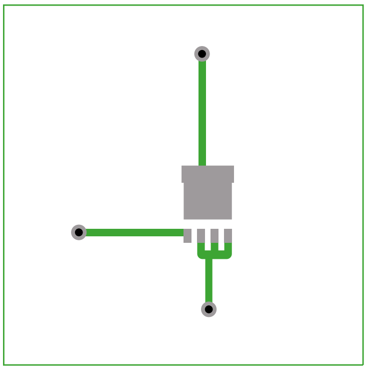
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 3		-	35	-	K/W
		Fig. 4		-	70	-	K/W



aaa-029383

Copper square 25.4 mm x 25.4 mm; 70 µm thick on FR4 board

Fig. 3. PCB layout for resistance from junction to ambient



aaa-029384

70 µm thick copper on FR4 board

Fig. 4. PCB layout with minimum footprint for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		2	3	4	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	[tbd]	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		-	[tbd]	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	[tbd]	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.1	25	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 125 °C		-	-	100	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		-	1.7	2.2	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C		-	2.7	3.4	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C		-	4	5	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		[tbd]	1	[tbd]	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 5		[tbd]	160	[tbd]	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V		-	83	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 50 V; V_{GS} = 10 V; Fig. 5		[tbd]	54	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	34	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	20	-	nC
Q_{GD}	gate-drain charge			[tbd]	26	[tbd]	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 50 V; Fig. 5		-	4.7	-	V
C_{iss}	input capacitance	V_{DS} = 50 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		[tbd]	12919	[tbd]	pF
C_{oss}	output capacitance			[tbd]	3356	[tbd]	pF
C_{rss}	reverse transfer capacitance			[tbd]	47	[tbd]	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 50 V; R_L = 2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω		-	43	-	ns
t_r	rise time			-	46	-	ns
$t_{d(off)}$	turn-off delay time			-	90	-	ns
t_f	fall time			-	57	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	0.8	1.2	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 50 V; Fig. 6		-	40	-	ns
Q_r	recovered charge		[1]	-	32	-	nC

[1] includes capacitive recovery

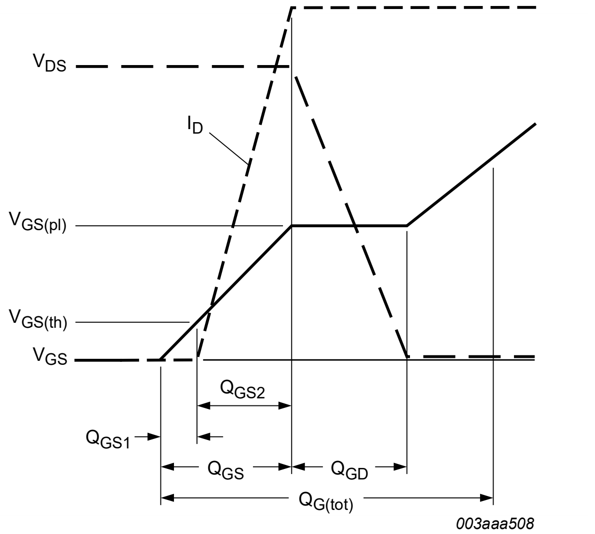


Fig. 5. Gate charge waveform definitions

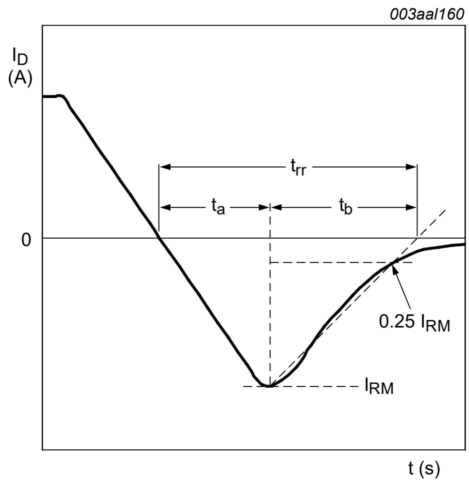
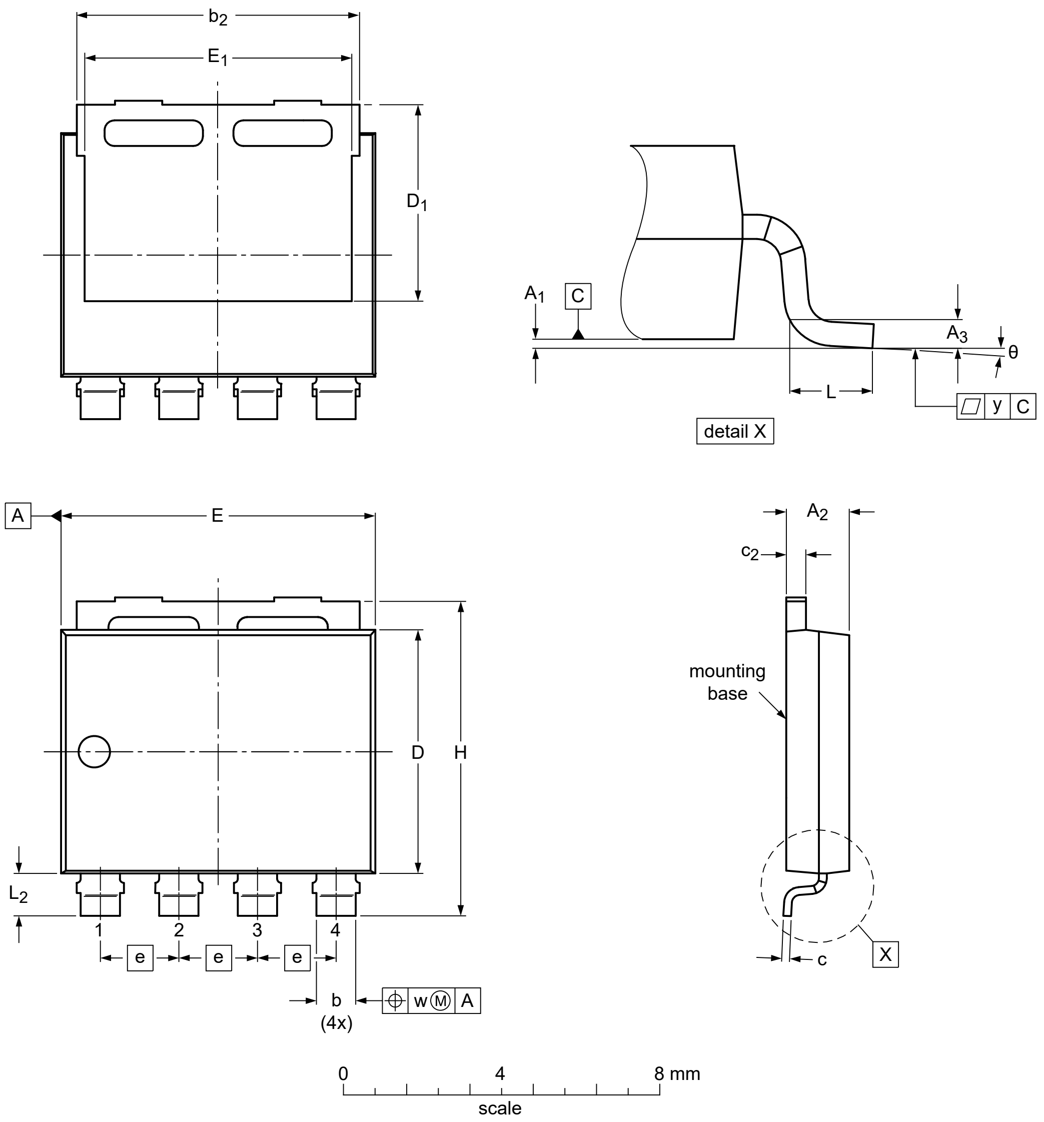


Fig. 6. Reverse recovery timing definition

11. Package outline

Plastic single-ended surface-mounted package (LFPAK88); 4 leads **SOT1235**



Dimensions (mm are the original dimensions)

Unit		A_1	A_2	A_3	b	b_2	c	c_2	D(1)	D_1(1)	E(1)	E_1(1)	e	H(1)	L	L_2	w	y	θ
mm	max	0.15	1.7		1.1	7.3	0.24	0.55	6.3	5.1	8.1	6.9		8.1	0.8	1.3			8°
	nom			0.25									2.0				0.25	0.10	
	min	0.00	1.5		0.9	7.1	0.18	0.45	6.1	4.9	7.9	6.7		7.8	0.6	0.9			0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

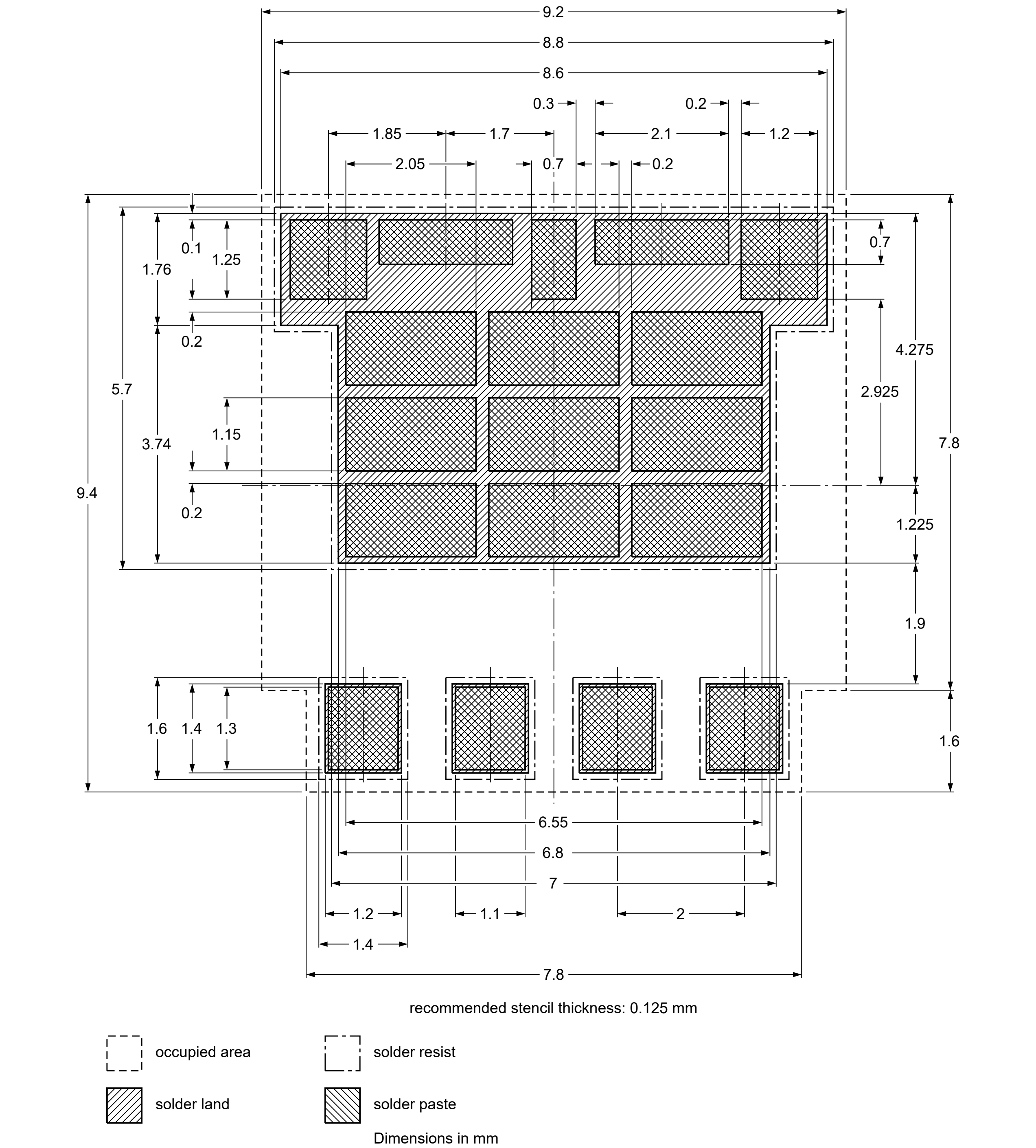
sot1235_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1235						~~17-08-02~~ 17-08-07

Fig. 7. Package outline LFPAK88 (SOT1235)

12. Soldering

Footprint information for reflow soldering of LFPAK88 package **SOT1235**



Issue date ~~18-12-12~~ 18-12-13

sot1235_fr

Fig. 8. Reflow soldering footprint for LFPAK88 (SOT1235)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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