



PSMN1R9-80SSJ

N-channel 80 V, 1.9 mOhm ASFET with enhanced dynamic current sharing in LFPAK88

24 October 2024

Objective data sheet

1. General description

In high-power applications, it is common practice to connect two or more MOSFETs in parallel to provide high current capability. Even when the gates are driven from the same gate driver, it can be challenging to ensure that MOSFETs share the load current equally.

Small differences in $V_{GS(th)}$ for individual devices cause the MOSFET with the lowest $V_{GS(th)}$ to turn on first, taking a larger share of the load current during the dynamic switching phase.

The difference in load current between individual MOSFETs ΔI_D can be significant often leading to differential heating and potential accelerated failure.

One method to reduce the ΔI between MOSFETs is to select devices with matched $V_{GS(th)}$, but testing & sorting MOSFETs with matched $V_{GS(th)}$ can be a difficult process. $V_{GS(th)}$ is typically measured at $I_D < 1$ mA and is influenced by temperature also.

ASFETs with enhanced dynamic current sharing are designed to show significantly improved current sharing with low ΔI_D when connected in parallel applications, they also deliver improved temperature stability showing lower ΔI_D due to temperature differences across the PCB.

2. Features and benefits

- Removes the need for $V_{GS(th)}$ matching
- Low ΔI_D enhances current sharing in parallel applications
- Less sensitive to temperature differences across the PCB
- Reduced $V_{GS(th)}$ spread
- Low R_{DSon}
- 286 A continuous I_D Max
- Avalanche rated, 100% tested
- Compact and Reliable 8x8 LFPAK88 package, qualified to 175 °C

3. Applications

- Applications using MOSFETs in parallel
- Applications utilizing MOSFETs with matched $V_{GS(th)}$
- High-power motor control

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ Fig. 2	-	-	286	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 1	-	-	340	W
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	1.6	1.9	mΩ

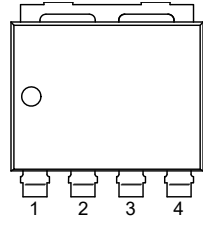
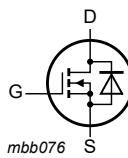
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}$; $V_{DS} = 40\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$	4	14	33	nC
Source-drain diode						
Q_r	recovered charge	$I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; [1] $V_{DS} = 40\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	107	-	nC

[1] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LFPAK88 (SOT1235)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R9-80SSJ	LFPAK88	plastic, single-ended surface-mounted package (LFPAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

7. Limiting values

Table 4. Limiting values

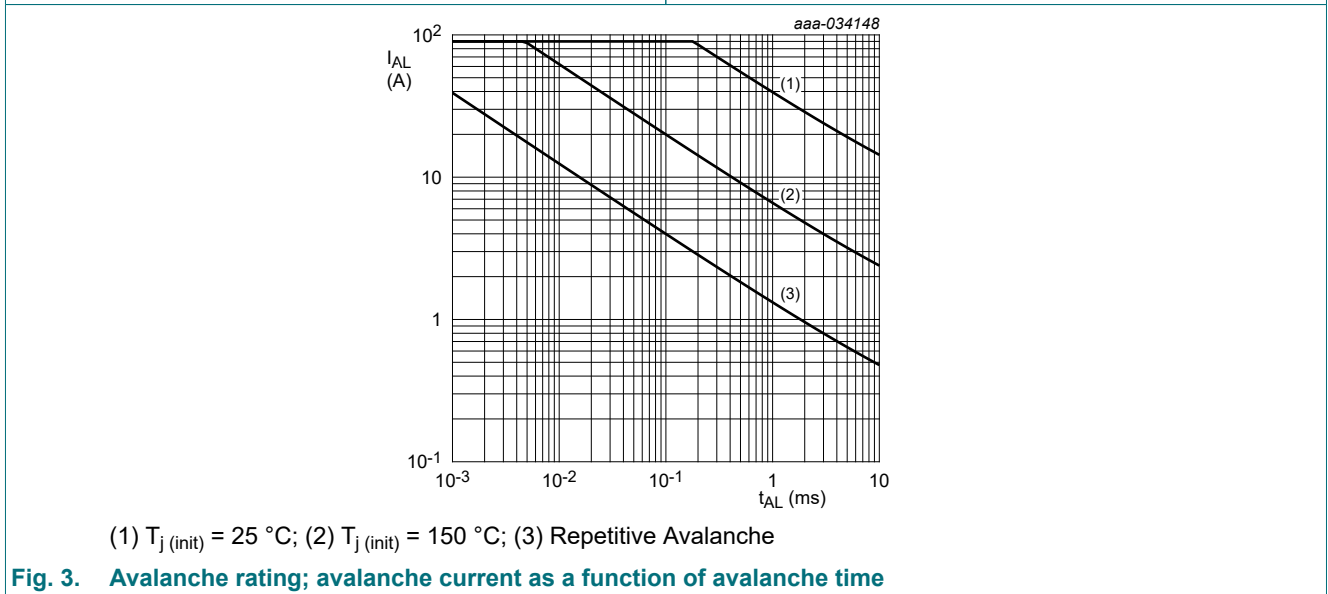
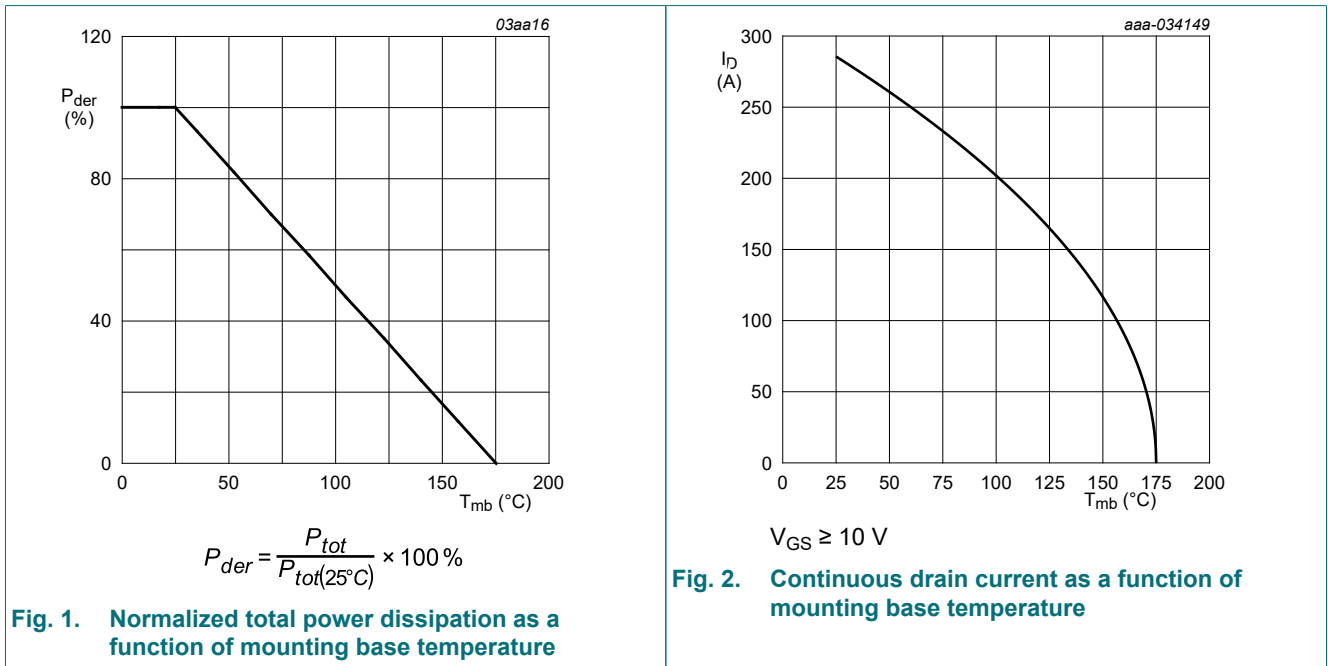
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	80	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	80	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	340	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	286	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	202	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	1142	A
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
$T_{sld(M)}$	peak soldering temperature		-	260	°C

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Symbol	Parameter	Conditions	Min	Max	Unit
Source-drain diode					
I_S	source current	$T_{mb} = 25\text{ °C}$	-	286	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$	-	1142	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 90\text{ A}$; $V_{sup} \leq 80\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; unclamped; $t_p = 179\text{ }\mu\text{s}$; Fig. 3	[1]	840	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} \leq 80\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(init)} = 25\text{ °C}$; $R_{GS} = 50\text{ }\Omega$; Fig. 3	[1]	90	A

[1] Protected by 100% test



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.2	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5	-	35	-	K/W
		Fig. 6	-	70	-	K/W

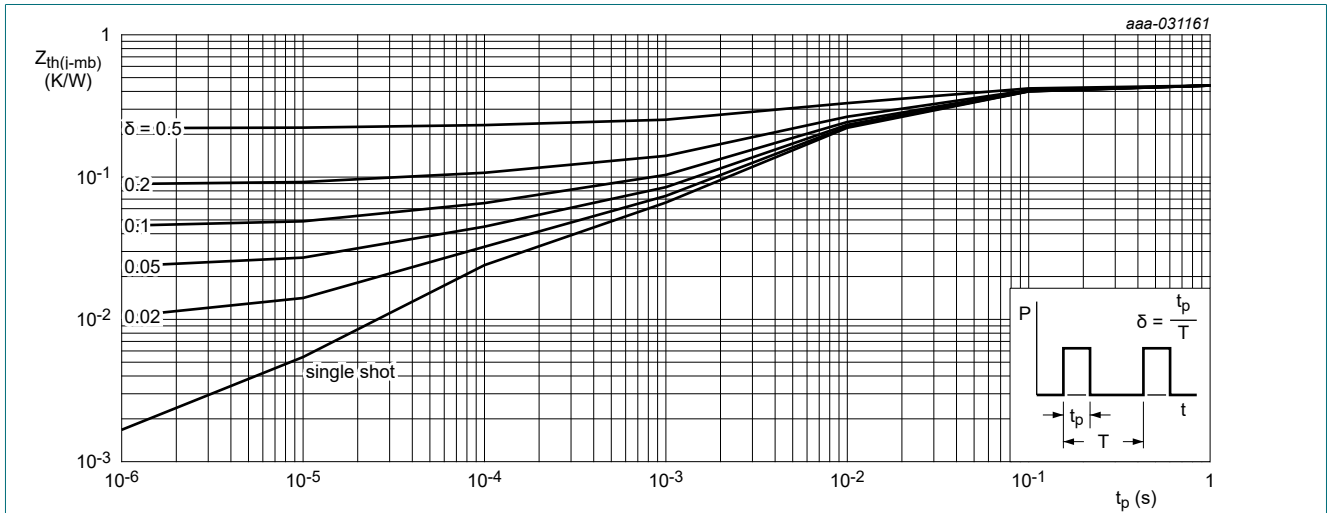


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

Copper square 25.4 mm x 25.4 mm; 70 μ m thick on FR4 board

70 μ m thick copper on FR4 board

Fig. 5. PCB layout for resistance from junction to ambient

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient

9. Characteristics

Table 6. Characteristics

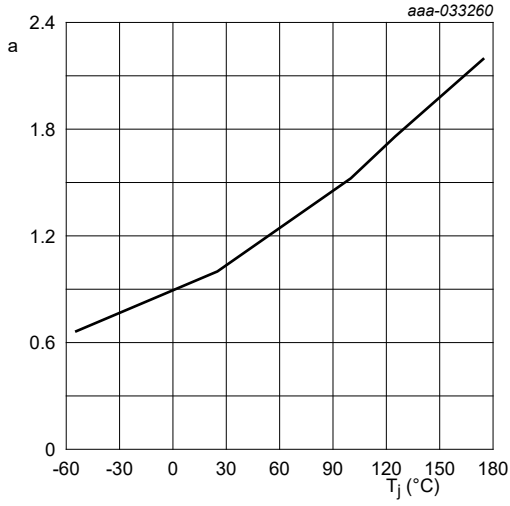
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	-	-	V

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	1	1.8	3	V
		$I_D = 100 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	-	2.2	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ\text{C}$	-	2.1	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ\text{C}$	-	1.1	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ\text{C} \leq T_j \leq 150 \text{ }^\circ\text{C}$	-	-4.5	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.02	1	μA
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ\text{C}$	-	66	200	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	1.6	1.9	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ\text{C};$ Fig. 7	-	2.6	3	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ Fig. 7	-	-	4.2	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C}$	0.8	1.6	3.2	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C}$	127	253	380	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C}$	-	[tbd]	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 \text{ }^\circ\text{C}$	54	90	126	nC
Q_{GD}	gate-drain charge	$T_j = 25 \text{ }^\circ\text{C}$	4	14	33	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25 \text{ A}; V_{DS} = 40 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	4	-	V
C_{iss}	input capacitance	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; f = 0.5 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C}$	12780	21300	29810	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ\text{C}$	1710	2843	4560	pF
C_{rss}	reverse transfer capacitance		7	64	195	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 1.6 \text{ }^\circ\Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 5 \text{ }^\circ\Omega; T_j = 25 \text{ }^\circ\text{C}$	-	59	-	ns
t_r	rise time		-	57	-	ns
$t_{d(off)}$	turn-off delay time		-	162	-	ns
t_f	fall time		-	71	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 8	-	0.78	1	V
t_{rr}	reverse recovery time	$I_S = 25 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V};$	-	65	-	ns
Q_r	recovered charge	$V_{DS} = 40 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ Fig. 9	[1]	107	-	nC

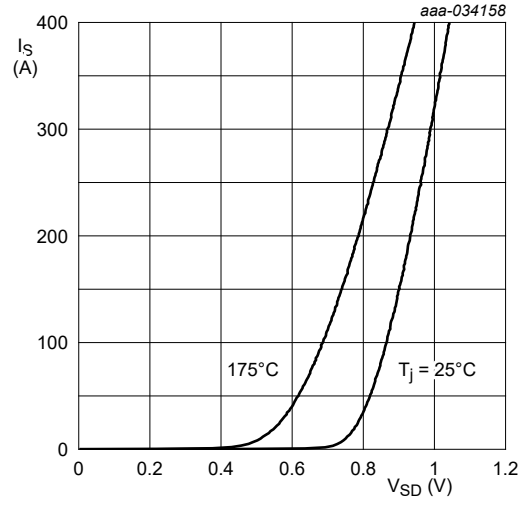
[1] includes capacitive recovery

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$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

Fig. 7. Normalized drain-source on-state resistance factor as a function of junction temperature



$V_{GS} = 0\text{ V}$

Fig. 8. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

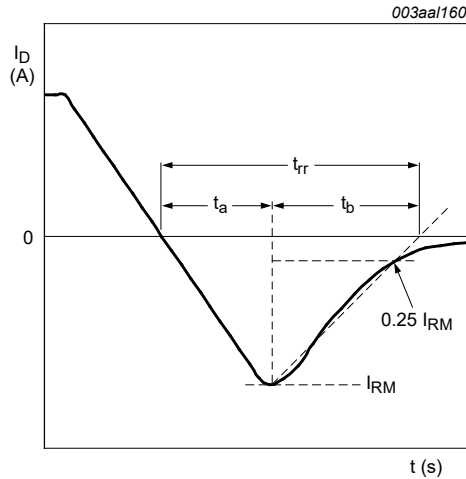


Fig. 9. Reverse recovery timing definition

10. Package outline

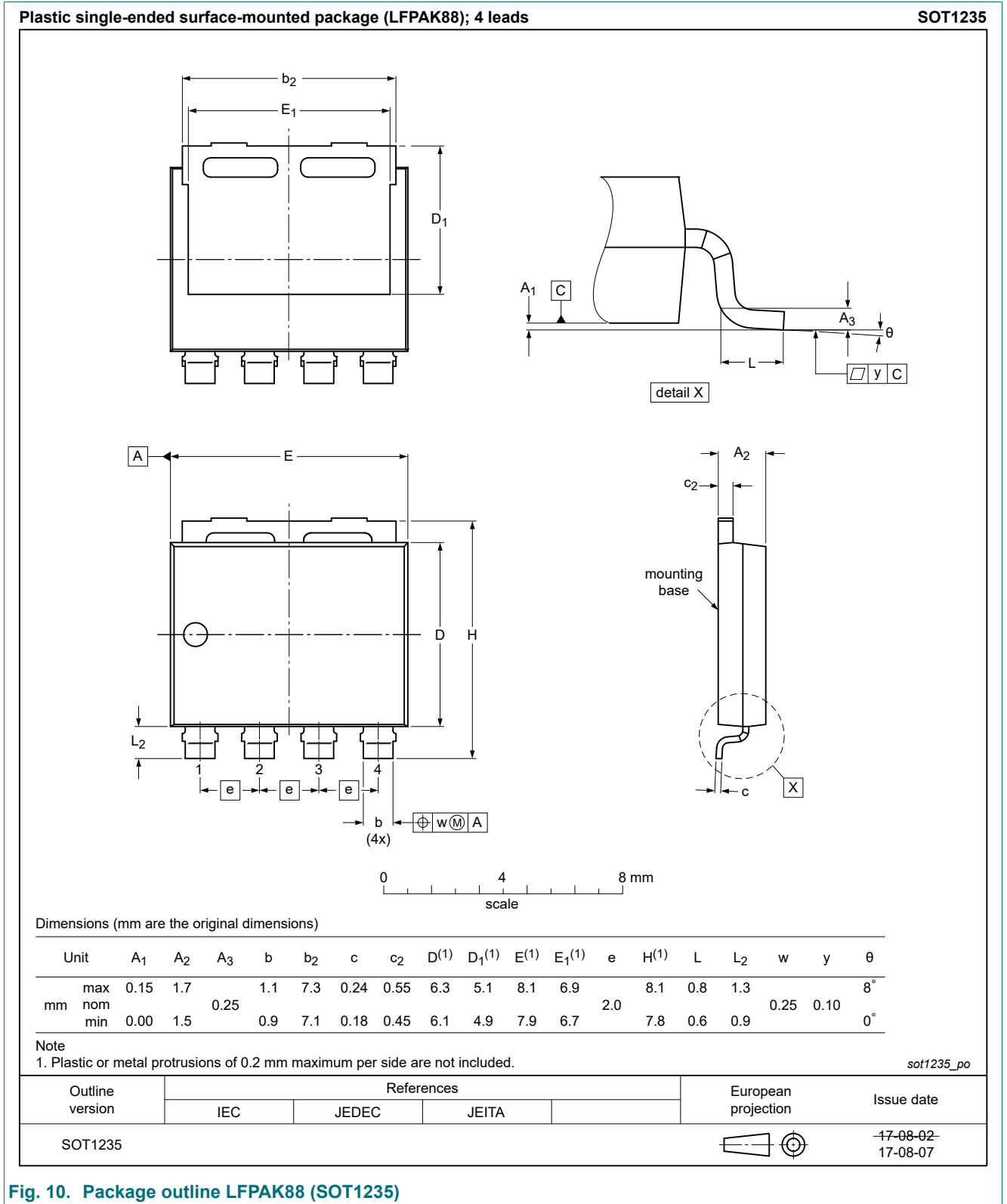


Fig. 10. Package outline LPAK88 (SOT1235)

11. Soldering

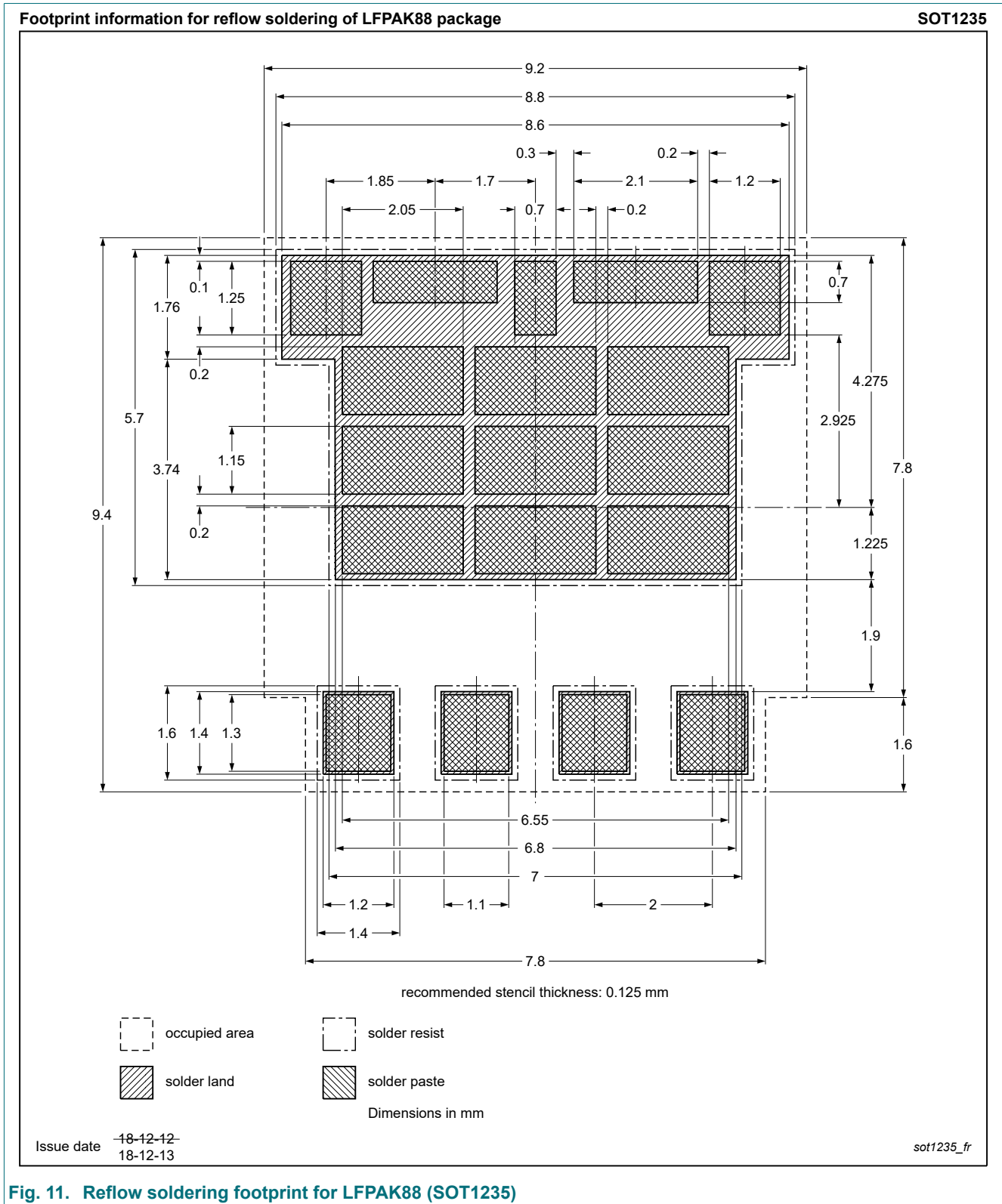


Fig. 11. Reflow soldering footprint for LPAK88 (SOT1235)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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