1. General description

200 A, logic level gate drive N-channel enhancement mode MOSFET in 175 °C LFPAK56 package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- 200 A continuous $I_{D\text{\,(max)}}$ rating
- Avalanche rated, 100% tested at $I_{AS} = 180$ A
- Strong SOA (linear-mode) rating
- NextPower-S3 technology delivers 'superfast switching with soft body-diode recovery'
- Low $Q_{RR}$, $Q_{G}$ and $Q_{GD}$ for high system efficiency and low EMI designs
- Schottky-Plus body-diode with low $V_{SD}$, low $Q_{RR}$, soft recovery and low $I_{DSS}$ leakage
- Optimised for 4.5 V gate drive utilising NextPower-S3 Superjunction technology
- High reliability LFPAK (Power SO8) package, with copper-clip and solder die attach, qualified to 175 °C
- Exposed leads can be wave soldered, visual solder joint inspection and high quality solder joints
- Low parasitic inductance and resistance

3. Applications

- High-performance synchronous rectification
- DC-to-DC converters
- High performance and high efficiency server power supply
- Brushless DC motor control
- Battery protection
- Load-switch and eFuse
- Inrush management, hotswap

4. Quick reference data

| Table 1. Quick reference data | Conditions | Min | Typ | Max | Unit |
| Symbol | Parameter | | | | |
| $V_{DS}$ | drain-source voltage | $25 \ ^\circ C \leq T_{j} \leq 175 \ ^\circ C$ | - | - | 40 | V |
| $I_{D}$ | drain current | $V_{GS} = 10$ V; $T_{mb} = 25$ °C; Fig. 2 | - | - | 200 | A |
| $P_{tot}$ | total power dissipation | $T_{mb} = 25$ °C; Fig. 1 | - | - | 194 | W |
| $T_{j}$ | junction temperature | -55 | - | 175 | °C |

Static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
| $R_{DS\text{\,on}}$ | drain-source on-state resistance | $V_{GS} = 10$ V; $I_{D} = 25$ A; $T_{j} = 25$ °C; Fig. 10 | - | 1.5 | 1.8 | mΩ |
| | | $V_{GS} = 4.5$ V; $I_{D} = 25$ A; $T_{j} = 25$ °C; Fig. 10 | - | 1.9 | 2.3 | mΩ |
Nexperia

PSMN1R7-40YLD

N-channel 40 V, 1.8 mΩ, 200 A logic level MOSFET in LFPAK56 using NexPower-S3 Schottky-Plus technology

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Q_{GD}$</td>
<td>gate-drain charge</td>
<td>$I_D = 25 \text{ A}; V_{DS} = 20 \text{ V}; V_{GS} = 4.5 \text{ V}; \text{Fig. 12; Fig. 13}$</td>
<td>2.3</td>
<td>7.7</td>
<td>15</td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{G(tot)}$</td>
<td>total gate charge</td>
<td></td>
<td>23</td>
<td>35</td>
<td>49</td>
<td>nC</td>
</tr>
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[1] 200A Continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

5. Pinning information

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
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<td>1</td>
<td>S</td>
<td>source</td>
<td>mb D</td>
<td>mb D</td>
</tr>
<tr>
<td>2</td>
<td>S</td>
<td>source</td>
<td>mb D</td>
<td>mb D</td>
</tr>
<tr>
<td>3</td>
<td>S</td>
<td>source</td>
<td>mb D</td>
<td>mb D</td>
</tr>
<tr>
<td>4</td>
<td>G</td>
<td>gate</td>
<td>mb D</td>
<td>mb D</td>
</tr>
<tr>
<td>mb</td>
<td>D</td>
<td>mounting base; connected to drain</td>
<td>mb D</td>
<td>mb D</td>
</tr>
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</table>

6. Ordering information

Table 3. Ordering information

<table>
<thead>
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<th>Type number</th>
<th>Package Name</th>
<th>Description</th>
<th>Version</th>
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</thead>
<tbody>
<tr>
<td>PSMN1R7-40YLD</td>
<td>LFPAK56; Power-SO8</td>
<td>plastic, single-ended surface-mounted package; 4 terminals</td>
<td>SOT669</td>
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7. Marking

Table 4. Marking codes

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<th>Marking code</th>
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<td>PSMN1R7-40YLD</td>
<td>1D7L40Y</td>
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</table>

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>drain-source voltage</td>
<td>$25 ^\circ C \leq T_j \leq 175 ^\circ C$</td>
<td>-</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DSM}$</td>
<td>peak drain-source voltage</td>
<td>$t_p \leq 20 \text{ ns}; f \leq 500 \text{ kHz}; E_{DS(AL)} \leq 200 \text{ nJ};$ pulsed</td>
<td>-</td>
<td>45</td>
<td>V</td>
</tr>
<tr>
<td>$V_{DGR}$</td>
<td>drain-gate voltage</td>
<td>$25 ^\circ C \leq T_j \leq 175 ^\circ C; R_{GS} = 20 \text{ k}\Omega$</td>
<td>-</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>gate-source voltage</td>
<td></td>
<td>-20</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{mb} = 25 ^\circ C; \text{Fig. 1}$</td>
<td>-</td>
<td>194</td>
<td>W</td>
</tr>
<tr>
<td>$I_D$</td>
<td>drain current</td>
<td>$V_{GS} = 10 \text{ V}; T_{mb} = 25 ^\circ C; \text{Fig. 2}$</td>
<td>[1]</td>
<td>-</td>
<td>200</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 10 \text{ V}; T_{mb} = 100 ^\circ C; \text{Fig. 2}$</td>
<td></td>
<td>-</td>
<td>167</td>
</tr>
<tr>
<td>$I_{DM}$</td>
<td>peak drain current pulsed; $t_p \leq 10 \mu s; T_{mb} = 25 ^\circ C; \text{Fig. 3}$</td>
<td></td>
<td>-</td>
<td>944</td>
<td>A</td>
</tr>
</tbody>
</table>
**N-channel 40 V, 1.8 mΩ, 200 A logic level MOSFET in LFPAK56 using NextPower-S3 Schottky-Plus technology**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$T_{stg}$</td>
<td>storage temperature</td>
<td>-55</td>
<td>175</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_j$</td>
<td>junction temperature</td>
<td>-55</td>
<td>175</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>$T_{sld(M)}$</td>
<td>peak soldering temperature</td>
<td>-</td>
<td>260</td>
<td>°C</td>
<td></td>
</tr>
</tbody>
</table>

### Source-drain diode

- $I_S$: source current, $T_{mb} = 25$ °C
  - Min: -194 A
- $I_{SM}$: peak source current, pulsed; $t_p \leq 10$ µs; $T_{mb} = 25$ °C
  - Min: -944 A

### Avalanche ruggedness

- $E_{DS(AlS)}$: non-repetitive drain-source avalanche energy
  - $I_D = 60.8$ A; $V_{sup} \leq 40$ V; $R_{GS} = 50$ Ω; $V_{DS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped; $t_p = 202$ µs
    - Min: -319 mJ
  - $I_D = 25$ A; $V_{sup} \leq 40$ V; $R_{GS} = 50$ Ω; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; unclamped; $t_p = 1.4$ ms
    - Min: -905 mJ
- $I_{AS}$: non-repetitive avalanche current
  - $V_{sup} = 40$ V; $V_{GS} = 10$ V; $T_{j(init)} = 25$ °C; $R_{GS} = 50$ Ω
    - Min: -180 A

[1] 200A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

[2] Protected by 100% test

---

**Fig. 1.** Normalized total power dissipation as a function of mounting base temperature

\[
P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\%
\]

**Fig. 2.** Continuous drain current as a function of mounting base temperature

$V_{GS} \geq 10$ V

(1) 200A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
N-channel 40 V, 1.8 mΩ, 200 A logic level MOSFET in LFPAK56 using NextPower-S3 Schottky-Plus technology

T_{mb} = 25 °C; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_{th(j-mb)}</td>
<td>thermal resistance from junction to mounting base</td>
<td>Fig. 4</td>
<td>-</td>
<td>0.69</td>
<td>0.77</td>
<td>K/W</td>
</tr>
<tr>
<td>R_{th(j-a)}</td>
<td>thermal resistance from junction to ambient</td>
<td>Fig. 5</td>
<td>-</td>
<td>42</td>
<td>-</td>
<td>K/W</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fig. 6</td>
<td>-</td>
<td>85</td>
<td>-</td>
<td>K/W</td>
</tr>
</tbody>
</table>

Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration
10. Characteristics

Table 7. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td><strong>Static characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{(BR)DSS}$</td>
<td>drain-source breakdown voltage</td>
<td>$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 ^\circ C$</td>
<td>40</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 ^\circ C$</td>
<td>36</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS(th)}$</td>
<td>gate-source threshold voltage</td>
<td>$I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 ^\circ C$</td>
<td>1.35</td>
<td>1.7</td>
<td>2.05</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{GS(th)}/\Delta T$</td>
<td>gate-source threshold voltage variation with temperature</td>
<td>$25 ^\circ C \leq T_j \leq 150 ^\circ C$</td>
<td>-</td>
<td>-4.6</td>
<td>-</td>
<td>mV/K</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>drain leakage current</td>
<td>$V_{DS} = 32 V; V_{GS} = 0 V; T_j = 25 ^\circ C$</td>
<td>-</td>
<td>0.006</td>
<td>1</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{DS} = 32 V; V_{GS} = 0 V; T_j = 125 ^\circ C$</td>
<td>-</td>
<td>2.1</td>
<td>-</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{GSS}$</td>
<td>gate leakage current</td>
<td>$V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 ^\circ C$</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 ^\circ C$</td>
<td>-</td>
<td>2</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>drain-source on-state resistance</td>
<td>$V_{GS} = 10 V; I_D = 25 A; T_j = 25 ^\circ C$; $V_{GS} = 10 V; T_j = 175 ^\circ C$</td>
<td>-</td>
<td>1.5</td>
<td>1.8</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 ^\circ C$; $V_{GS} = 4.5 V; T_j = 175 ^\circ C$</td>
<td>-</td>
<td>-</td>
<td>3.5</td>
<td>mΩ</td>
</tr>
<tr>
<td>$R_G$</td>
<td>gate resistance</td>
<td>$f = 1 MHz; T_j = 25 ^\circ C$</td>
<td>0.4</td>
<td>1</td>
<td>2.5</td>
<td>Ω</td>
</tr>
<tr>
<td></td>
<td><strong>Dynamic characteristics</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$Q_G(tot)$</td>
<td>total gate charge</td>
<td>$I_D = 25 A; V_{DS} = 20 V; V_{GS} = 4.5 V$; $I_D = 25 A; V_{DS} = 20 V; V_{GS} = 10 V$</td>
<td>23</td>
<td>35</td>
<td>49</td>
<td>nC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$</td>
<td>51</td>
<td>78</td>
<td>109</td>
<td>nC</td>
</tr>
</tbody>
</table>

Copper area 25.4 mm square; 70 µm thick on FR4 board

Fig. 5. PCB layout for thermal resistance from junction to ambient

70 µm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient
### Symbol | Parameter | Conditions | Min | Typ | Max | Unit
--- | --- | --- | --- | --- | --- | ---
$Q_{GS}$ | gate-source charge | $I_D = 25 \, A; \; V_{DS} = 20 \, V; \; V_{GS} = 4.5 \, V$; | 7.8 | 13 | 20 | nC
$Q_{GS(th)}$ | pre-threshold gate-source charge | | 4.8 | 8.1 | 12 | nC
$Q_{GS(th-pl)}$ | post-threshold gate-source charge | | 2.9 | 4.9 | 7.4 | nC
$Q_{GD}$ | gate-drain charge | | 2.3 | 7.7 | 15 | nC
$V_{GS(pl)}$ | gate-source plateau voltage | $I_D = 25 \, A; \; V_{DS} = 20 \, V$; | - | 2.7 | - | V
$C_{iss}$ | input capacitance | $V_{DS} = 20 \, V; \; V_{GS} = 0 \, V; \; f = 1 \, MHz$; $T_j = 25 \, ^\circ C$; | 3699 | 5690 | 7966 | pF
$C_{oss}$ | output capacitance | $T_j = 25 \, ^\circ C$; | 725 | 1115 | 1561 | pF
$C_{rss}$ | reverse transfer capacitance | | 57 | 190 | 418 | pF
$t_{d(on)}$ | turn-on delay time | $V_{DS} = 20 \, V; \; R_L = 0.8 \, \Omega; \; V_{GS} = 4.5 \, V; \; R_{G(\text{ext})} = 5 \, \Omega$ | - | 30 | - | ns
$t_r$ | rise time | | - | 30 | - | ns
$t_{d(off)}$ | turn-off delay time | | - | 36 | - | ns
$t_f$ | fall time | | - | 20 | - | ns
$Q_{oss}$ | output charge | $V_{GS} = 0 \, V; \; V_{DS} = 20 \, V; \; f = 1 \, MHz$; $T_j = 25 \, ^\circ C$; | - | 37 | - | nC

### Source-drain diode

$V_{SD}$ | source-drain voltage | $I_S = 25 \, A; \; V_{GS} = 0 \, V; \; T_j = 25 \, ^\circ C$; | - | 0.8 | 1 | V
$t_{rr}$ | reverse recovery time | $I_S = 25 \, A; \; dI_S/dt = -100 \, A/\mu s; \; V_{GS} = 0 \, V; \; V_{DS} = 20 \, V$; | - | 33 | - | ns
$Q_{r}$ | recovered charge | $V_{DS} = 20 \, V$; | [1] | 27 | - | nC
$t_a$ | reverse recovery rise time | | - | 18 | - | ns
$t_b$ | reverse recovery fall time | | - | 15 | - | ns

[1] includes capacitive recovery

---

**Fig. 7.** Output characteristics; drain current as a function of drain-source voltage; typical values

**Fig. 8.** Drain-source on-state resistance as a function of gate-source voltage; typical values

---

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N-channel 40 V, 1.8 mΩ, 200 A logic level MOSFET in LFPAK56 using NextPower-S3 Schottky-Plus technology

**Fig. 9.** Transfer characteristics; drain current as a function of gate-source voltage; typical values

**Fig. 10.** Drain-source on-state resistance as a function of drain current; typical values

**Fig. 11.** Normalized drain-source on-state resistance factor as a function of junction temperature

**Fig. 12.** Gate-source voltage as a function of gate charge; typical values
**N-channel 40 V, 1.8 mΩ, 200 A logic level MOSFET in LFPAK56 using NextPower-S3 Schottky-Plus technology**

**Fig. 13.** Gate charge waveform definitions

\[
V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}
\]

**Fig. 14.** Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

\[
V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}
\]

**Fig. 15.** Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

\[
V_{GS} = 0 \text{ V}
\]

**Fig. 16.** Reverse recovery timing definition
11. Package outline

Fig. 17. Package outline LFPAK56; Power-SO8 (SOT669)
12. Soldering

Footprint information for reflow soldering

![Footprint Diagram](sot69_fr)

- **SR opening = Cu × 0.075**
- **SP opening = Cu × 0.050**

Dimensions in mm:
- 0.6 (3x)
- 0.25 (2x)
- 3.45
- 3.5
- 2.55
- 2
- 2.16
- 3.3
- 1.27
- 0.7 (4x)
- 3.81

---

**Fig. 18. Reflow soldering footprint for LFPAK56; Power-SO8 (SOT69)**
Fig. 19. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)
13. Legal information

Data sheet status

<table>
<thead>
<tr>
<th>Document status</th>
<th>Product status</th>
<th>Definition</th>
</tr>
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<tbody>
<tr>
<td>Objective [short] data sheet</td>
<td>Development</td>
<td>This document contains data from the respective specification for product development.</td>
</tr>
<tr>
<td>Preliminary [short] data sheet</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
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<tr>
<td>Product [short] data sheet</td>
<td>Production</td>
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</table>

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term "short data sheet" is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com

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