PSMN1R5-60YSN

N-channel 60 V, 1.5 mOhm, standard level NextPowerS3 MOSFET in LFPAK56E

25 April 2024 **Objective data sheet**

1. General description

NextPowerS3 family leverages “superjunction” and Schottky-Plus technologies for super-fast switching with soft body-diode recovery, delivering low spiking without compromising efficiency or I_{DSS} leakage. This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- 250 A continuous $I_{D(max)}$
- Avalanche rated, 100% tested
- High reliability LFPAK (Power SO8) package, qualified to 175 °C
- LFPAK copper clip:
  - Improved thermal dissipation and even current distribution
  - Reduced electrical and thermal resistance
- LFPAK gull wing lead:
  - Enhanced wetting area for solder coverage and visual soldering inspection
  - High Board Level Reliability, absorbing thermal expansion and mechanical strain

3. Applications

- eFuse
- Battery protection
- Motor control
- Power supply for servers and telecoms
- DC-to-DC converters

4. Quick reference data

Table 1. Quick reference data

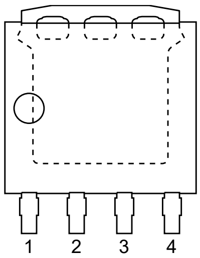
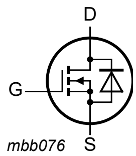
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	60	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	-	250	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	250	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		[tbd]	1.2	1.5	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 30 V; V_{GS} = 10 V; T_j = 25 °C		[tbd]	79	[tbd]	nC
$Q_{G(tot)}$	total gate charge			[tbd]	236	[tbd]	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{sup} ≤ 60 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[1]	-	-	[tbd]	mJ
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C; Fig. 2	[2]	-	[tbd]	-	nC

[1] Protected by 100% test.
[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56E; Power-SO8 (SOT1023)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R5-60YSN	LFPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LFPAK56E); 4 leads; 1.27 mm pitch	SOT1023

7. Limiting values

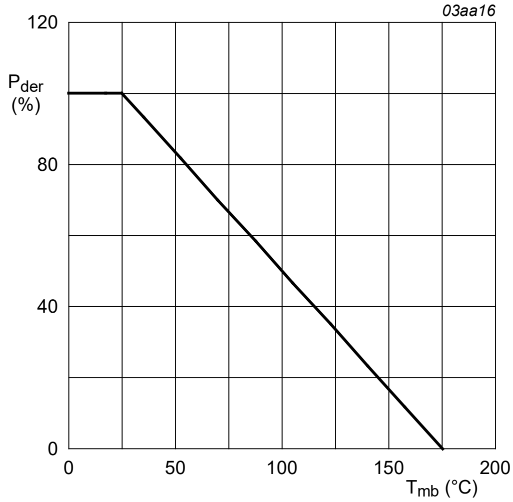
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	60	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	250	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C		-	250	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1152	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	250	A

Symbol	Parameter	Conditions		Min	Max	Unit
I_{SM}	peak source current	pulsed; t_p ≤ 10 μs; T_{mb} = 25 °C		-	1152	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	V_{sup} ≤ 60 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[1]	-	[tbd]	mJ
I_{AS}	non-repetitive avalanche current	$T_{j(init)}$ = 25 °C	[1]	-	[tbd]	A

[1] Protected by 100% test.



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	[tbd]	0.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient			-	[tbd]	-	K/W

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 μA; V_{GS} = 0 V; T_j = 25 °C		60	[tbd]	-	V
		I_D = 250 μA; V_{GS} = 0 V; T_j = -55 °C		-	[tbd]	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		2.4	3	3.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	[tbd]	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 175 °C		-	[tbd]	-	mV/K

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{DSS}	drain leakage current	V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 °C		-	[tbd]	1	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		[tbd]	1.2	1.5	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C		[tbd]	2.4	3.02	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		[tbd]	[tbd]	[tbd]	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 30 V; V_{GS} = 10 V; T_j = 25 °C		[tbd]	236	[tbd]	nC
		I_D = 0 A; V_{DS} = 0 V; T_j = 25 °C		-	[tbd]	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 30 V; V_{GS} = 10 V; T_j = 25 °C		[tbd]	33	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			[tbd]	[tbd]	[tbd]	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			[tbd]	[tbd]	[tbd]	nC
Q_{GD}	gate-drain charge			[tbd]	79	[tbd]	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 30 V; T_j = 25 °C		-	[tbd]	-	V
C_{iss}	input capacitance	V_{DS} = 30 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		[tbd]	[tbd]	[tbd]	pF
C_{oss}	output capacitance			[tbd]	[tbd]	[tbd]	pF
C_{rss}	reverse transfer capacitance			[tbd]	[tbd]	[tbd]	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	[tbd]	-	ns
t_r	rise time			-	[tbd]	-	ns
$t_{d(off)}$	turn-off delay time			-	[tbd]	-	ns
t_f	fall time			-	[tbd]	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	[tbd]	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C; Fig. 2		-	[tbd]	-	ns
Q_r	recovered charge		[1]	-	[tbd]	-	nC

[1] includes capacitive recovery

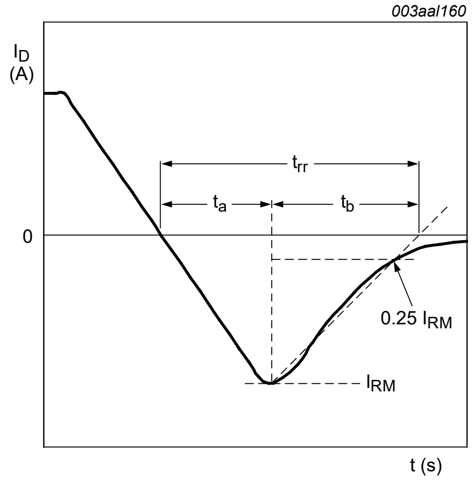
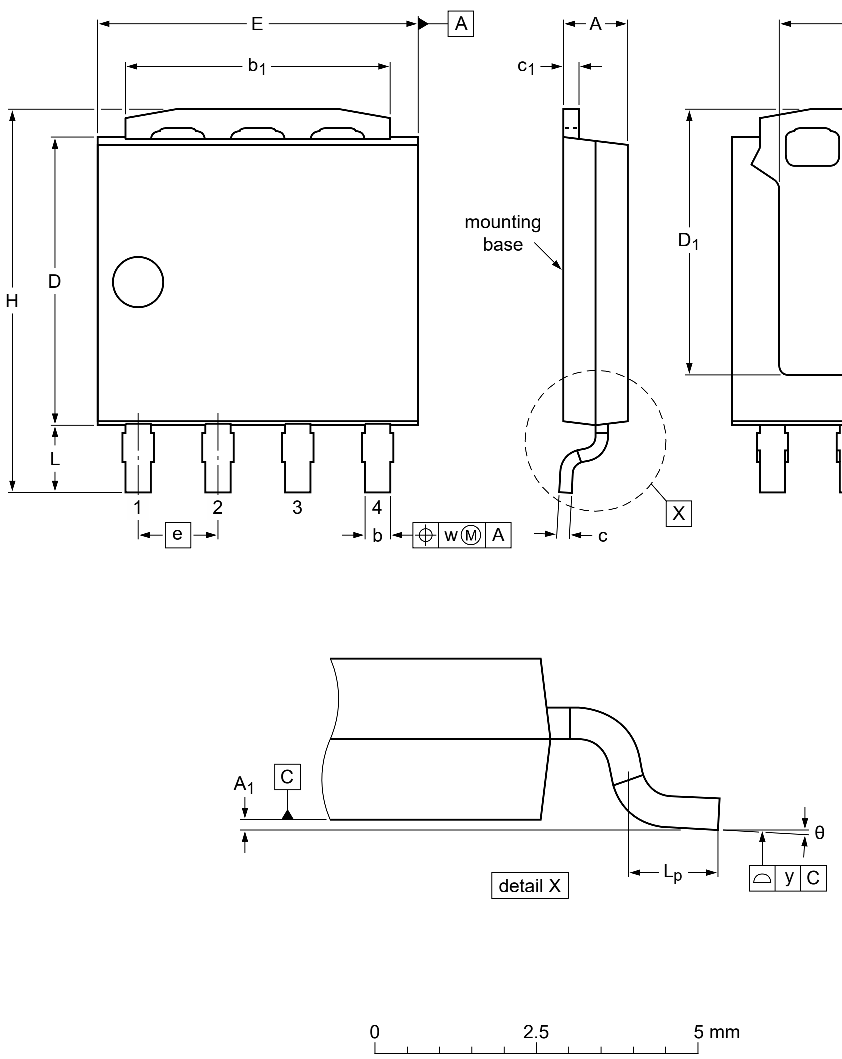


Fig. 2. Reverse recovery timing definition

10. Package outline

Plastic single-ended surface-mounted package (LFPAK56E); 4 leads **SOT1023**



Dimensions

Unit		A	A_1	b	b_1	b_2	c	c_1	$D^{(1)}$	$D_1^{(1)}$	$E^{(1)}$	$E_1^{(1)}$	e	H	L	L_p	w	y	θ
mm	max	1.10	0.15	0.50	4.41		0.25	0.30	4.70	4.45	5.30	3.7		6.2	1.3	0.85			8°
	nom					0.85							1.27				0.25	0.1	
	min	0.95	0.00	0.35	3.62		0.19	0.24	4.45		4.95	3.5		5.9	0.8	0.40			0°

Note

1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1023_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1023						~~13-03-05~~ 17-07-31

Fig. 3. Package outline LFPAK56E; Power-SO8 (SOT1023)

11. Soldering

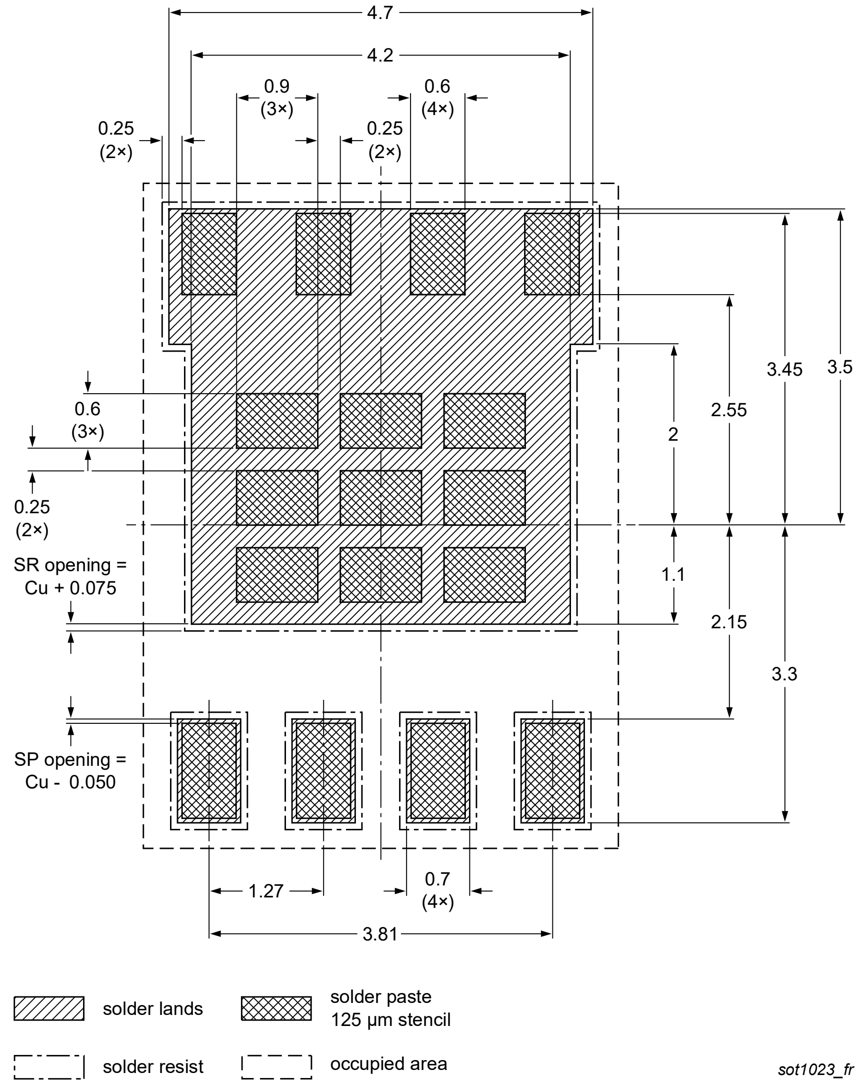


Fig. 4. Reflow soldering footprint for LFPAK56E; Power-SO8 (SOT1023)

12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Contents