



# PSMN1R3-80SSF

NextPower 80 V, 1.3 mOhm, 325 Amp, N-channel MOSFET in LFAK88 package

21 June 2023

Objective data sheet

## 1. General description

NextPower 80 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

## 2. Features and benefits

- Low  $Q_{rr}$  for higher efficiency and lower spiking
- 325 Amps  $I_{D(max)}$  continuous current rating
- Low  $Q_G \times R_{DS(on)}$  FOM for high efficiency switching applications
- Strong avalanche energy rating ( $E_{as}$ )
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFAK88 package

## 3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in DC-DC
- BLDC motor control
- Full-bridge and half-bridge applications
- Battery protection

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	325	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	341	W
$T_j$	junction temperature		-55	-	175	°C
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	0.9	1.3	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C}$	-	1.4	2.1	mΩ
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 40\text{ V}; V_{GS} = 10\text{ V}; T_j = 25\text{ °C}$	[tbd]	32.5	[tbd]	nC
$Q_{G(tot)}$	total gate charge		[tbd]	180	[tbd]	nC
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 92\text{ A}; V_{sup} \leq 80\text{ V}; R_{GS} = 50\text{ Ω}; V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; \text{unclamped}; t_p = 184\text{ μs}; \text{Fig. 2}$	[1]	-	878	mJ

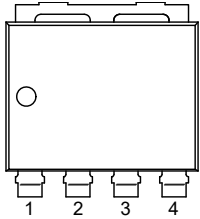
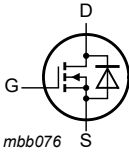
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$Q_r$	recovered charge	$I_S = 25 \text{ A}$ ; $di_S/dt = -100 \text{ A}/\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ; $V_{DS} = 40 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 6</a>	-	70	-	nC

[1] Protected by 100% test

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>LFAK88 (SOT1235)</p>	 <p>mbb076</p>
2	S	Source		
3	S	Source		
4	S	Source		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R3-80SSF	LFAK88	plastic, single-ended surface-mounted package (LFAK88); 4 leads; 2 mm pitch; 8 mm x 8 mm x 1.6 mm body	SOT1235

## 7. Limiting values

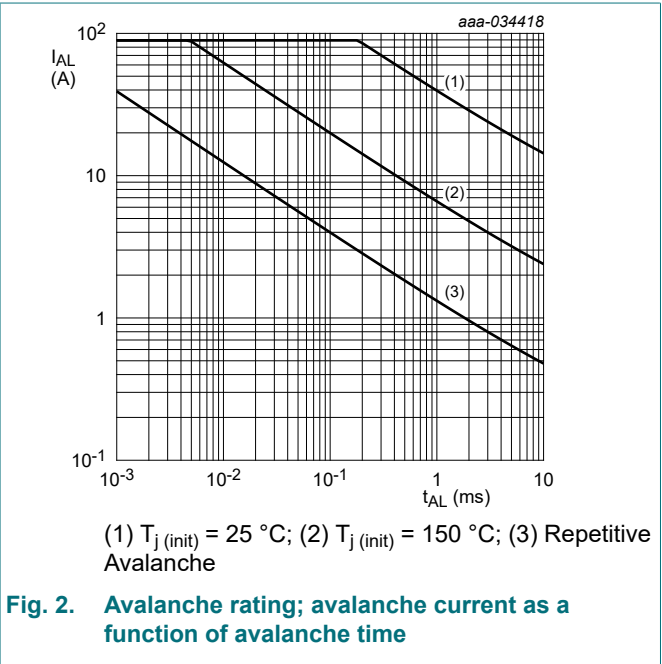
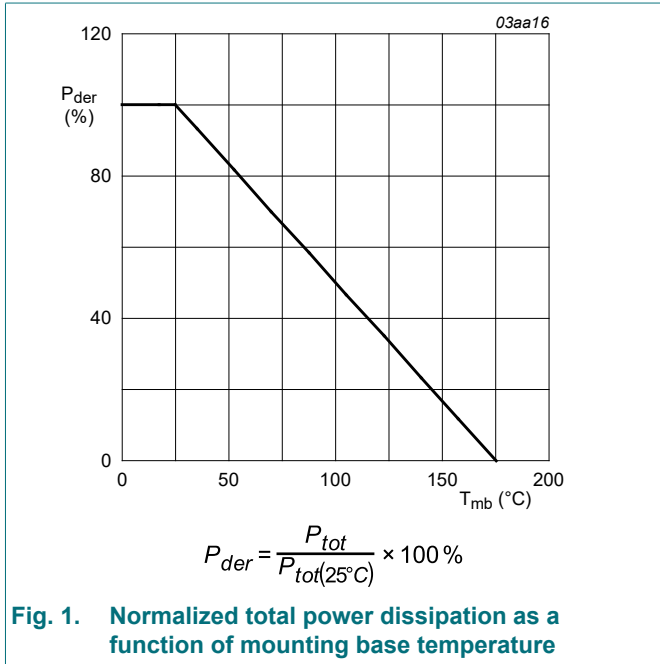
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).  $T_j = 25 \text{ }^\circ\text{C}$ , unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$	-	80	V
$V_{DGR}$	drain-gate voltage	$25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$ ; $R_{GS} = 20 \text{ k}\Omega$	-	80	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$ ; <a href="#">Fig. 1</a>	-	341	W
$I_D$	drain current	$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	325	A
		$V_{GS} = 10 \text{ V}$ ; $T_{mb} = 100 \text{ }^\circ\text{C}$	-	230	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10 \text{ }\mu\text{s}$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	1302	A
$T_{stg}$	storage temperature		-55	175	$^\circ\text{C}$
$T_j$	junction temperature		-55	175	$^\circ\text{C}$
$T_{sld(M)}$	peak soldering temperature		-	260	$^\circ\text{C}$
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	284	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10 \text{ }\mu\text{s}$ ; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	1302	A

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 92\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\ \Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ }^\circ\text{C}$ ; unclamped; $t_p = 184\ \mu\text{s}$ ; <a href="#">Fig. 2</a>	[1]	-	878	mJ
$I_{AS}$	non-repetitive avalanche current	$V_{sup} \leq 80\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ }^\circ\text{C}$ ; $R_{GS} = 50\ \Omega$ ; <a href="#">Fig. 2</a>	[1]	-	92	A

[1] Protected by 100% test



## 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 3</a>	-	0.2	0.44	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	<a href="#">Fig. 4</a>	-	35	-	K/W
		<a href="#">Fig. 5</a>	-	70	-	K/W

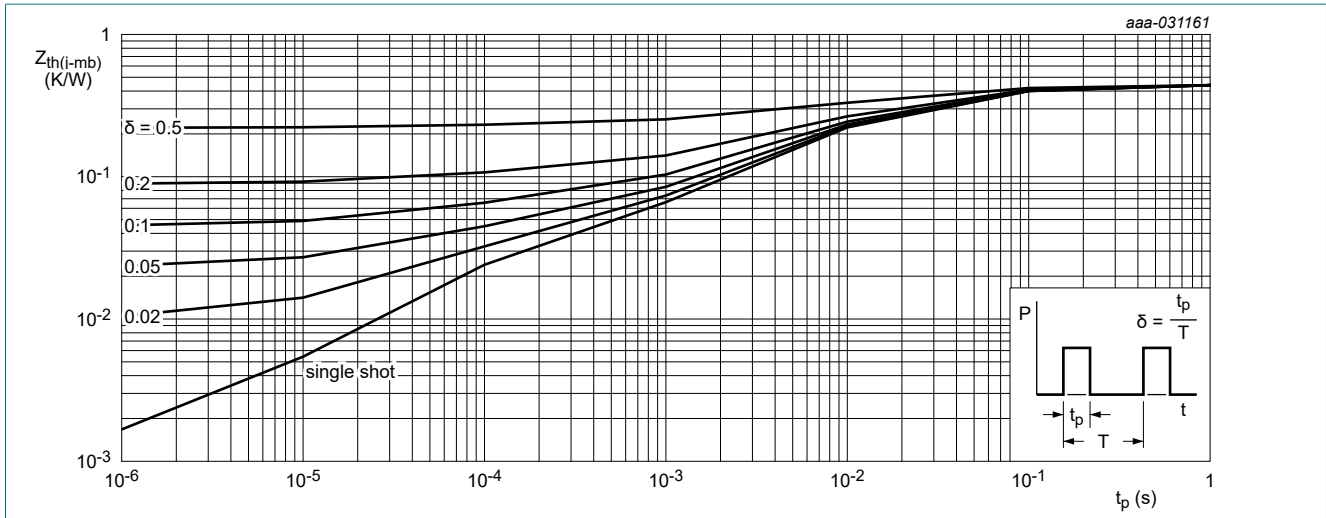


Fig. 3. Transient thermal impedance from junction to mounting base as a function of pulse duration

aaa-029383

Copper square 25.4 mm square; 70 μm thick on FR4 board

aaa-029384

70 μm thick copper on FR4 board

Fig. 4. PCB layout for thermal resistance from junction to ambient

Fig. 5. PCB layout with minimum footprint for thermal resistance from junction to ambient

## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	80	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	2.2	3	3.8	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.5	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$	-	1.7	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	-8.4	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.06	1	μA
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	7	100	μA
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA

NextPower 80 V, 1.3 mOhm, 325 Amp, N-channel MOSFET in LPAK88 package

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 25 °C	-	0.9	1.3	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 100 °C	-	1.4	2.1	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>J</sub> = 175 °C	-	2	3	mΩ
R <sub>G</sub>	gate resistance	f = 1 MHz; T <sub>J</sub> = 25 °C	[tbd]	0.63	[tbd]	Ω
<b>Dynamic characteristics</b>						
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 10 V; T <sub>J</sub> = 25 °C	[tbd]	180	[tbd]	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 10 V; T <sub>J</sub> = 25 °C	-	93	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 10 V; T <sub>J</sub> = 25 °C	[tbd]	54.5	[tbd]	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge		-	35.6	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge		-	18.9	-	nC
Q <sub>GD</sub>	gate-drain charge		[tbd]	32.5	[tbd]	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 25 A; V <sub>DS</sub> = 40 V; T <sub>J</sub> = 25 °C	-	4.5	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 40 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>J</sub> = 25 °C	[tbd]	13273	[tbd]	pF
C <sub>oss</sub>	output capacitance		[tbd]	3748	[tbd]	pF
C <sub>rss</sub>	reverse transfer capacitance		[tbd]	88	[tbd]	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 40 V; R <sub>L</sub> = 1.6 Ω; V <sub>GS</sub> = 10 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>J</sub> = 25 °C	-	47	-	ns
t <sub>r</sub>	rise time		-	36	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	98	-	ns
t <sub>f</sub>	fall time		-	51	-	ns
<b>Source-drain diode</b>						
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 25 A; V <sub>GS</sub> = 0 V; T <sub>J</sub> = 25 °C	-	0.8	1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 25 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 40 V; T <sub>J</sub> = 25 °C; Fig. 6	-	59	-	ns
Q <sub>r</sub>	recovered charge		-	70	-	nC

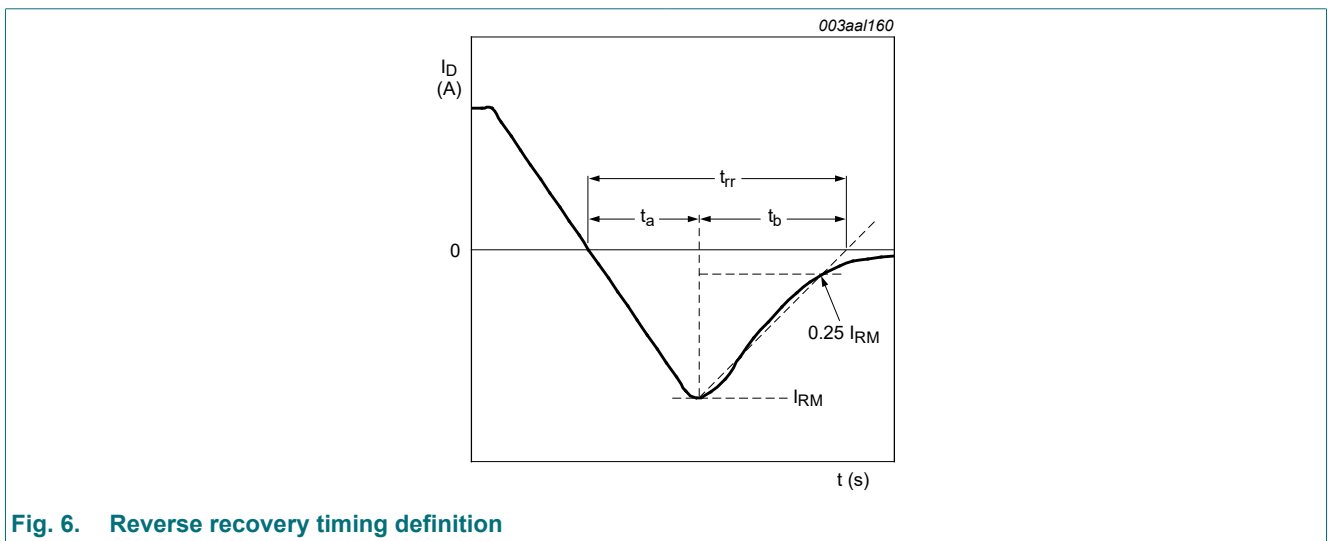


Fig. 6. Reverse recovery timing definition

10. Package outline

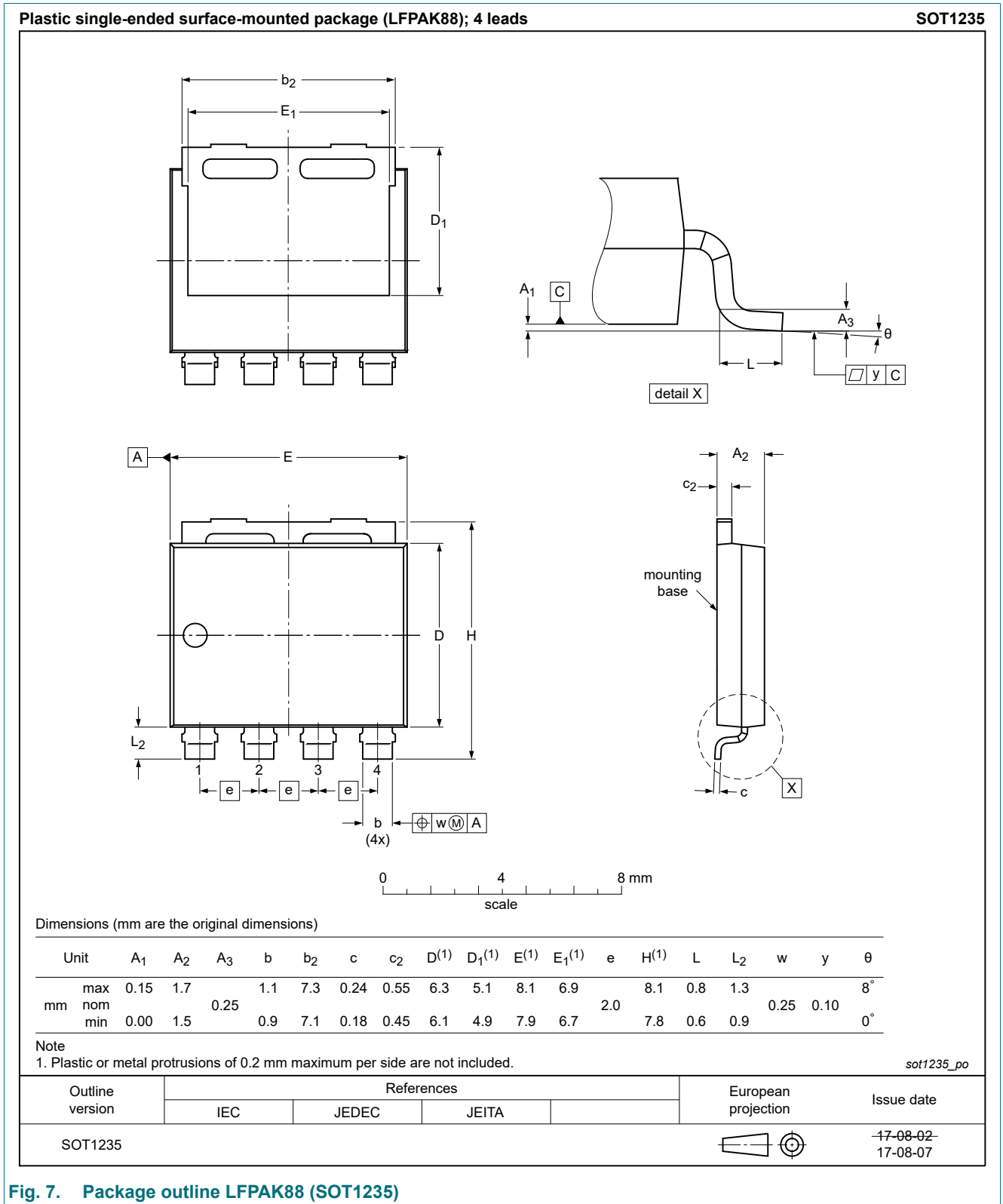
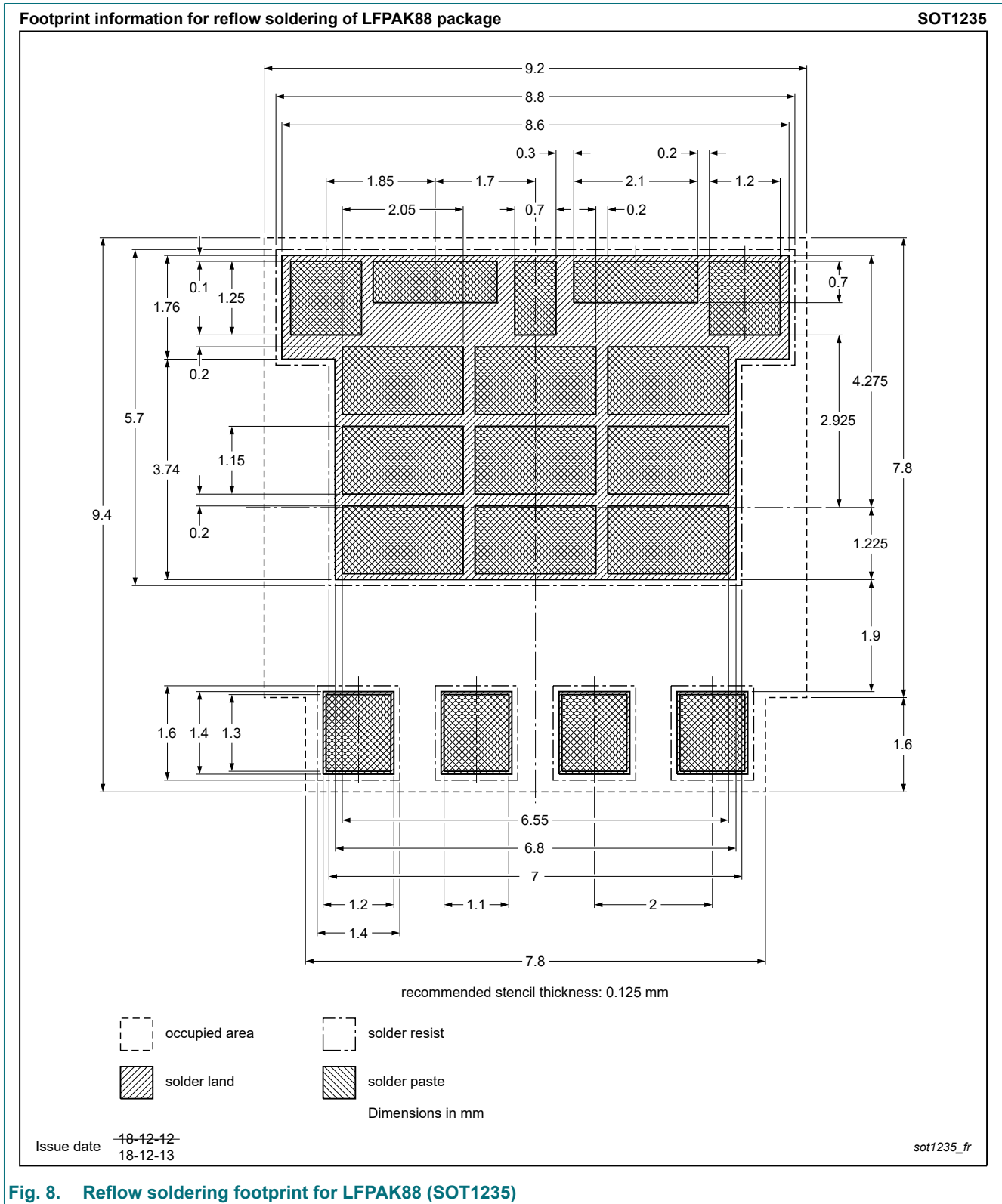


Fig. 7. Package outline LPAK88 (SOT1235)

### 11. Soldering



**Fig. 8. Reflow soldering footprint for LPAK88 (SOT1235)**

## 12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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