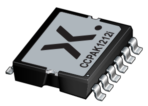


PSMN1R2-80CSE

N-channel, 80 V, 1.3 mOhm, MOSFET with enhanced SOA in CCPAK1212i package

21 October 2025 — Product data sheet

1. General description

N-channel enhancement mode MOSFET in a CCPAK1212i package qualified to 175 °C.
Part of Nexperia's Application Specific MOSFETs (ASFETs) for Hotswap and Soft Start. The PSMN1R2-80CSE delivers very low R_{DSon} and enhanced safe operating area performance in a high-reliability copper-clip package (CCPAK1212i).

PSMN1R2-80CSE complements the latest "hot-swap" controllers - robust enough to withstand substantial inrush currents during turn-on, low R_{DSon} to minimize I^2R losses and deliver optimum efficiency when turned fully ON.

2. Features and benefits

- Fully optimized Safe Operating Area (SOA) for superior linear mode operation
- Low R_{DSon} for low I^2R conduction losses
- CCPAK1212i package for applications that demand the highest performance and reliability
- Inverted package, suitable for top-side cooling
- CCPAK1212i is JEDEC listed package for open market and 2^{nd} source compatibility

3. Applications

- Hot swap
- Load switch
- Soft start
- E-fuse
- Telecommunication systems based on a 48 V backplane/supply rail

4. Quick reference data

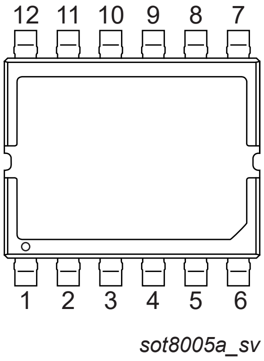
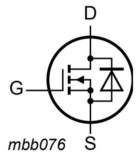
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	80	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	-	375	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	935	W
T_j	junction temperature			-55	-	175	°C
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11		-	1.17	1.3	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14		117	233	350	nC
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 40 V; T_j = 25 °C; Fig. 17		-	76.5	-	nC

nexperia

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 CCPAK1212i (SOT8005A)	
2	S	source		
3	S	source		
4	S	source		
5	S	source		
6	G	gate		
7	D	drain		
8	D	drain		
9	D	drain		
10	D	drain		
11	D	drain		
12	D	drain		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R2-80CSE	CCPAK1212i	Plastic, surface mounted copper clip package (CCPAK1212i); 12 terminals; 2.0 mm pitch, 12 mm × 12 mm × 2.5 mm body	SOT8005A

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R2-80CSE	XP1E2S80C

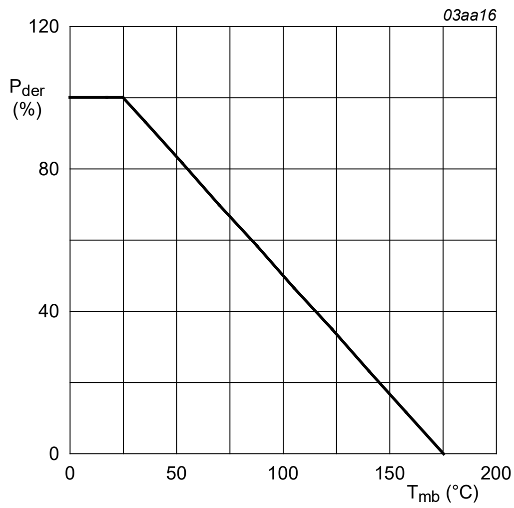
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).T_j = 25 °C unless otherwise stated.

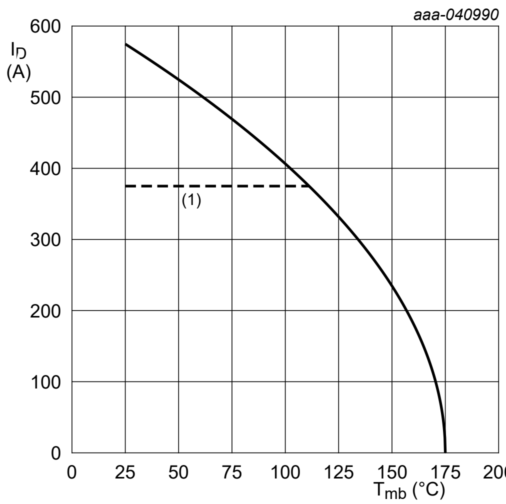
Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	80	V
V_{DGR}	drain-gate voltage	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ		-	80	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	935	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C; Fig. 2		-	375	A
		V_{GS} = 10 V; T_{mb} = 100 °C; Fig. 2		-	375	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C; Fig. 3		-	2236	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	340	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	2236	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 109 A; V_{sup} ≤ 80 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; t_p = 229 µs; Fig. 4	[1]	-	1300	mJ
I_{AS}	non-repetitive avalanche current	V_{sup} = 80 V; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; R_{GS} = 50 Ω; Fig. 4	[1]	-	109	A

[1] Protected by 100% test



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

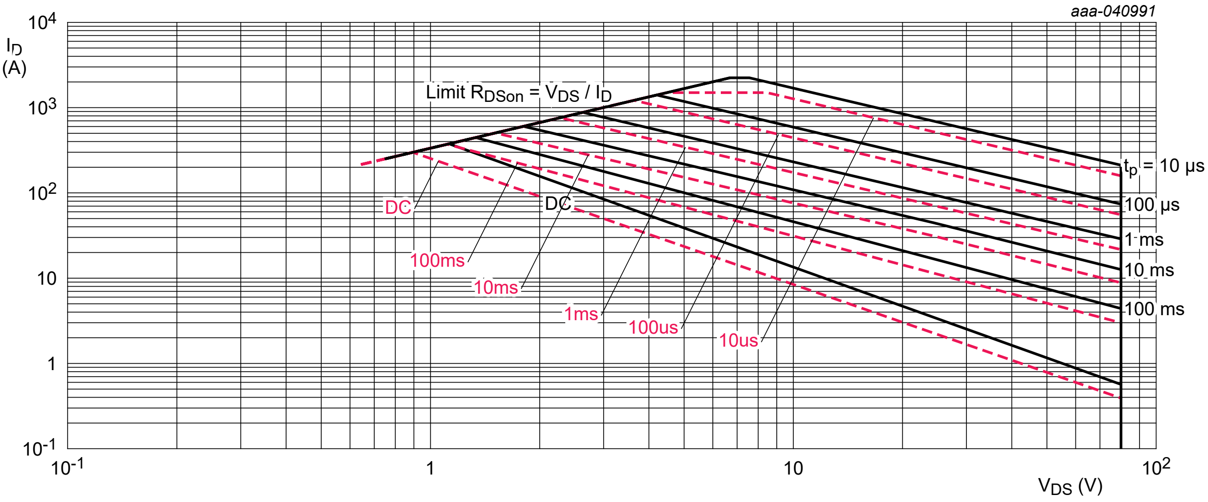
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



V_{GS} ≥ 10 V

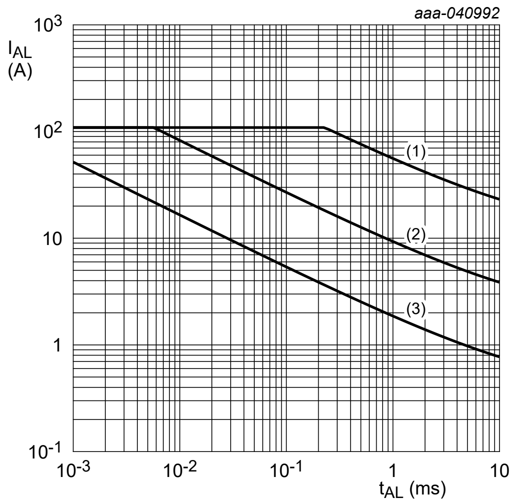
(1) 375 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C (solid black line); T_{mb} = 125 °C (red dashed line); I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\ (init)}$ = 25 °C; (2) $T_{j\ (init)}$ = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5		-	0.12	0.16	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 6		-	58	-	K/W
		Fig. 7		-	29	-	K/W

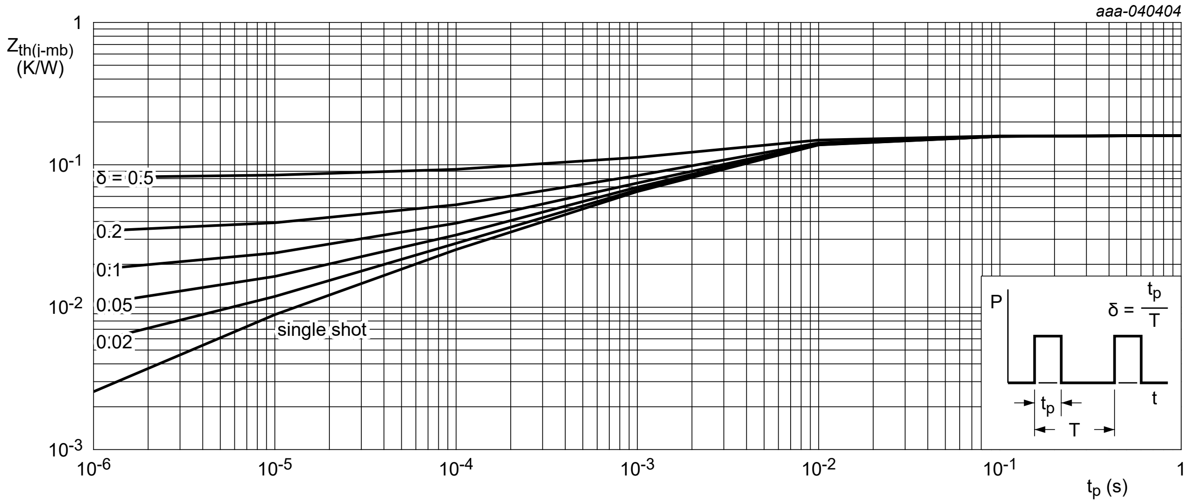
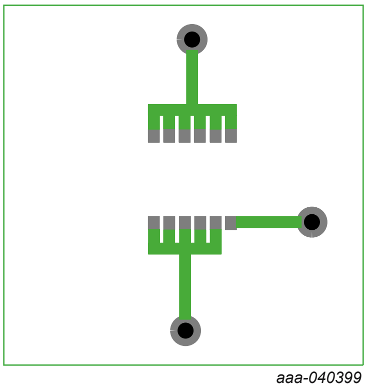
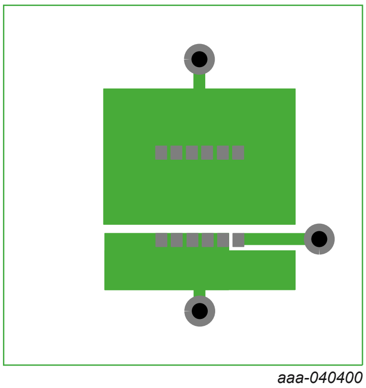


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



70 µm thick copper on FR4 board

Fig. 6. PCB layout with minimum footprint for thermal resistance from junction to ambient



Copper area 25.4 mm square; 70 µm thick on FR4 board

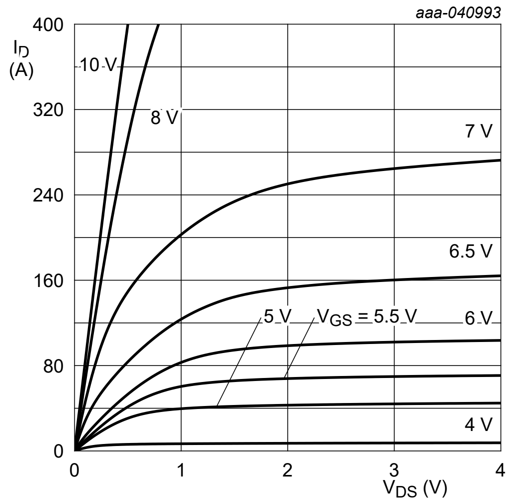
Fig. 7. PCB layout for thermal resistance from junction to ambient

10. Characteristics

Table 7. Characteristics

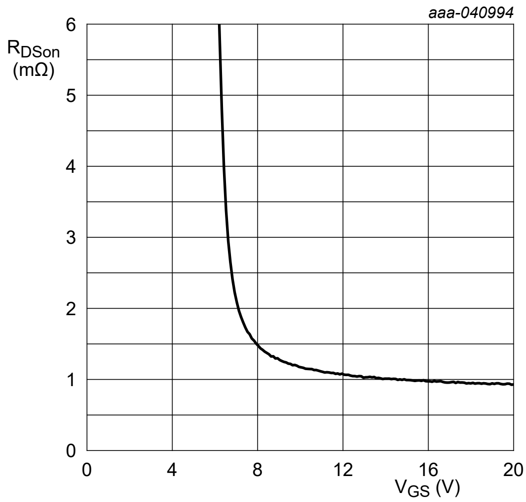
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		80	-	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C		2	2.8	3.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		-	1.75	-	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	3.3	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T_j ≤ 150 °C		-	-6.83	-	mV/K
I_{DSS}	drain leakage current	V_{DS} = 80 V; V_{GS} = 0 V; T_j = 25 °C		-	0.13	1.6	µA
		V_{DS} = 80 V; V_{GS} = 0 V; T_j = 125 °C		-	32	160	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11		-	1.17	1.3	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 100 °C; Fig. 12		-	1.7	2	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 12		-	2.4	3	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.56	1.12	2.24	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14		117	233	350	nC
		I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C		-	216	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 13; Fig. 14		51	84	118	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	53	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	31.5	-	nC
Q_{GD}	gate-drain charge			8	27.3	63	nC
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 40 V; T_j = 25 °C; Fig. 13; Fig. 14		-	4.7	-	V
C_{iss}	input capacitance	V_{DS} = 40 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C; Fig. 15		11223	18705	26187	pF
C_{oss}	output capacitance			2618	4363	6981	pF
C_{rss}	reverse transfer capacitance			11	106	319	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 40 V; R_L = 1.6 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	67	-	ns
t_r	rise time			-	57	-	ns
$t_{d(off)}$	turn-off delay time			-	133	-	ns
t_f	fall time			-	70	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 16		-	0.8	1	V

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 40 V; T_j = 25 °C; Fig. 17		-	62	-	ns
Q_r	recovered charge			-	76.5	-	nC



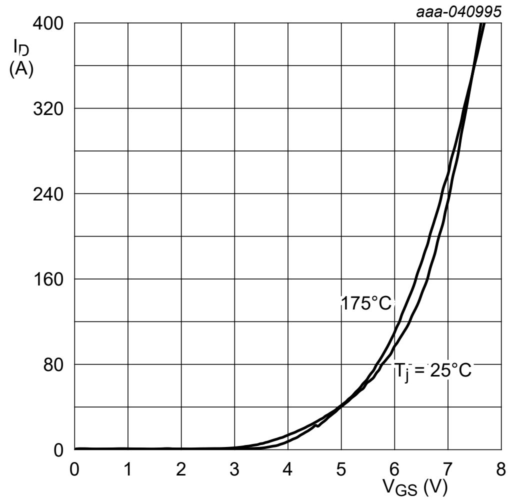
T_j = 25 °C

Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values



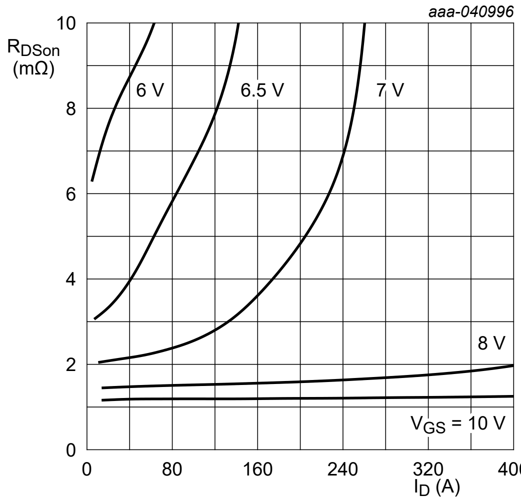
T_j = 25 °C; I_D = 25 A

Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



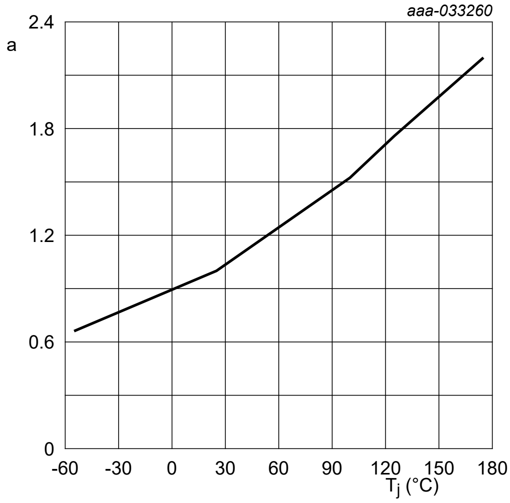
V_{DS} = 8 V

Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values



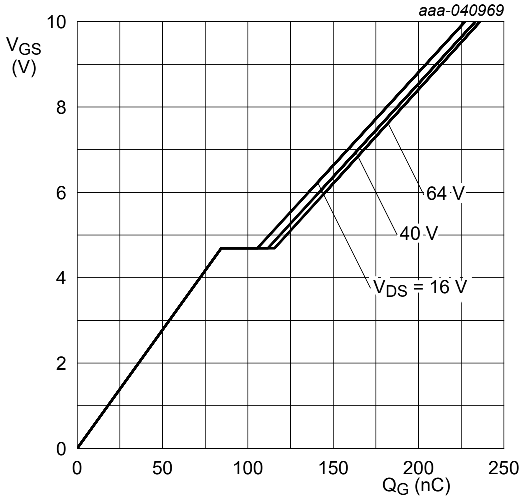
T_j = 25 °C

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25°C)}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature



T_j = 25 °C; I_D = 25 A

Fig. 13. Gate-source voltage as a function of gate charge; typical values

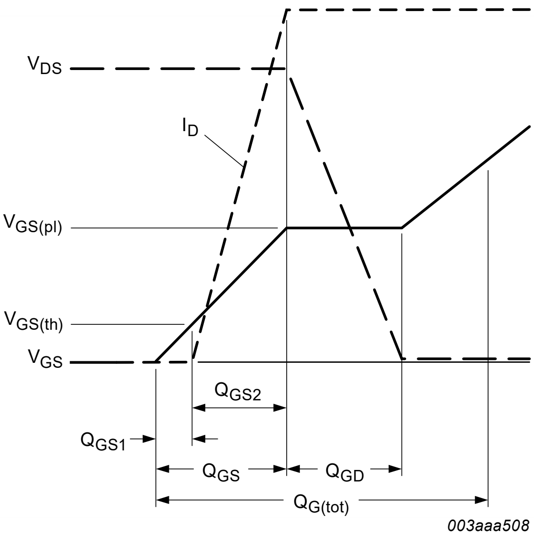
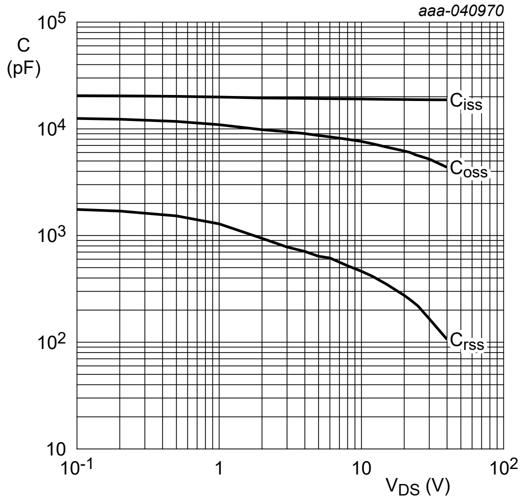


Fig. 14. Gate charge waveform definitions



V_{GS} = 0 V; f = 1 MHz

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

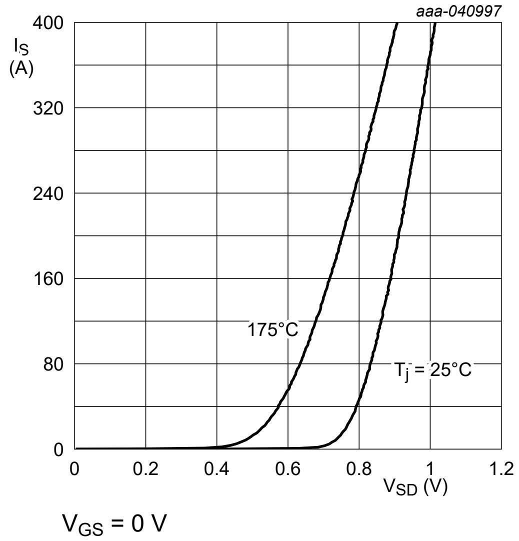


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

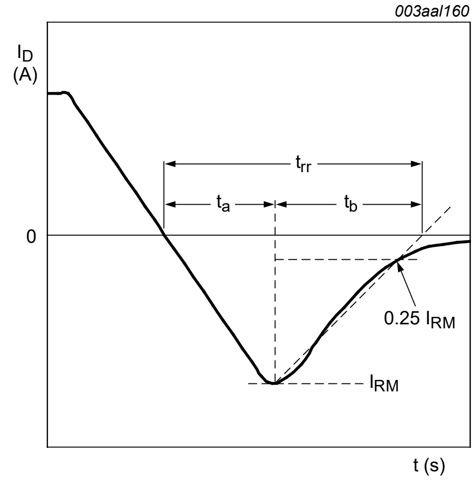
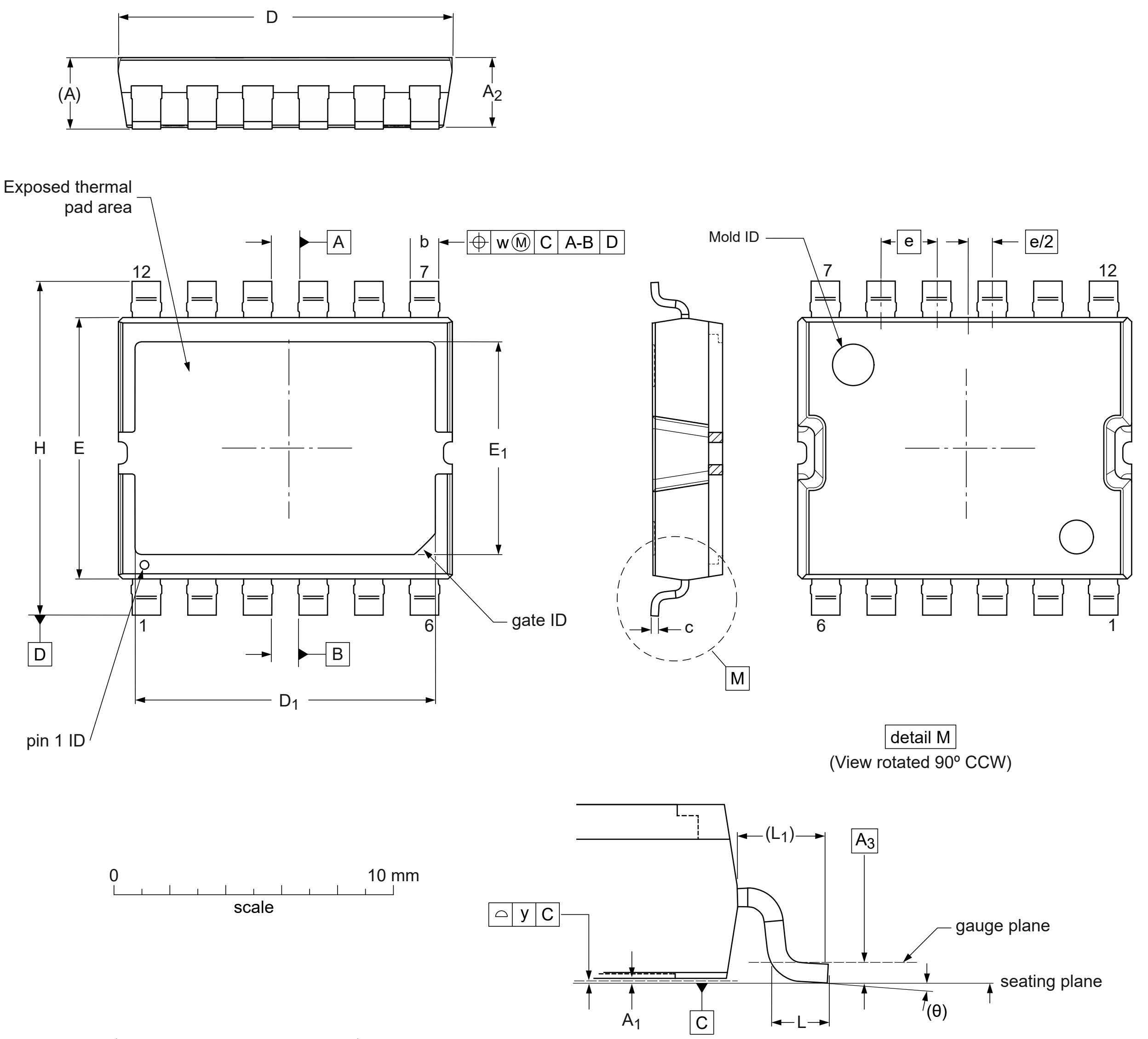


Fig. 17. Reverse recovery timing definition

11. Package outline

SOT8005A: Plastic, surface mounted copper clip package (CCPAK1212i); 12 terminals; 2.0 mm pitch, 12 mm × 12 mm × 2.5 mm body **SOT8005A**



Dimensions (mm are the original dimensions)

Unit[1]		A(ref)	A1	A2	A3	b	c	D	D1	E	E1	e	H	L	L1(ref)	w	y	θ(ref)
mm	max		0.13	2.525		1.12	0.30	12.15	10.95	9.55	7.40		12.15	1				
	nom	2.63			0.25							2.0			1.3	0.20	0.1	4°
	min		0	2.475		0.93	0.22	11.85	10.65	9.25	7.10		11.85	0.6				

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included for dimension D.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included for dimension E.

sot8005a_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8005A		MO-359				~~25-04-14~~ 25-05-06

Fig. 18. Package outline CCPAK1212i (SOT8005A)

12. Soldering

Footprint information for reflow soldering of CCPAK1212i package **SOT8005A**

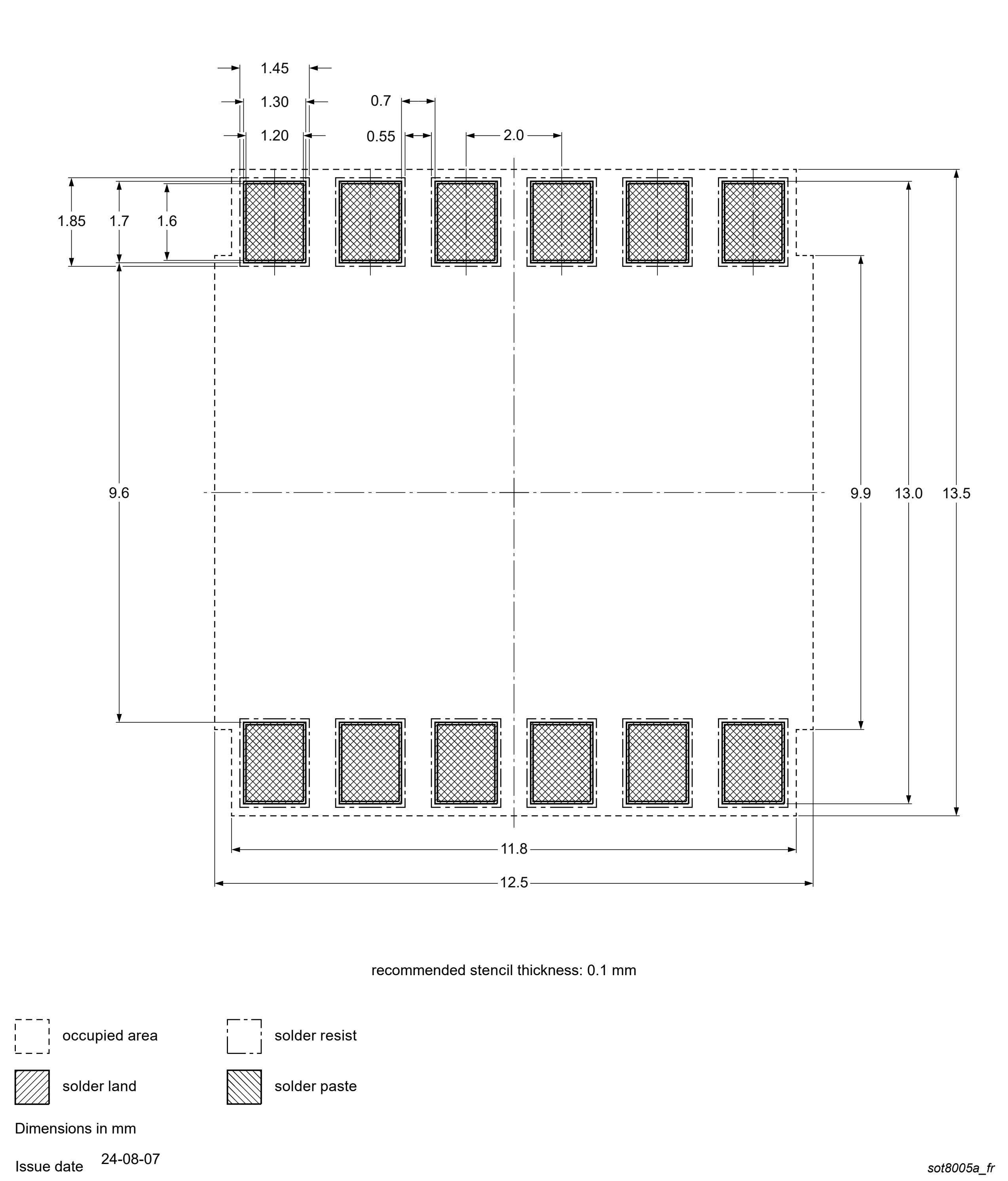


Fig. 19. Reflow soldering footprint for CCPAK1212i (SOT8005A)

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 21 October 2025