

PSMN1R1-80CSF

NextPower 80 V, 1.16 mOhm, N-channel MOSFET in CCPAK1212i package

13 May 2024

Objective data sheet

1. General description

NextPower 80 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for high power industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- 400 Amps I_{D(max)} continuous current rating
- Low Q_G × R_{DSon} FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{as})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant CCPAK1212i package
- · Inverted package, suitable for top-side cooling

3. Applications

- Battery protection
- High power full and half-bridge configurations
- · BLDC motor control
- OR-ing

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	80	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C	[1]	-	-	400	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	1.071	kW
Tj	junction temperature			-55	-	175	°C
Static charac	cteristics				·		
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C		-	0.92	1.16	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C		-	[tbd]	[tbd]	mΩ
Dynamic cha	racteristics						
Q_{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V;		-	34	-	nC
Q _{G(tot)}	total gate charge	T _j = 25 °C; <u>Fig. 2</u>		[tbd]	206	[tbd]	nC
Avalanche ru	ıggedness			'	'		
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	I_D = 109 A; $V_{sup} \le 80$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[2]	-	-	1325	mJ



Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Source-drain d	iode						
Q _r		$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 40 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 3$	[3]	-	82	-	nC

- [1] Max current will be demonstrated through application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
- [2] Protected by 100% test
- [3] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source	12 11 10 9 8 7	
4	S	source		
5	S	source		
6	G	gate		D
7	D	drain		
8	D	drain		G
9	D	drain		mbb076 S
10	D	drain	1 2 3 4 5 6	
11	D	drain	sot8005a_sv	
12	D	drain	CCPAK1212i (SOT8005A)	
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PSMN1R1-80CSF	CCPAK1212i	Plastic, surface mounted copper clip package (CCPAK1212i); 12 terminals; 2.0 mm pitch, 12 mm × 12 mm × 2.5 mm body	SOT8005A			

7. Limiting values

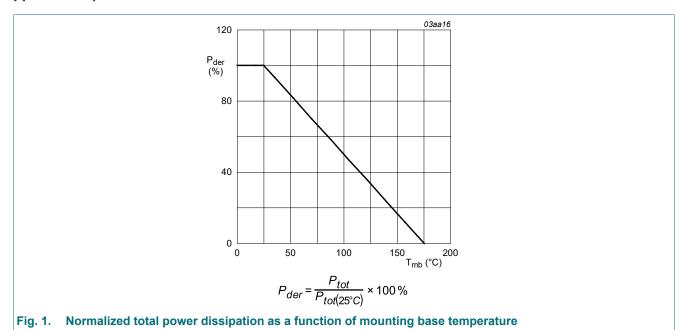
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). T_i = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	80	V
V _{GS}	gate-source voltage			-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 1</u>		-	1.071	kW
I_D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C	[1]	-	400	Α
		V _{GS} = 10 V; T _{mb} = 100 °C		-	282	Α
I _{DM}	peak drain current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$		-	1600	Α
T _{stg}	storage temperature			-55	175	°C
Tj	junction temperature			-55	175	°C
Source-drain	diode			'	•	_
Is	source current	T _{mb} = 25 °C		-	400	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \mu s$; $T_{mb} = 25 °C$		-	1600	Α
Avalanche ru	iggedness		'	'		
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	I_D = 109 A; V_{sup} ≤ 80 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[2]	-	1325	mJ

^[1] Max current will be demonstrated through application tests. Practically the current will be limited by PCB, thermal design and operating temperature.





8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base		-	[tbd]	0.14	K/W

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9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static charac	teristics					
V _{(BR)DSS}	drain-source	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	80	-	-	V
	breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	72	-	-	V
V _{GS(th)}	gate-source threshold	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}$	2	3	4	V
	voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C}$	-	1.6	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}$	-	3.5	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T _j ≤ 150 °C	-	[tbd]	-	mV/K
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C	-	[tbd]	5	μΑ
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 125 °C	-	[tbd]	[tbd]	μΑ
I _{GSS}	gate leakage current	V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
			-	2	100	nA
R _{DSon}	drain-source on-state	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C	-	0.92	1.16	mΩ
	resistance	V _{GS} = 7 V; I _D = 25 A; T _j = 25 °C	-	1.04	1.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 100 °C	-	[tbd]	[tbd]	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C	-	[tbd]	[tbd]	mΩ
R_G	gate resistance	f = 1 MHz; T _j = 25 °C	[tbd]	[tbd]	[tbd]	Ω
Dynamic cha	racteristics					
Q _{G(tot)}	total gate charge	I_D = 25 A; V_{DS} = 40 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 2	[tbd]	206	[tbd]	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V; T _i = 25 °C	-	107	-	nC
Q _{GS}	gate-source charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _i = 25 °C; <u>Fig. 2</u>	[tbd]	61	[tbd]	nC
Q _{GS(th)}	pre-threshold gate- source charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _i = 25 °C	-	42	-	nC
Q _{GS(th-pl)}	post-threshold gate- source charge		-	19	-	nC
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 40 V; V _{GS} = 10 V; T _i = 25 °C; Fig. 2	-	34	-	nC
V _{GS(pl)}	gate-source plateau voltage	I _D = 25 A; V _{DS} = 40 V; T _j = 25 °C	-	[tbd]	-	V
C _{iss}	input capacitance	V _{DS} = 40 V; V _{GS} = 0 V; f = 0.5 MHz;	[tbd]	15363	[tbd]	pF
C _{oss}	output capacitance	T _j = 25 °C	[tbd]	4580	[tbd]	pF
C _{rss}	reverse transfer capacitance		[tbd]	104	[tbd]	pF
t _{d(on)}	turn-on delay time	$V_{DS} = 40 \text{ V}; R_L = 1.6 \Omega; V_{GS} = 10 \text{ V};$	-	55	-	ns
t _r	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 °C$	-	46	-	ns
$t_{d(off)}$	turn-off delay time		-	127	-	ns
t _f	fall time		-	64	-	ns
Source-drain					1	
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _i = 25 °C	_	[tbd]	1	V

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
t _{rr}		$I_S = 25 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$		-	71	-	ns
Q _r	recovered charge	$V_{DS} = 40 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 3$	[1]	-	82	-	nC

[1] includes capacitive recovery

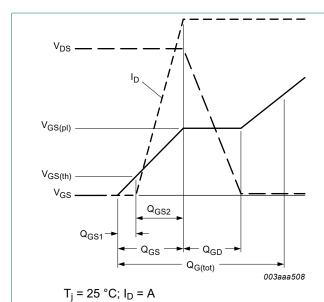


Fig. 2. Gate-source voltage as a function of gate charge; typical values

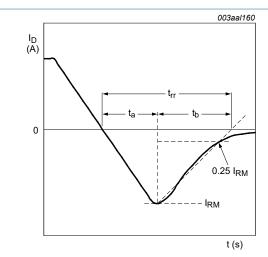
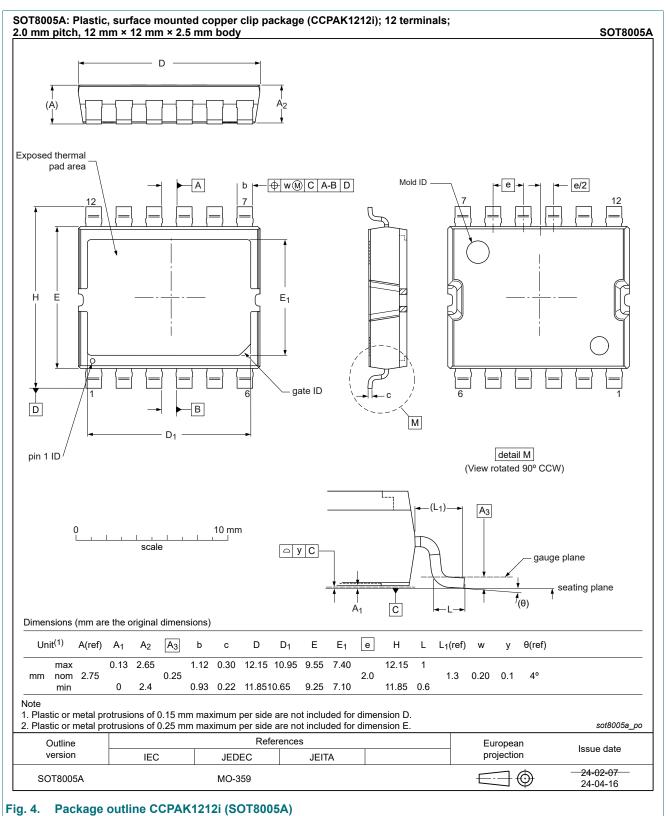


Fig. 3. Reverse recovery timing definition

10. Package outline



11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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