



PSMN012-100YSF

NextPower 100 V, 11.2 mOhm N-channel MOSFET in LFPAK56 package

25 January 2021

Objective data sheet

1. General description

NextPower 100 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

2. Features and benefits

- Low Q_{rr} for higher efficiency and lower spiking
- Low $Q_G \times R_{DS(on)}$ FOM for high efficiency switching applications
- Strong avalanche energy rating (E_{AS})
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFPAK56 package
- Wave-solderable LFPAK56 package

3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch – 48 V DC-DC
- BLDC motor control
- USB-PD and mobile fast-charge adapters
- Flyback and resonant topologies

4. Quick reference data

Table 1. Quick reference data

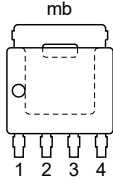
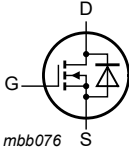
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$	-	-	53	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}; \text{Fig. 1}$	-	-	129	W
T_j	junction temperature		-55	-	175	°C
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$	-	8.5	11.2	mΩ
		$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C}$	-	14	18	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 25\text{ A}; V_{DS} = 50\text{ V}; V_{GS} = 10\text{ V}$	[tbd]	6	[tbd]	nC
$Q_{G(tot)}$	total gate charge		[tbd]	29	[tbd]	nC
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 29\text{ A}; V_{sup} \leq 100\text{ V}; R_{GS} = 50\text{ }\Omega; V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; \text{unclamped}$	[1]	-	88	mJ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
Q _r	recovered charge	I _S = 25 A; di _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 50 V; T _j = 25 °C; Fig. 5	-	29	-	nC

[1] Protected by 100% test

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LPAK56; Power-SO8 (SOT669)</p>	 <p>mbb076</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN012-100YSF	LPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Limiting values

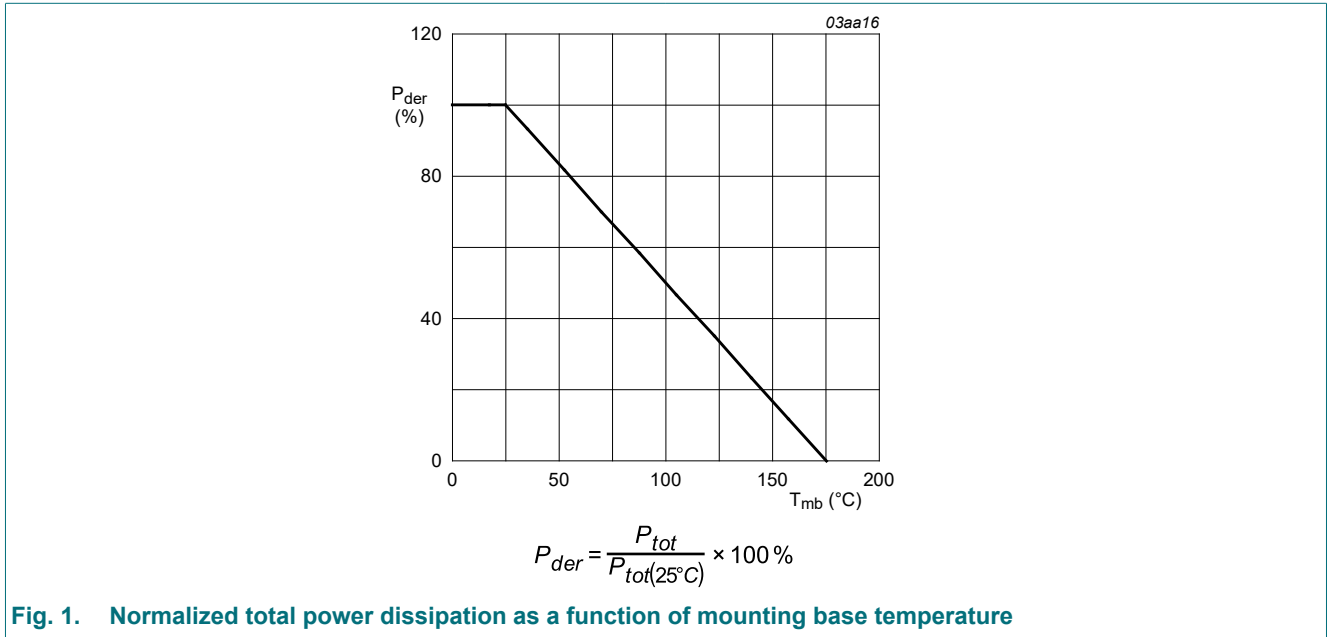
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C	-	100	V
V _{DGR}	drain-gate voltage	25 °C ≤ T _j ≤ 175 °C; R _{GS} = 20 kΩ	-	100	V
V _{GS}	gate-source voltage		-20	20	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1	-	129	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C	-	53	A
		V _{GS} = 10 V; T _{mb} = 100 °C	-	38	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	212	A
T _{stg}	storage temperature		-55	175	°C
T _j	junction temperature		-55	175	°C
T _{slid(M)}	peak soldering temperature		-	260	°C
Source-drain diode					
I _S	source current	T _{mb} = 25 °C	-	53	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C	-	212	A

Symbol	Parameter	Conditions		Min	Max	Unit
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 29\text{ A}$; $V_{sup} \leq 100\text{ V}$; $R_{GS} = 50\ \Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; unclamped	[1]	-	88	mJ
I_{AS}	non-repetitive avalanche current	$V_{sup} = 100\text{ V}$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $R_{GS} = 50\ \Omega$	[1]	-	29	A

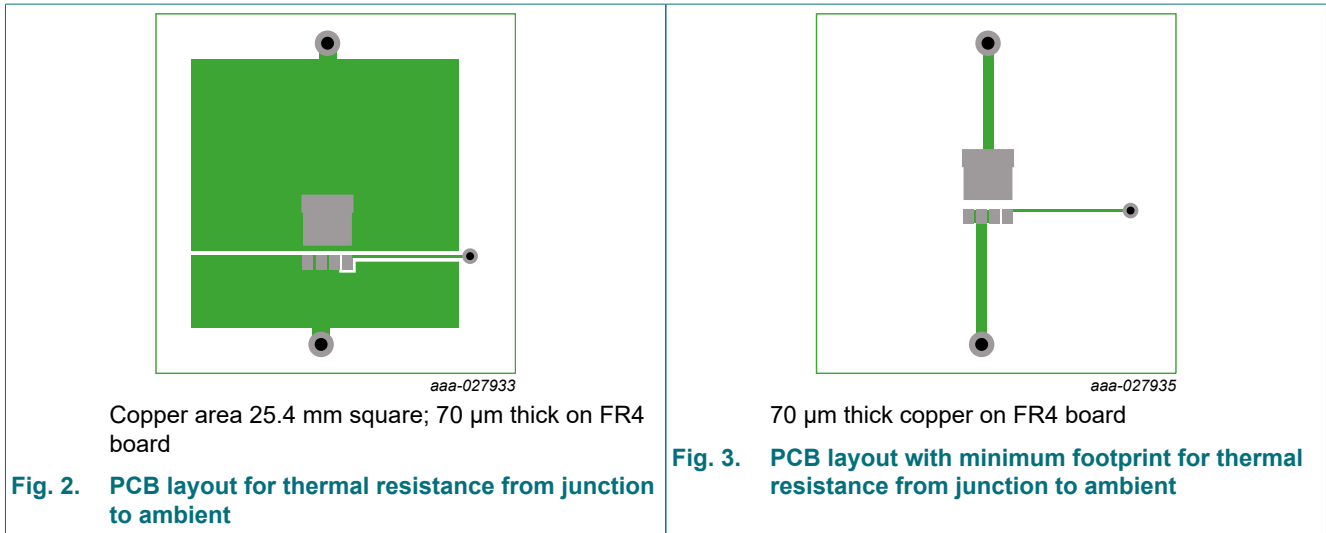
[1] Protected by 100% test



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	[tbd]	1.16	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 2		-	42	-	K/W
		Fig. 3		-	85	-	K/W

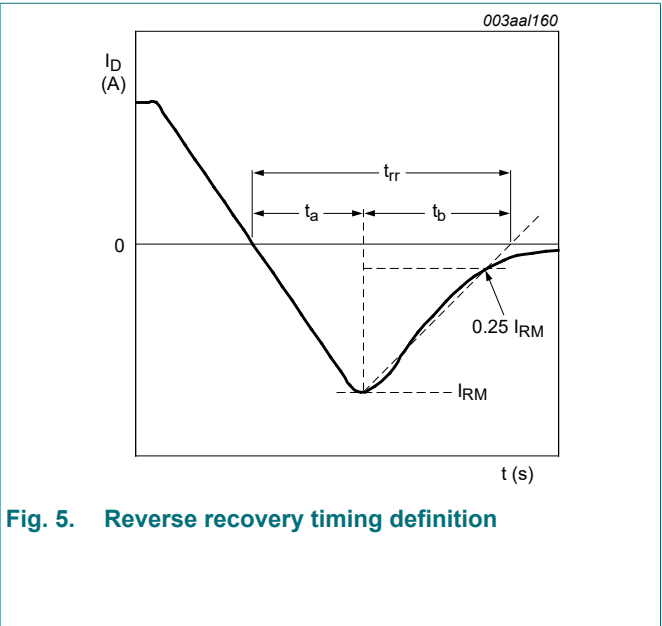
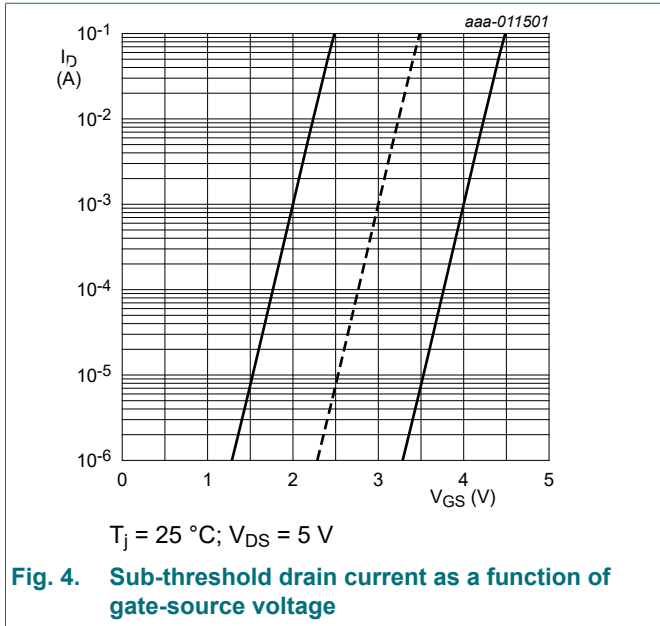


9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	100	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C; \text{Fig. 4}$	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 150 \text{ }^\circ C$	-	1.9	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$	-	3.5	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25 \text{ }^\circ C \leq T_j \leq 150 \text{ }^\circ C$	-	[tbd]	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	[tbd]	25	μA
		$V_{DS} = 100 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{DS} = 20 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{DS} = -20 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$	-	8.5	11.2	m Ω
		$V_{GS} = 7 \text{ V}; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$	-	10.5	13.5	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 100 \text{ }^\circ C$	-	14	18	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$	-	19.5	26	m Ω
R_G	gate resistance	$f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$	[tbd]	1.5	[tbd]	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V}$	[tbd]	29	[tbd]	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V}$	-	15	-	nC
Q_{GS}	gate-source charge	$I_D = 25 \text{ A}; V_{DS} = 50 \text{ V}; V_{GS} = 10 \text{ V}$	[tbd]	8.5	[tbd]	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	5.6	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	2.9	-	nC
Q_{GD}	gate-drain charge		[tbd]	6	[tbd]	nC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{GS(pl)}$	gate-source plateau voltage	$V_{DS} = 50\text{ V}$	-	4.5	-	V
C_{iss}	input capacitance	$V_{DS} = 50\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz}; T_j = 25\text{ }^\circ\text{C}$	[tbd]	2056	[tbd]	pF
C_{oss}	output capacitance		[tbd]	451	[tbd]	pF
C_{rss}	reverse transfer capacitance		[tbd]	14	[tbd]	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 50\text{ V}; R_L = 2\text{ }\Omega; V_{GS} = 10\text{ V}; R_{G(ext)} = 5\text{ }\Omega$	-	7.4	-	ns
t_r	rise time		-	6.3	-	ns
$t_{d(off)}$	turn-off delay time		-	18	-	ns
t_f	fall time		-	8.9	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	-	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; \text{Fig. 5}$	-	34	-	ns
Q_r	recovered charge	$I_S = 25\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; T_j = 25\text{ }^\circ\text{C}; \text{Fig. 5}$	-	29	-	nC



10. Package outline

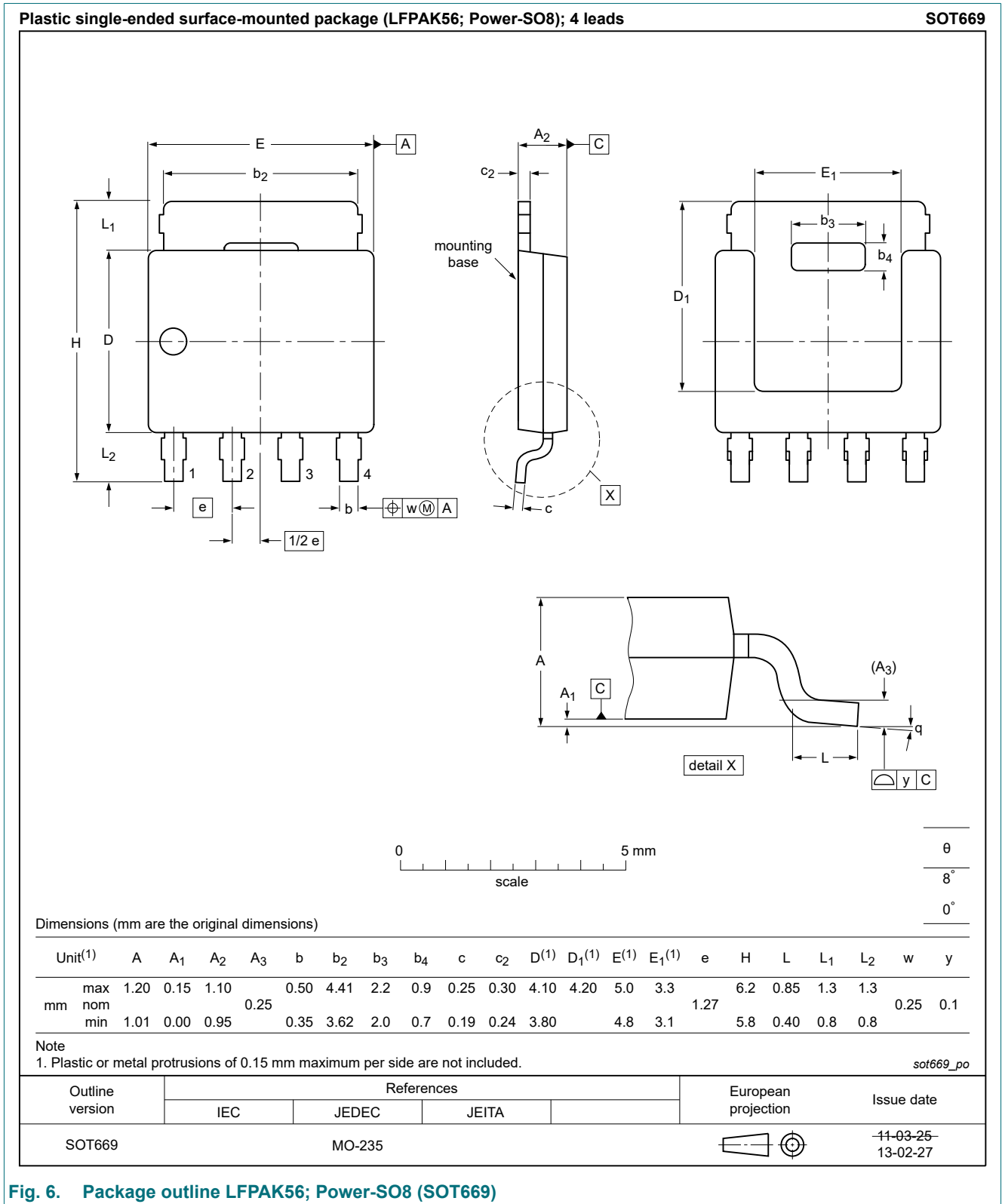


Fig. 6. Package outline LPAK56; Power-SO8 (SOT669)

11. Soldering

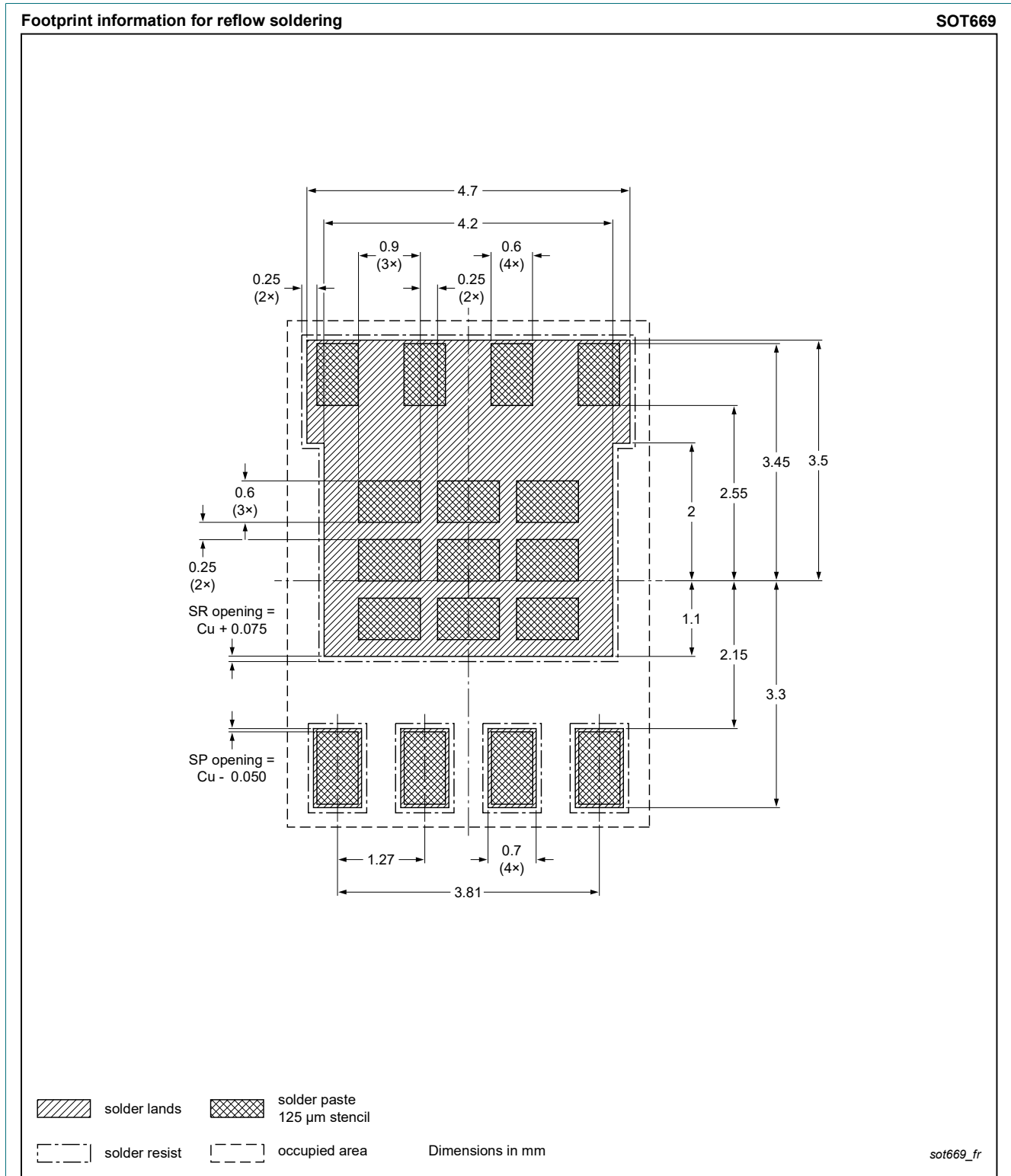
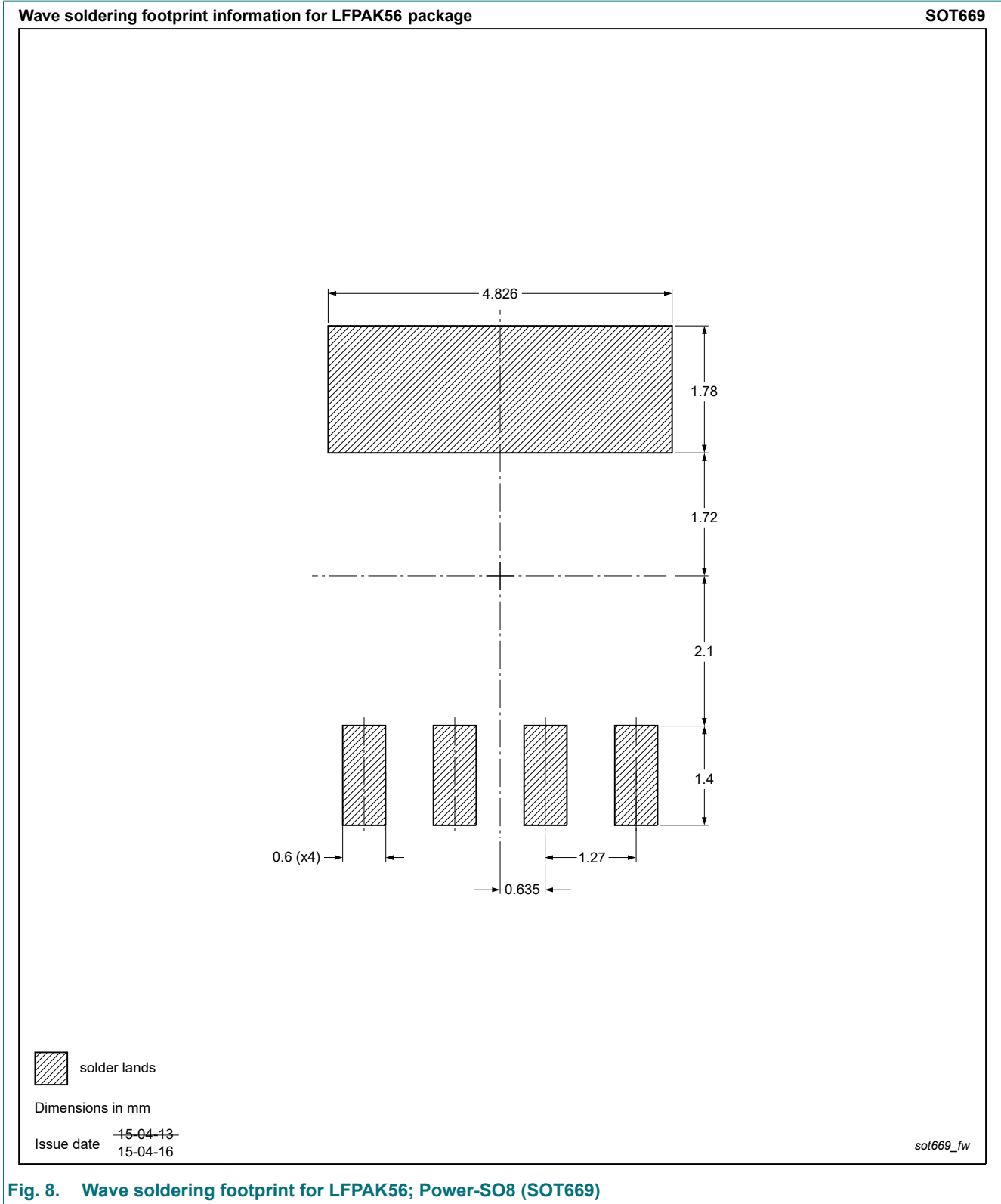


Fig. 7. Reflow soldering footprint for LPAK56; Power-SO8 (SOT669)



12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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