1. General description

NPN/PNP Resistor-Equipped double Transistors (RET) in a leadless ultra small DFN1412-6 (SOT1268) leadless Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PRMH11; PNP/PNP complement: PRMB11.

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- Low package height of 0.5 mm
- AEC-Q101 qualified

3. Applications

- Digital applications
- Cost-saving alternative to BC847/BC857 series in digital applications
- Control of IC inputs
- Switching loads

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CEO}$</td>
<td>collector-emitter voltage</td>
<td>open base</td>
<td>-</td>
<td>-</td>
<td>50</td>
<td>V</td>
</tr>
<tr>
<td>$I_O$</td>
<td>output current</td>
<td></td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>$h_{FE}$</td>
<td>DC current gain</td>
<td>$V_{CE} = 5 , V; , I_C = 5 , mA; , T_{amb} = 25 , ^\circ C$</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>R1</td>
<td>bias resistor 1</td>
<td>$T_{amb} = 25 , ^\circ C$</td>
<td>[1]</td>
<td>7</td>
<td>13</td>
<td>kΩ</td>
</tr>
<tr>
<td>R2/R1</td>
<td>bias resistor ratio</td>
<td></td>
<td>[1]</td>
<td>0.8</td>
<td>1</td>
<td>1.2</td>
</tr>
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</table>

[1] See section "Test information" for resistor calculation and test conditions.
5. Pinning information

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
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<tr>
<td>1</td>
<td>GND1</td>
<td>GND (emitter) TR1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>I1</td>
<td>input (base) TR1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>O2</td>
<td>output (collector) TR2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>GND2</td>
<td>GND (emitter) TR2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>I2</td>
<td>input (base) TR2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>O1</td>
<td>output (collector) TR1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>O1</td>
<td>output (collector) TR1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>O2</td>
<td>output (collector) TR2</td>
<td></td>
<td></td>
</tr>
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6. Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Description</th>
<th>Version</th>
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</thead>
<tbody>
<tr>
<td>PRMD3</td>
<td>DFN1412-6</td>
<td>plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 mm x 1.2 mm x 0.47 mm</td>
<td>SOT1268</td>
</tr>
</tbody>
</table>

7. Marking

Table 4. Marking codes

<table>
<thead>
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<th>Marking code</th>
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<tr>
<td>PRMD3</td>
<td>B3</td>
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</table>
8. Limiting values

Table 5. Limiting values

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CBO}$</td>
<td>collector-base voltage</td>
<td>open emitter</td>
<td>-</td>
<td>50</td>
<td>V</td>
</tr>
<tr>
<td>$V_{CEO}$</td>
<td>collector-emitter voltage</td>
<td>open base</td>
<td>-</td>
<td>50</td>
<td>V</td>
</tr>
<tr>
<td>$V_{EBO}$</td>
<td>emitter-base voltage</td>
<td>open collector</td>
<td>-</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>$V_I$</td>
<td>input voltage</td>
<td>positive</td>
<td>-</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>negative</td>
<td>-</td>
<td>-10</td>
<td>V</td>
</tr>
<tr>
<td>$I_O$</td>
<td>output current</td>
<td></td>
<td>-</td>
<td>100</td>
<td>mA</td>
</tr>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{amb} \leq 25 , ^\circ C$</td>
<td>[1]</td>
<td>-</td>
<td>325</td>
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</tbody>
</table>

**Per device**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P_{tot}$</td>
<td>total power dissipation</td>
<td>$T_{amb} \leq 25 , ^\circ C$</td>
<td>[1]</td>
<td>-</td>
<td>480</td>
</tr>
<tr>
<td>$T_j$</td>
<td>junction temperature</td>
<td></td>
<td>-</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{amb}$</td>
<td>ambient temperature</td>
<td></td>
<td>-55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{stg}$</td>
<td>storage temperature</td>
<td></td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>


![Fig. 1. Per device: Power derating curve](image-url)
9. Thermal characteristics

Table 6. Thermal characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{th(j-a)}$</td>
<td>thermal resistance from junction to ambient</td>
<td>in free air</td>
<td>[1]</td>
<td>-</td>
<td>-</td>
<td>385 K/W</td>
</tr>
<tr>
<td>$R_{th(j-a)}$</td>
<td>thermal resistance from junction to ambient</td>
<td>in free air</td>
<td>[1]</td>
<td>-</td>
<td>-</td>
<td>261 K/W</td>
</tr>
</tbody>
</table>


Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values
10. Characteristics

Table 7. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{CEO}$</td>
<td>collector-emitter cut-off current</td>
<td>$V_{CE} = 30 \text{ V}; I_B = 0 \text{ A}; T_{amb} = 25 \text{ °C}$</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$I_{CBO}$</td>
<td>collector-base cut-off current</td>
<td>$V_{CB} = 50 \text{ V}; I_E = 0 \text{ A}; T_{amb} = 25 \text{ °C}$</td>
<td>-</td>
<td>-</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>$I_{EBO}$</td>
<td>emitter-base cut-off current</td>
<td>$V_{EB} = 5 \text{ V}; I_C = 0 \text{ A}; T_{amb} = 25 \text{ °C}$</td>
<td>-</td>
<td>-</td>
<td>400</td>
<td>$\mu$A</td>
</tr>
<tr>
<td>$h_{FE}$</td>
<td>DC current gain</td>
<td>$V_{CE} = 5 \text{ V}; I_C = 5 \text{ mA}; T_{amb} = 25 \text{ °C}$</td>
<td>30</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>$V_{CESat}$</td>
<td>collector-emitter saturation voltage</td>
<td>$I_C = 10 \text{ mA}; I_B = 0.5 \text{ mA}; T_{amb} = 25 \text{ °C}$</td>
<td>-</td>
<td>-</td>
<td>150</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{I(off)}$</td>
<td>off-state input voltage</td>
<td>$V_{CE} = 5 \text{ V}; I_C = 100 \mu\text{A}; T_{amb} = 25 \text{ °C}$</td>
<td>-</td>
<td>1.1</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>$V_{I(on)}$</td>
<td>on-state input voltage</td>
<td>$V_{CE} = 0.3 \text{ V}; I_C = 10 \text{ mA}; T_{amb} = 25 \text{ °C}$</td>
<td>2.5</td>
<td>1.8</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>$R1$</td>
<td>bias resistor 1</td>
<td>$T_{amb} = 25 \text{ °C}$</td>
<td>7</td>
<td>10</td>
<td>13</td>
<td>kΩ</td>
</tr>
<tr>
<td>$R2/R1$</td>
<td>bias resistor ratio</td>
<td>0.8</td>
<td>1</td>
<td>1.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_C$</td>
<td>collector capacitance</td>
<td>$V_{CE} = 10 \text{ V}; I_E = 0 \text{ A}; I_E = 0 \text{ A}; f = 1 \text{ MHz}; T_{amb} = 25 \text{ °C}$</td>
<td>-</td>
<td>-</td>
<td>2.5</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CE} = -10 \text{ V}; I_E = 0 \text{ A}; I_E = 0 \text{ A}; f = 1 \text{ MHz}; T_{amb} = 25 \text{ °C}$</td>
<td>-</td>
<td>-</td>
<td>3</td>
<td>pF</td>
</tr>
<tr>
<td>$f_T$</td>
<td>transition frequency</td>
<td>$V_{CE} = 5 \text{ V}; I_C = 10 \text{ mA}; f = 100 \text{ MHz}; T_{amb} = 25 \text{ °C}$</td>
<td>[2]</td>
<td>-</td>
<td>230</td>
<td>MHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CE} = -5 \text{ V}; I_C = -10 \text{ mA}; f = 100 \text{ MHz}; T_{amb} = 25 \text{ °C}$</td>
<td>[2]</td>
<td>-</td>
<td>180</td>
<td>MHz</td>
</tr>
</tbody>
</table>

[1] See section "Test information" for resistor calculation and test conditions.

Fig. 3. NPN transistor: DC current gain as a function of collector current; typical values

Fig. 4. NPN transistor: Collector current as a function of collector-emitter voltage; typical values

$V_{CE} = 5 \text{ V}$
(1) $T_{amb} = 100 \text{ °C}$
(2) $T_{amb} = 25 \text{ °C}$
(3) $T_{amb} = 40 \text{ °C}$

Fig. 4. NPN transistor: Collector current as a function of collector-emitter voltage; typical values

$T_{amb} = 25 \text{ °C}$
Fig. 5. **NPN transistor: Collector-emitter saturation voltage as a function of collector current; typical values**

\[ V_{CE\text{sat}} (\text{V}) \]

- $I_C/I_B = 20$
- (1) $T_{\text{amb}} = 100 \, ^\circ\text{C}$
- (2) $T_{\text{amb}} = 25 \, ^\circ\text{C}$
- (3) $T_{\text{amb}} = -40 \, ^\circ\text{C}$

$V_{CE\text{sat}} = 0.3 \, \text{V}$
- (1) $T_{\text{amb}} = -40 \, ^\circ\text{C}$
- (2) $T_{\text{amb}} = 25 \, ^\circ\text{C}$
- (3) $T_{\text{amb}} = 100 \, ^\circ\text{C}$

Fig. 6. **NPN transistor: On-state input voltage as a function of collector current; typical values**

\[ V_{I(\text{on})} (\text{V}) \]

$V_{CE} = 5 \, \text{V}$
- (1) $T_{\text{amb}} = -40 \, ^\circ\text{C}$
- (2) $T_{\text{amb}} = 25 \, ^\circ\text{C}$
- (3) $T_{\text{amb}} = 100 \, ^\circ\text{C}$

$V_{CE} = 0.3 \, \text{V}$
- (1) $T_{\text{amb}} = -40 \, ^\circ\text{C}$
- (2) $T_{\text{amb}} = 25 \, ^\circ\text{C}$
- (3) $T_{\text{amb}} = 100 \, ^\circ\text{C}$

Fig. 7. **NPN transistor: Off-state input voltage as a function of collector current; typical values**

\[ V_{I(\text{off})} (\text{V}) \]

$V_{CE} = 5 \, \text{V}$
- (1) $T_{\text{amb}} = -40 \, ^\circ\text{C}$
- (2) $T_{\text{amb}} = 25 \, ^\circ\text{C}$
- (3) $T_{\text{amb}} = 100 \, ^\circ\text{C}$

$V_{CE} = 0.3 \, \text{V}$
- (1) $T_{\text{amb}} = -40 \, ^\circ\text{C}$
- (2) $T_{\text{amb}} = 25 \, ^\circ\text{C}$
- (3) $T_{\text{amb}} = 100 \, ^\circ\text{C}$

Fig. 8. **NPN transistor: Collector capacitance as a function of collector-base voltage; typical values**

\[ C_C (\text{pF}) \]

- $f = 1 \, \text{MHz}$
- $T_{\text{amb}} = 25 \, ^\circ\text{C}$

$V_{CE} = 5 \, \text{V}$
- (1) $T_{\text{amb}} = -40 \, ^\circ\text{C}$
- (2) $T_{\text{amb}} = 25 \, ^\circ\text{C}$
- (3) $T_{\text{amb}} = 100 \, ^\circ\text{C}$

$V_{CE} = 0.3 \, \text{V}$
- (1) $T_{\text{amb}} = -40 \, ^\circ\text{C}$
- (2) $T_{\text{amb}} = 25 \, ^\circ\text{C}$
- (3) $T_{\text{amb}} = 100 \, ^\circ\text{C}$
50 V, 100 mA NPN/PNP Resistor-Equipped double Transistors (RET)

**Fig. 9.** NPN transistor: Transition frequency as a function of collector current; typical values of built-in transistor

\[ V_{CE} = 5 \text{ V}, \ T_{amb} = 25 \ ^\circ\text{C} \]

**Fig. 10.** PNP transistor: DC current gain as a function of collector current; typical values

\[ V_{CE} = -5 \text{ V} \]

(1) \( T_{amb} = 100 \ ^\circ\text{C} \)

(2) \( T_{amb} = 25 \ ^\circ\text{C} \)

(3) \( T_{amb} = -40 \ ^\circ\text{C} \)

**Fig. 11.** PNP transistor: Collector current as a function of collector-emitter voltage; typical values

\[ T_{amb} = 25 \ ^\circ\text{C} \]

**Fig. 12.** PNP transistor: Collector-emitter saturation voltage as a function of collector current; typical values

\[ I_{C}/I_{B} = 20 \]

(1) \( T_{amb} = 100 \ ^\circ\text{C} \)

(2) \( T_{amb} = 25 \ ^\circ\text{C} \)

(3) \( T_{amb} = -40 \ ^\circ\text{C} \)
Fig. 13. PNP transistor: On-state input voltage as a function of collector current; typical values

Fig. 14. PNP transistor: Off-state input voltage as a function of collector current; typical values

Fig. 15. PNP transistor: Collector capacitance as a function of collector-base voltage; typical values

Fig. 16. PNP transistor: Transition frequency as a function of collector current; typical values of built-in transistor
11. Test information

Quality information
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

Resistor calculation
- Calculation of bias resistor 1 (R1)
  \[ R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1} \]
- Calculation of bias resistor ratio (R2/R1)
  \[ \frac{R_2}{R_1} = \frac{V(I_2) - V(I_1)}{R_1 \cdot (I_2 - I_1)} - 1 \]

Fig. 17. NPN transistor: Resistor test circuit

Fig. 18. PNP transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions
Per transistor; for the PNP transistor with negative polarity

<table>
<thead>
<tr>
<th>R1 (kΩ)</th>
<th>R2 (kΩ)</th>
<th>Test conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>10</td>
<td>I_1: 350 μA, I_2: 450 μA, I_3: -350 μA, I_4: -450 μA</td>
</tr>
</tbody>
</table>
12. Package outline

DFN1412-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body: 1.4 x 1.2 x 0.47 mm

Fig. 19. Package outline DFN1412-6 (SOT1268)
13. Soldering

Footprint information for reflow soldering of DFN1412-6 package

Fig. 20. Reflow soldering footprint for DFN1412-6 (SOT1268)
## 14. Revision history

<table>
<thead>
<tr>
<th>Data sheet ID</th>
<th>Release date</th>
<th>Data sheet status</th>
<th>Change notice</th>
<th>Supersedes</th>
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Document status | Product status | Definition
--- | --- | ---
[1][2] | [3] | [1] Please consult the most recently issued document before initiating or completing a design.

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