



PMPB50XN

110 V, N-channel Trench MOSFET

16 May 2024

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020M-6 (SOT1220-2) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology

3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

4. Quick reference data

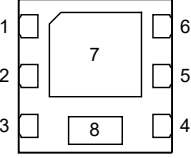
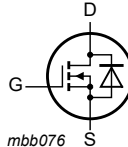
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	110	V
V_{GS}	gate-source voltage		-12	-	12	V
I_D	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	5	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	3.9	A
		$V_{GS} = 4.5\text{ V}; T_{sp} = 25\text{ °C}$		-	-	9.9
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 3.9\text{ A}; T_j = 25\text{ °C}$	-	50	70	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view DFN2020M-6 (SOT1220-2)</p>	 <p><i>mbb076</i></p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB50XN	DFN2020M-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1220-2

7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB50XN	RK

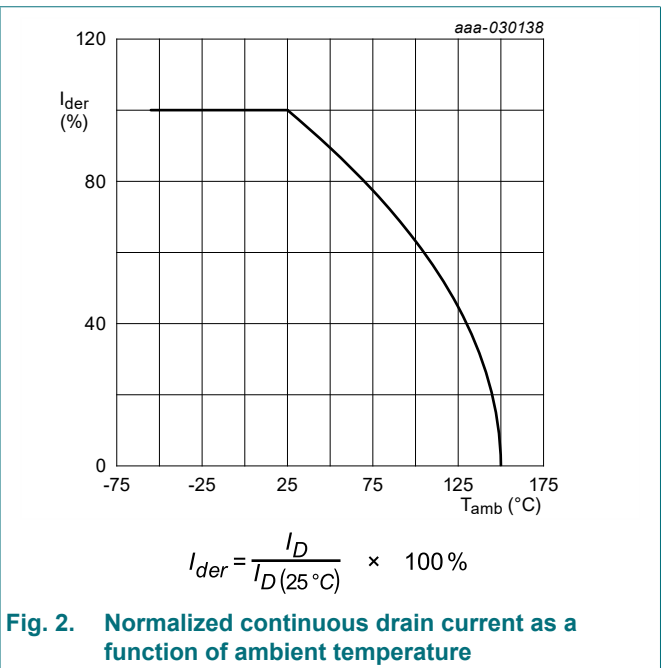
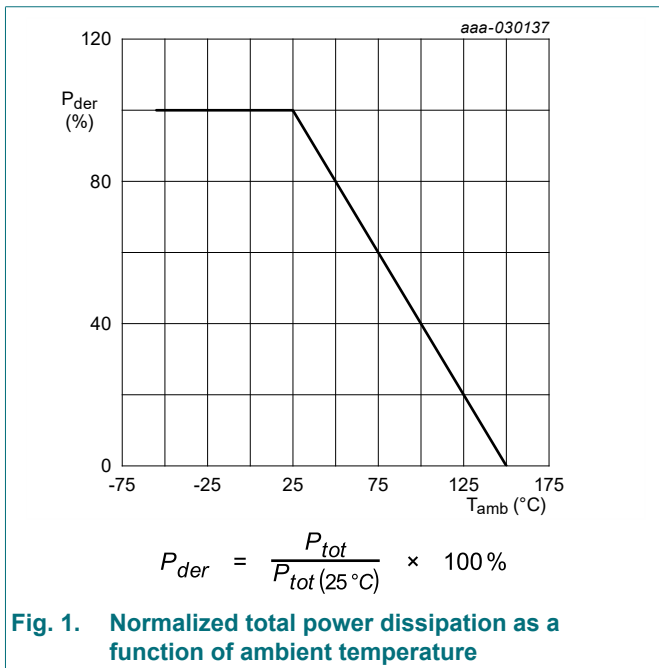
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	110	V
V _{GS}	gate-source voltage			-12	12	V
I _D	drain current	V _{GS} = 4.5 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	5	A
		V _{GS} = 4.5 V; T _{amb} = 25 °C	[1]	-	3.9	A
		V _{GS} = 4.5 V; T _{sp} = 25 °C		-	9.9	A
		V _{GS} = 4.5 V; T _{amb} = 100 °C	[1]	-	2.3	A
		V _{GS} = 4.5 V; T _{sp} = 100 °C		-	6.3	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	39.6	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	0.58	W
			[1]	-	1.7	W
		T _{sp} = 25 °C		-	13	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	1.5	A
		T _{sp} = 25 °C		-	9.9	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	T _{j(initial)} = 25 °C; I _D = 1.2 A; DUT in avalanche (unclamped)		-	52.8	mJ

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



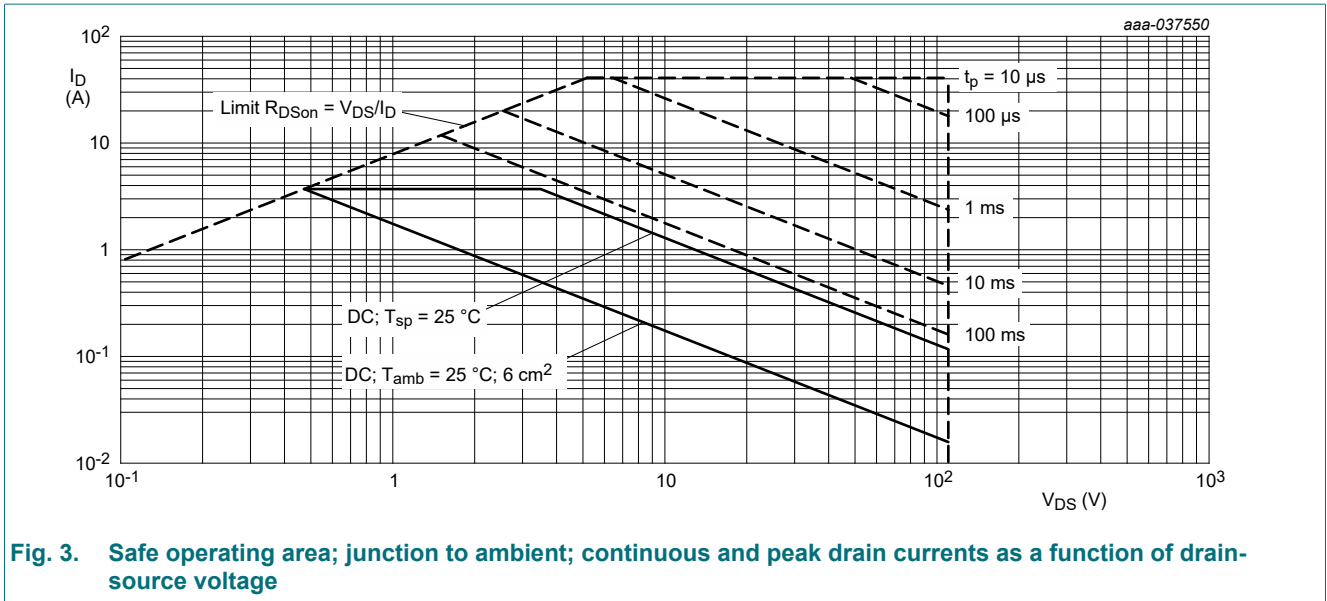


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	189	217	K/W
			[2]	-	64	74	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	6	10	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm².

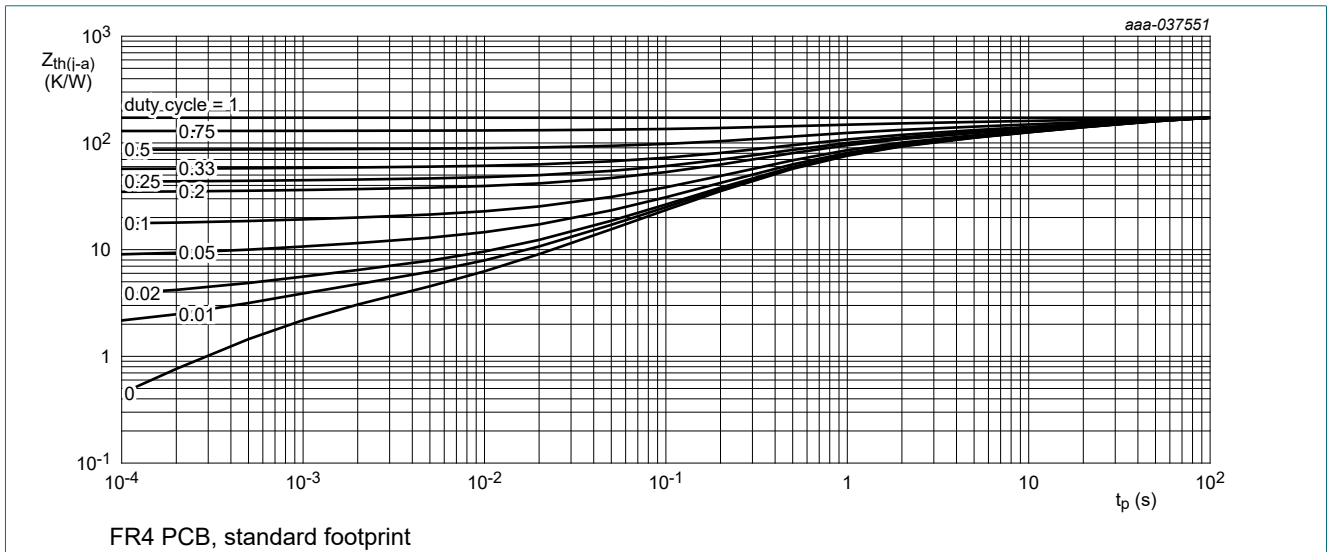


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

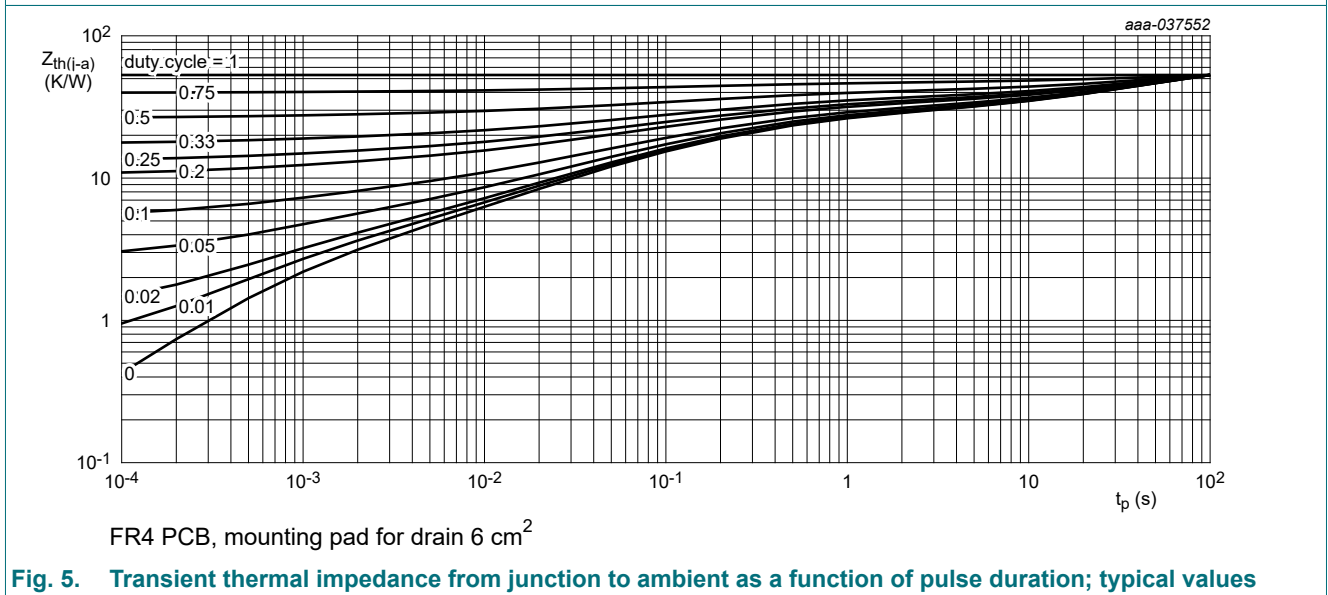


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 10 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	110	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \text{ } \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	0.5	1	1.4	V
I_{DSS}	drain leakage current	$V_{DS} = 90 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -12 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 3.9 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	50	70	m Ω
		$V_{GS} = 4.5 \text{ V}; I_D = 3.9 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	95	130	m Ω
		$V_{GS} = 2.5 \text{ V}; I_D = 2 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	62	80	m Ω
g_{fs}	forward transconductance	$V_{DS} = 5 \text{ V}; I_D = 3.9 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	11.9	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$	-	1.1	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 50 \text{ V}; I_D = 3.9 \text{ A}; V_{GS} = 4.5 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	6.7	-	nC
Q_{GS}	gate-source charge		-	1.2	-	nC
Q_{GD}	gate-drain charge		-	2.1	-	nC
C_{iss}	input capacitance	$V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	741.5	-	pF
C_{oss}	output capacitance		-	149.4	-	pF
C_{rss}	reverse transfer capacitance		-	5.9	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 50 \text{ V}; I_D = 3.9 \text{ A}; V_{GS} = 4.5 \text{ V}; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	4.3	-
t_r	rise time	-		4.3	-	ns
$t_{d(off)}$	turn-off delay time	-		13	-	ns
t_f	fall time	-		7.7	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 1.5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.75	1.2	V
t_{rr}	reverse recovery time	$I_S = 1.5 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 4.5 \text{ V}; V_{DS} = 50 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	36	-	ns
Q_r	recovered charge		-	12.8	-	nC

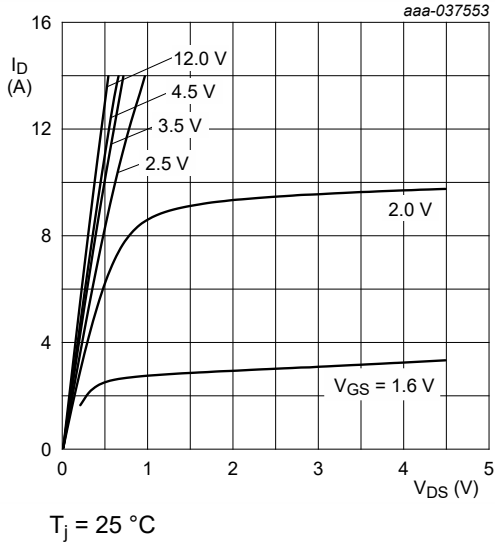


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

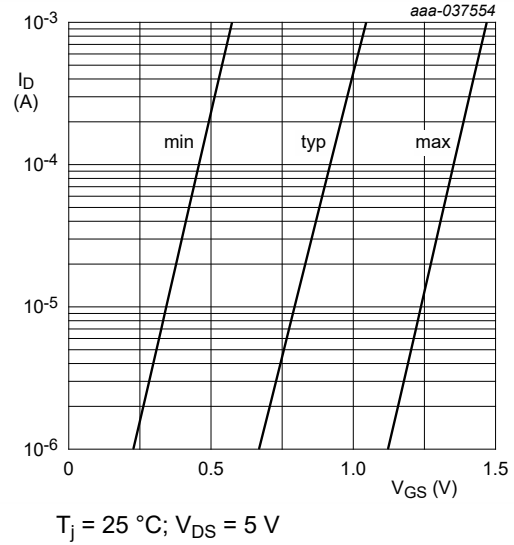


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

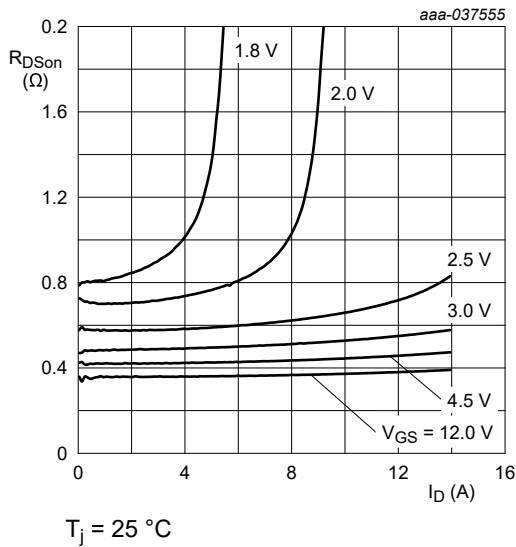


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

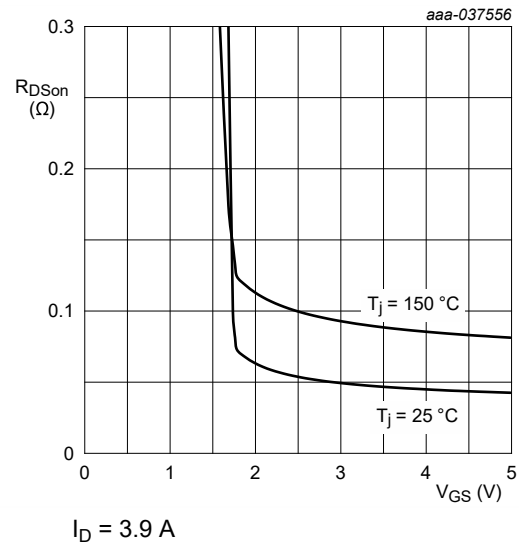


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

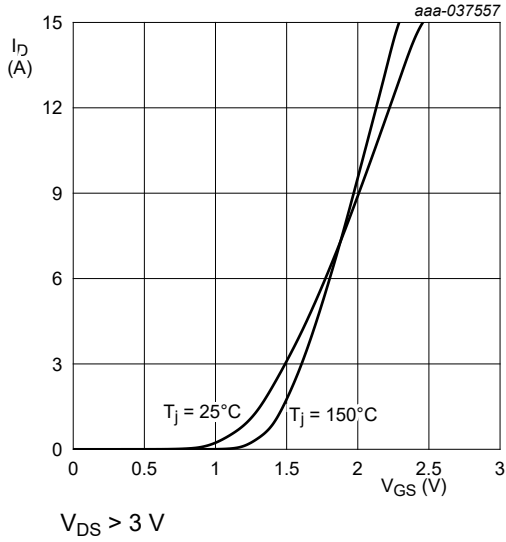
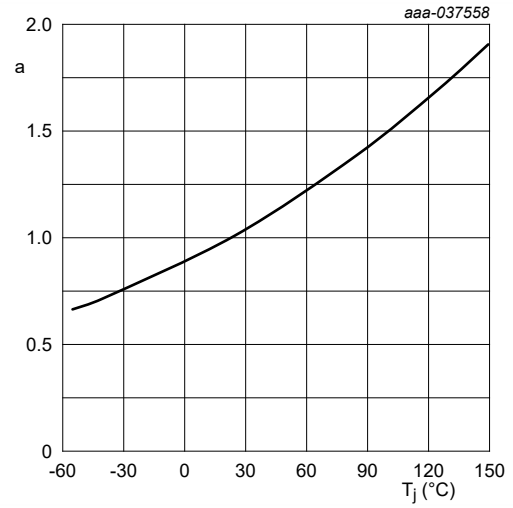


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}C)}$$

Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

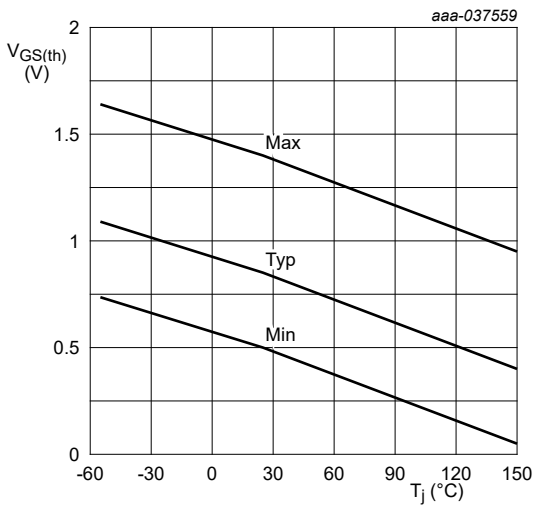


Fig. 12. Gate-source threshold voltage as a function of junction temperature

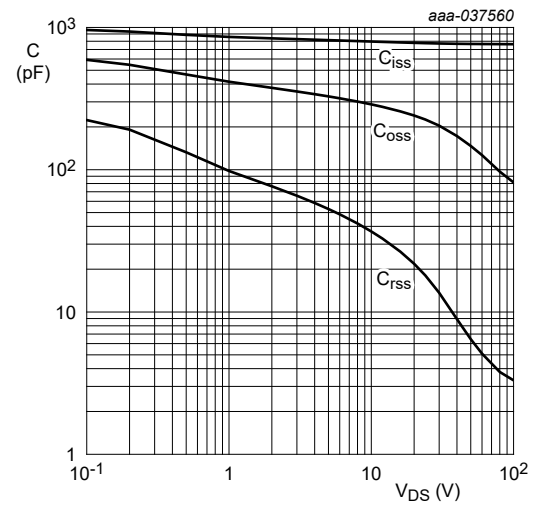
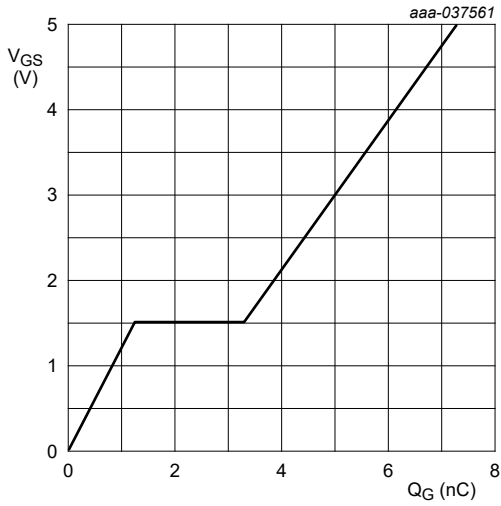


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = 50 \text{ V}; I_D = 3.9 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

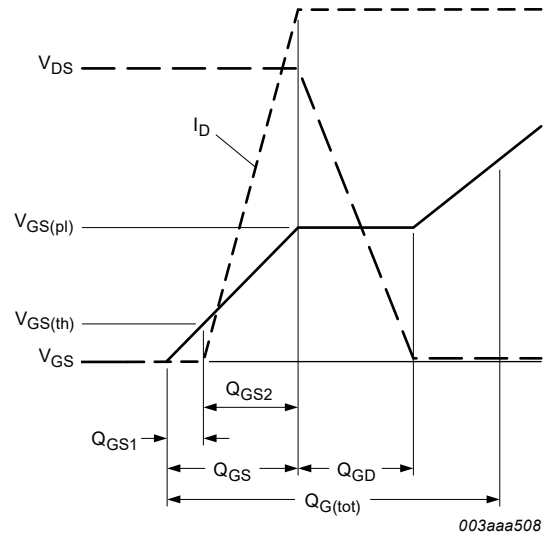
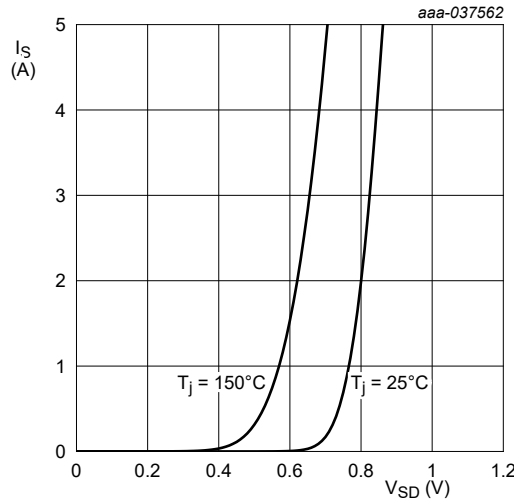


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

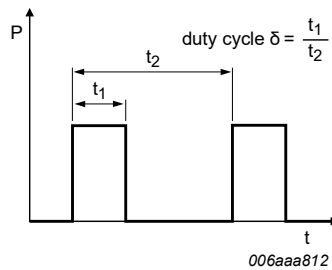
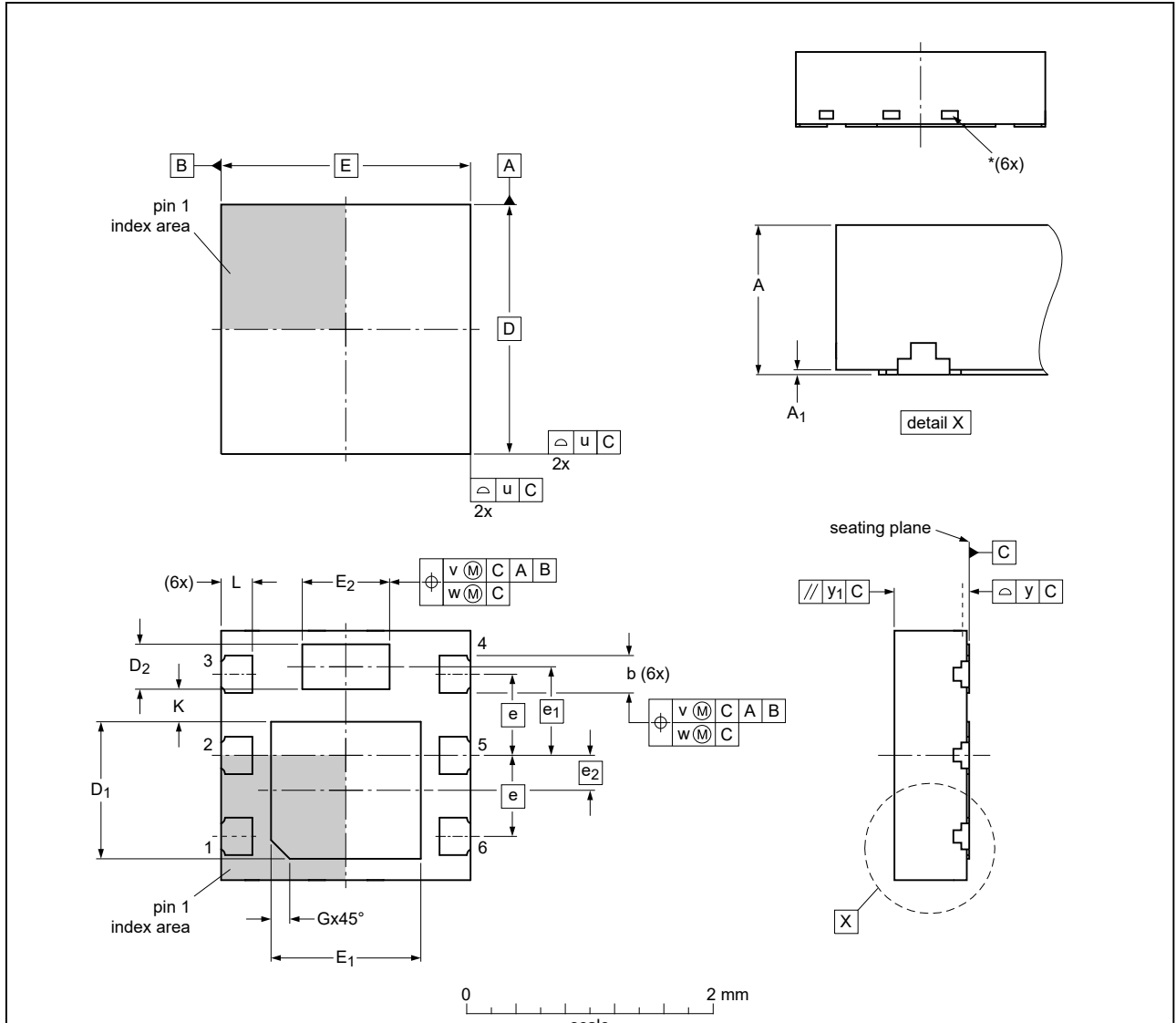


Fig. 17. Duty cycle definition

12. Package outline

DFN2020M-6: plastic thermal enhanced ultra thin small outline package; no leads;
6 terminals; body 2 x 2 x 0.65 mm

SOT1220-2



Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	D	D ₁	D ₂	E	E ₁	E ₂	e	e ₁	e ₂	G	K	L	u	v	w	y	y ₁	
min	0.55	0	0.25	1.0	0.31	1.1	0.6							0.2	0.20						
mm	nom	0.60	0.02	0.30	2	1.1	0.36	2	1.2	0.7	0.65	0.71	0.28	0.15 (ref)	0.25	0.05	0.1	0.05	0.05	0.05	
	max	0.65	0.04	0.35	1.2	0.41	1.3	0.8							0.30						

Note

1. Dimension A is including plating thickness.
2. * Visible depend upon used manufacturing technology.

sot1220-2_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1220-2		---				-20-03-31- 20-04-01

Fig. 18. Package outline DFN2020M-6 (SOT1220-2)

13. Soldering

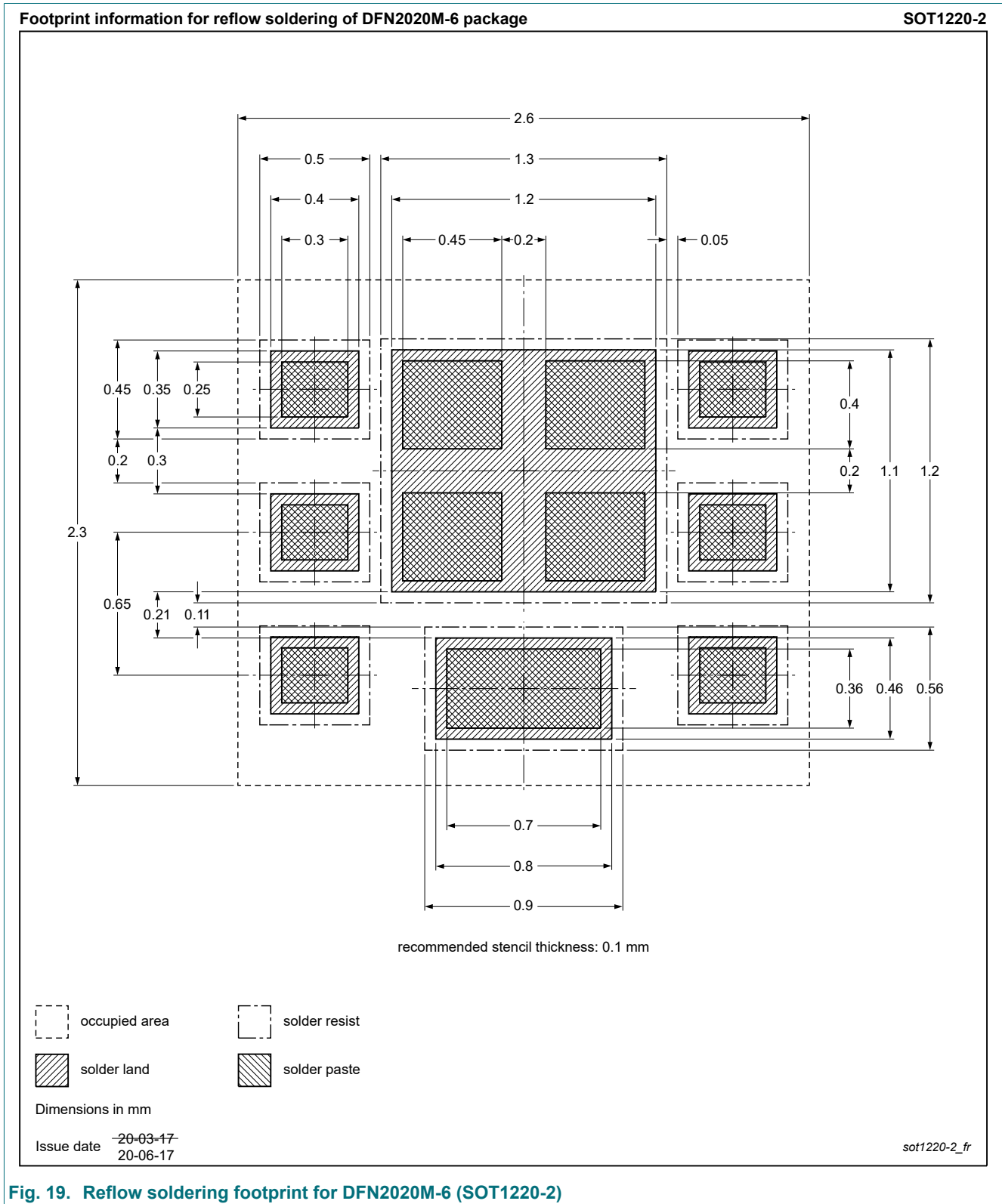


Fig. 19. Reflow soldering footprint for DFN2020M-6 (SOT1220-2)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB50XN v.1	20240516	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 16 May 2024
