



PIMN32PA

50 V, 500 mA NPN/NPN Resistor-Equipped double Transistor;
R1 = 2.2 k Ω , R2 = 10 k Ω

31 August 2023

Product data sheet

1. General description

NPN/NPN Resistor-Equipped double Transistor (RET) in a medium power SOT1118 (DFN2020-6) leadless Surface-Mounted Device (SMD) plastic package.

NPN/PNP complement: PIMC32PA

PNP/PNP complement: PIMP32PA

2. Features and benefits

- 500 mA output current capability
- Built-in resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

3. Applications

- Digital applications
- Cost-saving alternative to BC817 series in digital applications
- Control of IC inputs
- Switching loads

4. Quick reference data

Table 1. Quick reference data

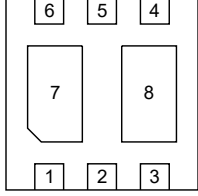
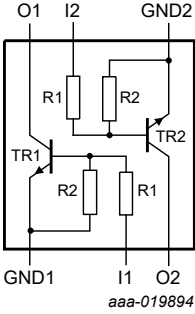
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V _{CEO}	collector-emitter voltage	open base		-	-	50	V
I _O	output current			-	-	500	mA
R1	bias resistor 1 (input)	T _{amb} = 25 °C	[1]	1.54	2.2	2.86	k Ω
R2/R1	bias resistor ratio		[1]	4.1	4.55	5	

[1] See section "Test information" for resistor calculation and test conditions.

50 V, 500 mA NPN/NPN Resistor-Equipped double Transistor; R1 = 2.2 k Ω , R2 = 10 k Ω

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1	 <p>Transparent top view DFN2020-6 (SOT1118)</p>	 <p>aaa-019894</p>
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2		
5	I2	input (base) TR2		
6	O1	output (collector) TR1		
7	O1	output (collector) TR1		
8	O2	output (collector) TR2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PIMN32PA	DFN2020-6	plastic, leadless thermal enhanced ultra thin small outline package; no leads; 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1118

7. Marking

Table 4. Marking codes

Type number	Marking code
PIMN32PA	8K

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	5	V
V _I	input voltage			-5	12	V
I _O	output current			-	500	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	360	mW
			[2]	-	550	mW
			[3]	-	510	mW
			[4]	-	730	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	500	mW
			[2]	-	750	mW
			[3]	-	700	mW
			[4]	-	1	W
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided, 35μm copper, tin-plated; mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated; mounting pad for collector 1 cm².

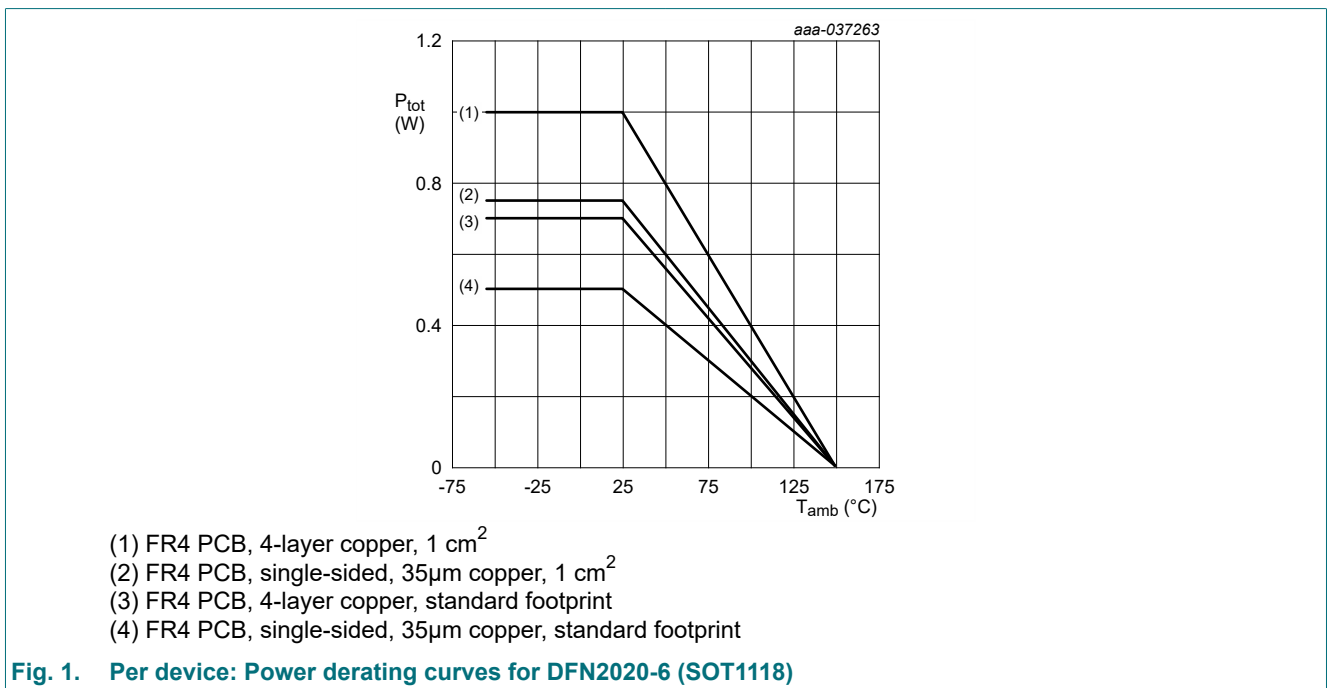


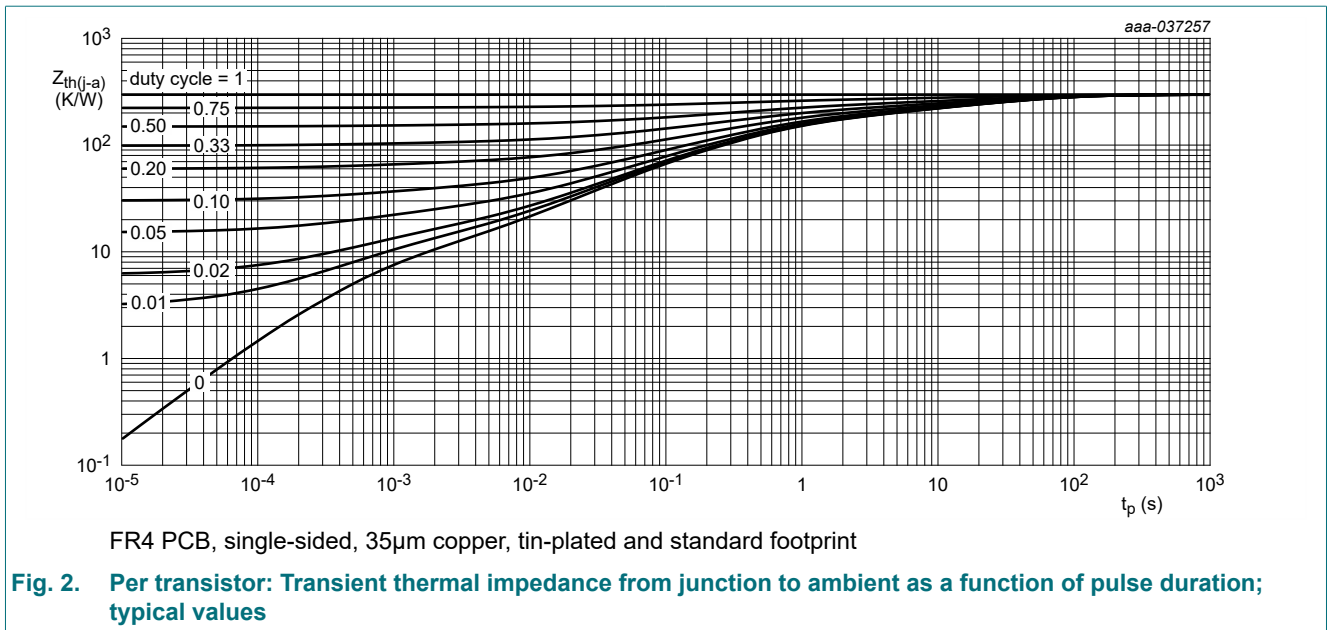
Fig. 1. Per device: Power derating curves for DFN2020-6 (SOT1118)

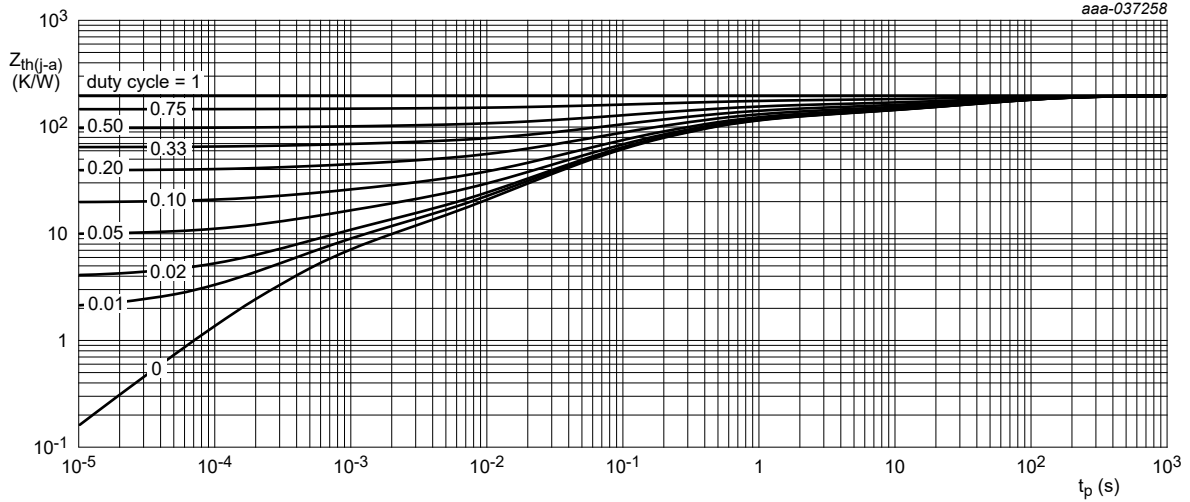
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	348	K/W
			[2]	-	-	228	K/W
			[3]	-	-	246	K/W
			[4]	-	-	172	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	250	K/W
			[2]	-	-	167	K/W
			[3]	-	-	179	K/W
			[4]	-	-	125	K/W

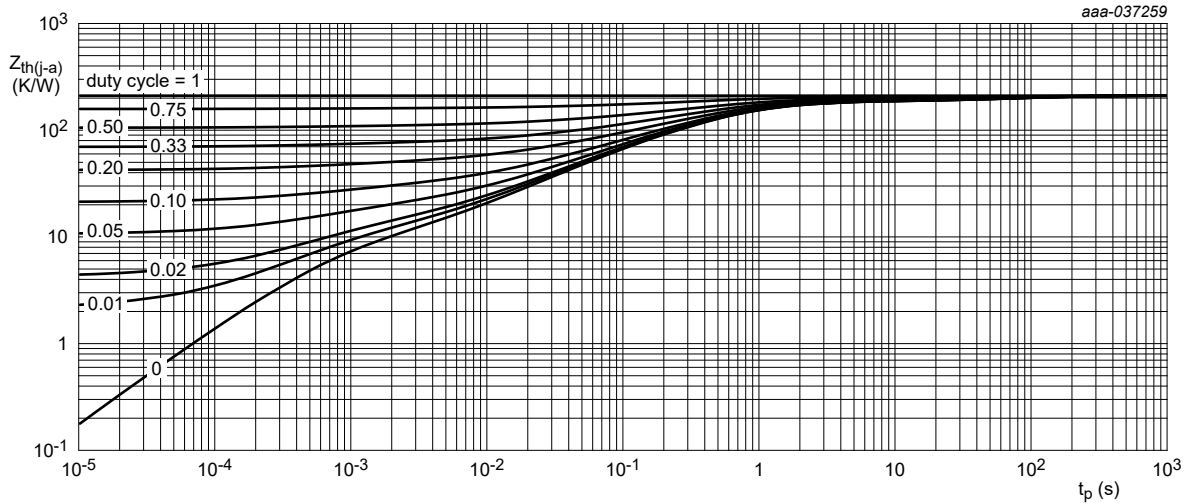
- [1] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided, 35 μm copper, tin-plated; mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.
- [4] Device mounted on an FR4 PCB, 4-layer copper, tin-plated; mounting pad for collector 1 cm².





FR4 PCB, single-sided, 35µm copper, tin-plated, mounting pad for collector 1 cm².

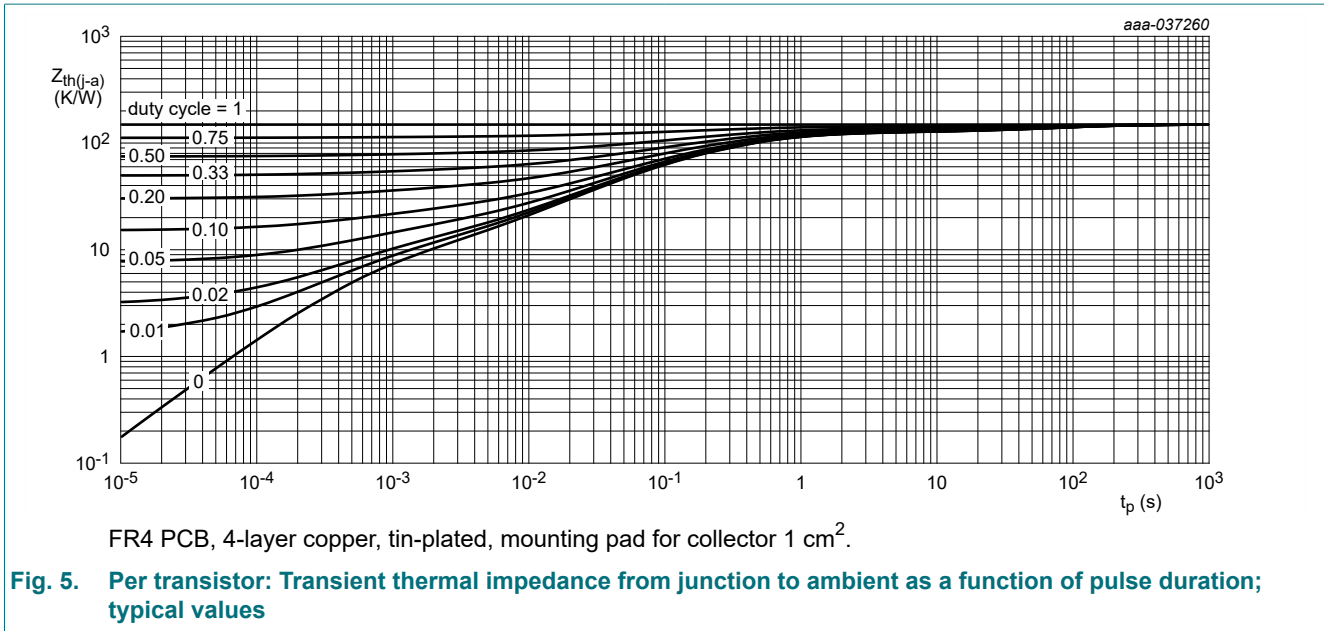
Fig. 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, 4-layer copper, tin-plated and standard footprint.

Fig. 4. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

50 V, 500 mA NPN/NPN Resistor-Equipped double Transistor; R1 = 2.2 kΩ, R2 = 10 kΩ

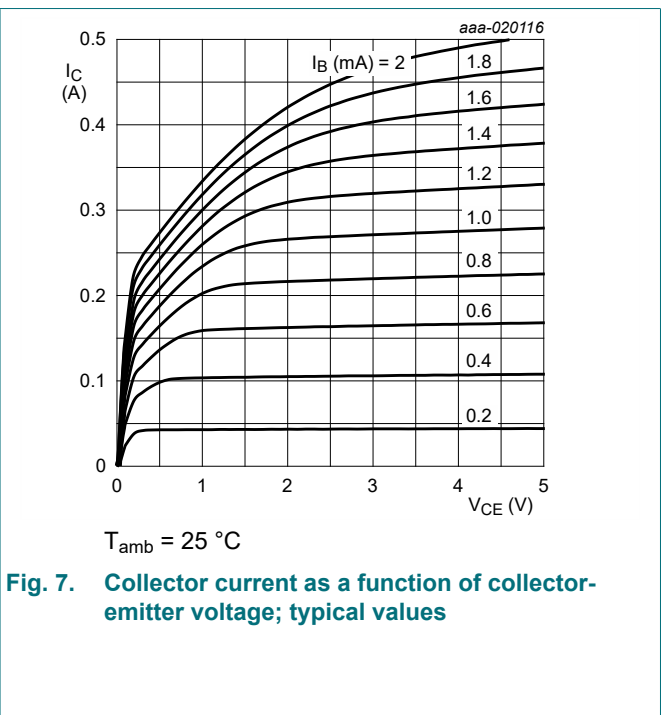
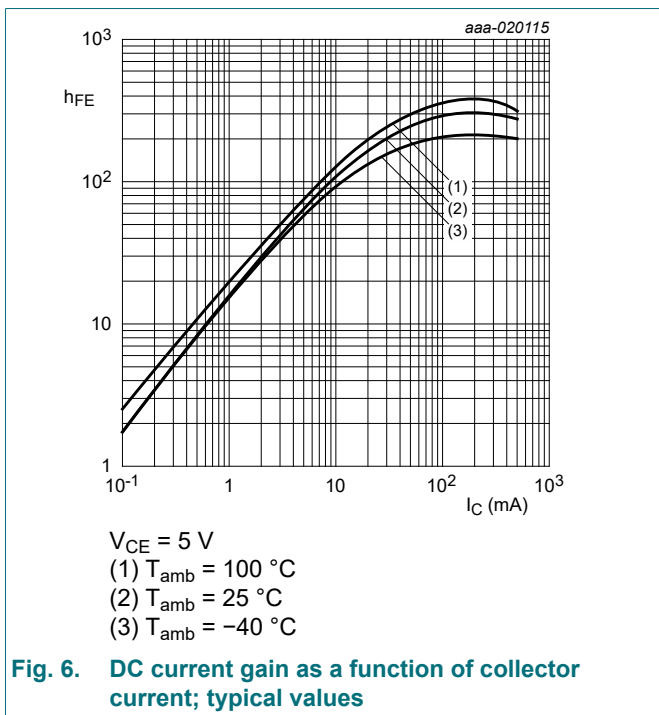


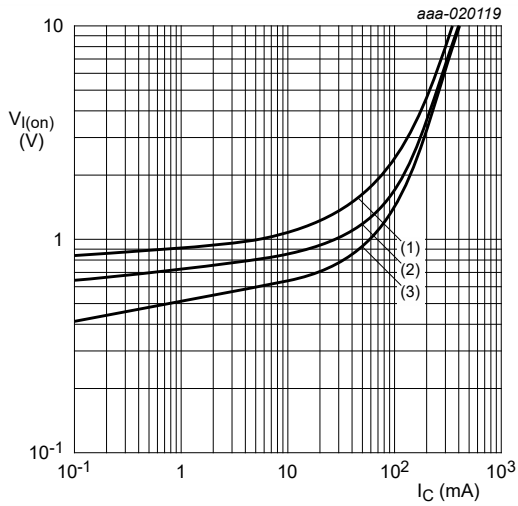
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Per transistor							
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100 \mu A; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$	50	-	-	V	
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 10 \text{ mA}; I_B = 0 A; T_{amb} = 25 \text{ }^\circ C$	50	-	-	V	
I_{CBO}	collector-base cut-off current	$V_{CB} = 50 \text{ V}; I_E = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	100	nA	
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 50 \text{ V}; I_B = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	0.5	μA	
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_C = 0 A; T_{amb} = 25 \text{ }^\circ C$	-	-	0.65	mA	
h_{FE}	DC current gain	$V_{CE} = 5 \text{ V}; I_C = 50 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	70	-	-		
V_{CEsat}	collector-emitter saturation voltage	$I_C = 50 \text{ mA}; I_B = 2.5 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	-	-	100	mV	
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5 \text{ V}; I_C = 100 \mu A; T_{amb} = 25 \text{ }^\circ C$	0.4	0.65	1	V	
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3 \text{ V}; I_C = 20 \text{ mA}; T_{amb} = 25 \text{ }^\circ C$	0.5	0.95	1.4	V	
R1	bias resistor 1 (input)	$T_{amb} = 25 \text{ }^\circ C$	[1]	1.54	2.2	2.86	kΩ
R2/R1	bias resistor ratio		[1]	4.1	4.55	5	
C_c	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 A; i_e = 0 A; f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ C$	-	5	-	pF	
f_T	transition frequency	$V_{CE} = 5 \text{ V}; I_C = 50 \text{ mA}; f = 100 \text{ MHz}; T_{amb} = 25 \text{ }^\circ C$	[2]	210	-	MHz	

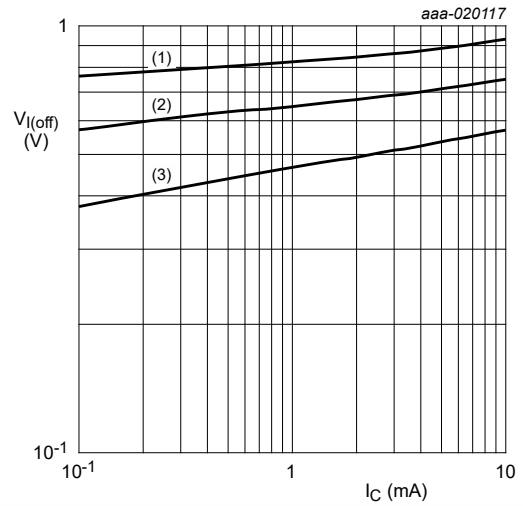
- [1] See section "Test information" for resistor calculation and test conditions.
- [2] Characteristics of built-in transistor.





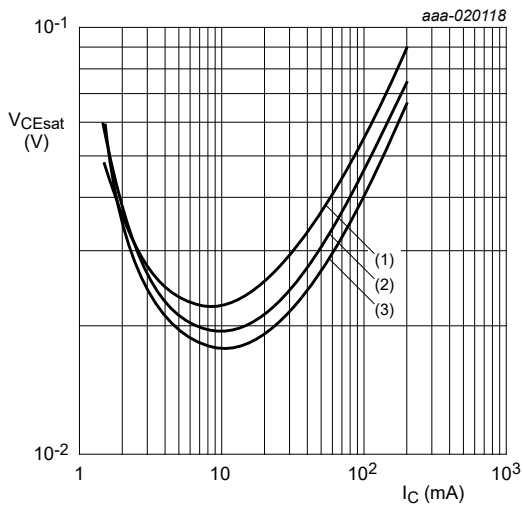
$V_{CE} = 0.3$ V
 (1) $T_{amb} = -40$ °C
 (2) $T_{amb} = 25$ °C
 (3) $T_{amb} = 100$ °C

Fig. 8. On-state input voltage as a function of collector current; typical values



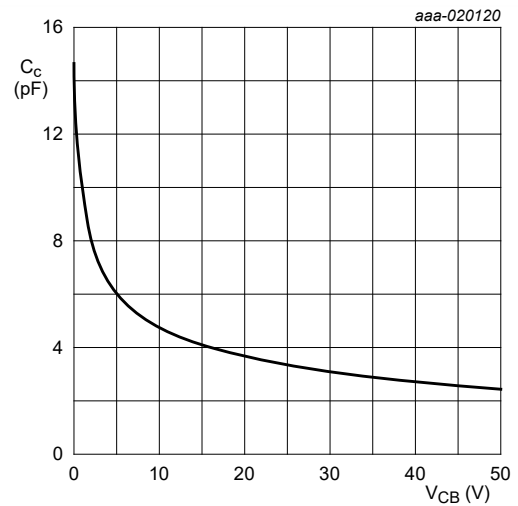
$V_{CE} = 5$ V
 (1) $T_{amb} = -40$ °C
 (2) $T_{amb} = 25$ °C
 (3) $T_{amb} = 100$ °C

Fig. 9. Off-state input voltage as a function of collector current; typical values



$I_C/I_B = 20$
 (1) $T_{amb} = 100$ °C
 (2) $T_{amb} = 25$ °C
 (3) $T_{amb} = -40$ °C

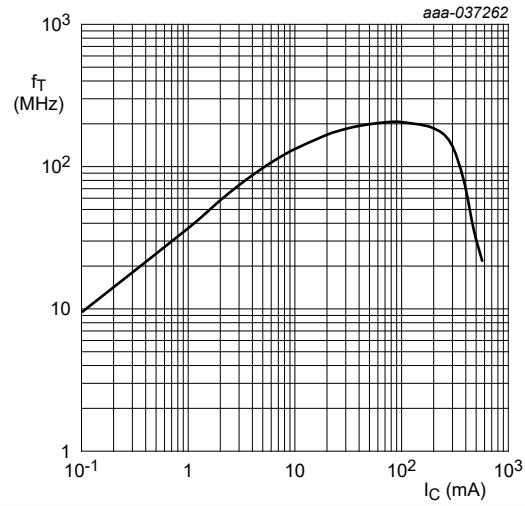
Fig. 10. Collector-emitter saturation voltage as a function of collector current; typical values



$f = 1$ MHz
 $T_{amb} = 25$ °C

Fig. 11. Collector capacitance as a function of collector-base voltage; typical values

50 V, 500 mA NPN/NPN Resistor-Equipped double Transistor; R1 = 2.2 kΩ, R2 = 10 kΩ



$f = 100 \text{ MHz}; V_{CE} = -5 \text{ V } T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 12. Transition frequency as a function of collector current; typical values of built-in transistor

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1):

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1):

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

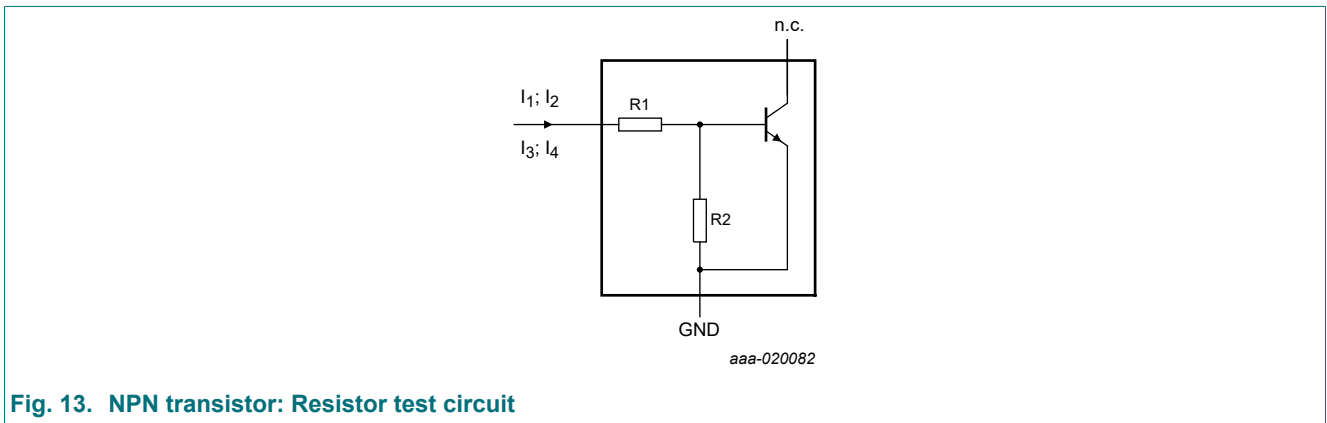


Fig. 13. NPN transistor: Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

PIMN32PA	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	I ₂	I ₃	I ₄
TR1/TR2 (NPN)	2.2	10	0.7 mA	0.8 mA	-0.45 mA	-0.55 mA

12. Package outline

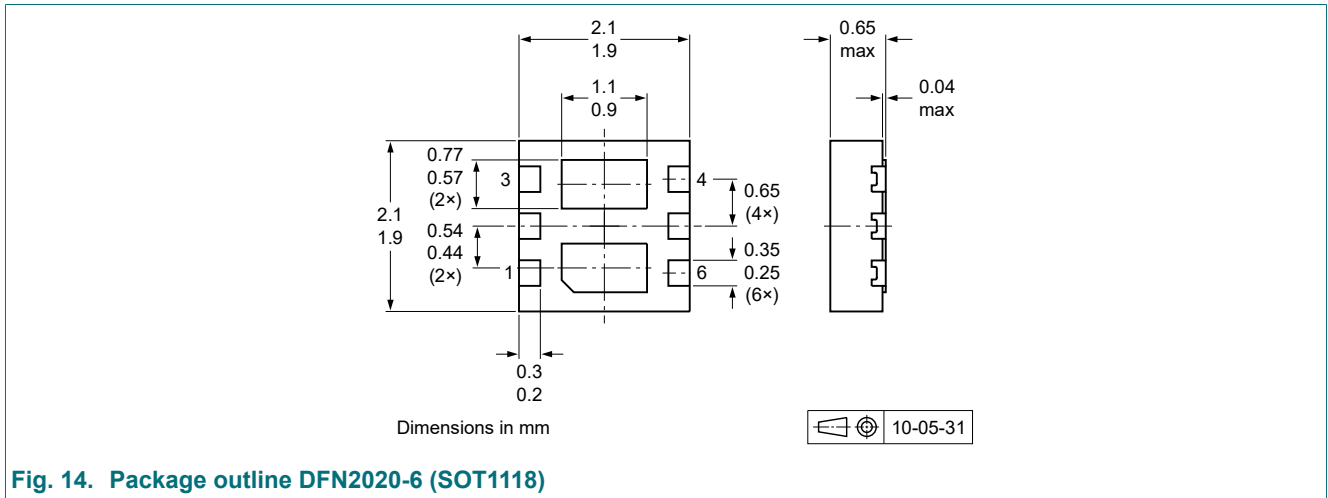


Fig. 14. Package outline DFN2020-6 (SOT1118)

13. Soldering

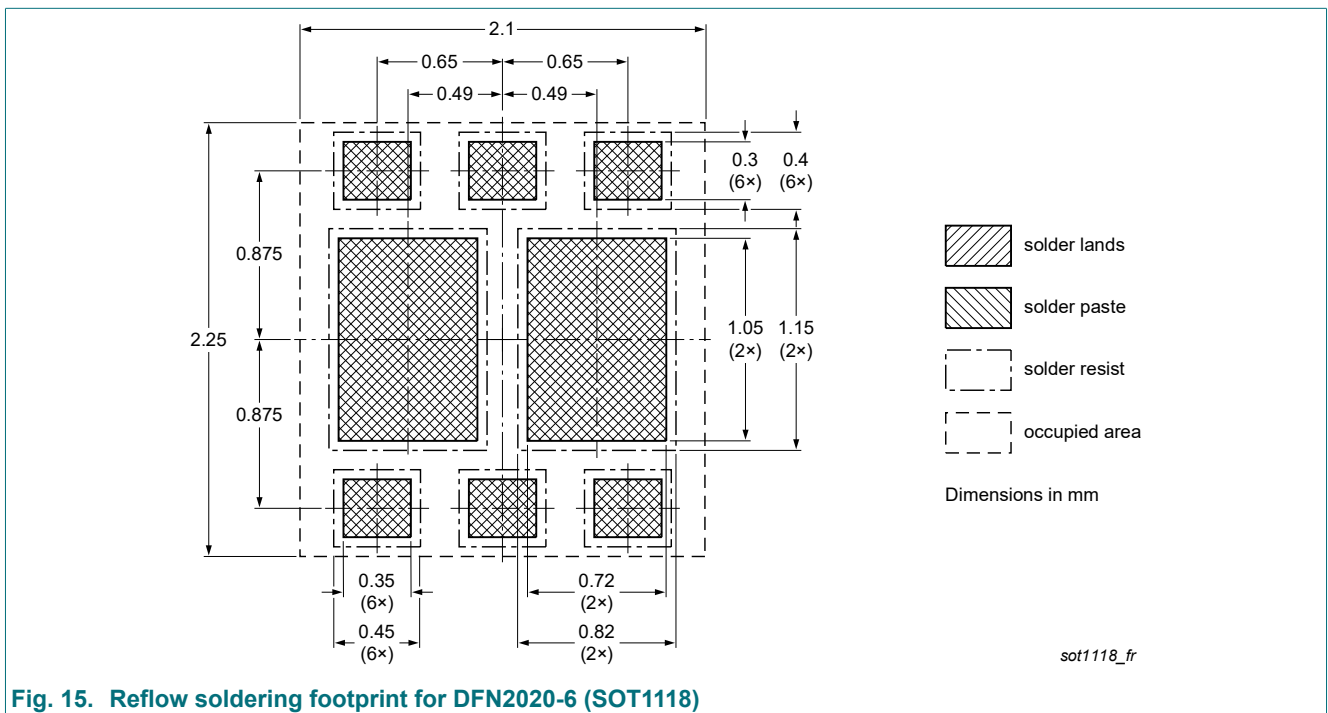


Fig. 15. Reflow soldering footprint for DFN2020-6 (SOT1118)

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PIMN32PA v.1	20230831	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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Contents

1. General description.....	1
2. Features and benefits.....	1
3. Applications.....	1
4. Quick reference data.....	1
5. Pinning information.....	2
6. Ordering information.....	2
7. Marking.....	2
8. Limiting values.....	3
9. Thermal characteristics.....	4
10. Characteristics.....	7
11. Test information.....	10
12. Package outline.....	11
13. Soldering.....	11
14. Revision history.....	12
15. Legal information.....	13

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