



PESD75VX1BLS-Q

ESD protection for in-vehicle networks

14 August 2024

Product data sheet

1. General description

ESD protection device in a leadless ultra small DFN1006BD-2 (SOD882BD) Surface-Mounted Device (SMD) plastic package with side-wettable flanks, designed to protect one single line from the damage caused by ElectroStatic Discharge (ESD) and other transients.

2. Features and benefits

- High reverse standoff voltage: $V_{RWM} = 75\text{ V}$
- High trigger voltage: $V_{t1} = 100\text{ V min}$
- Low capacitance: $C_d < 0.4\text{ pF}$
- ESD protection up to 18 kV (IEC 61000-4-2)
- ESD protection 1000 contact discharges up to 15 kV (IEC 61000-4-2)
- Qualified according to AEC-Q101 and recommended for use in automotive applications
- Single line protection suitable for VW80121-3 specification

3. Applications

ESD protection for in-vehicle network lines in automotive environments

- Automotive data lines such as automotive Ethernet
- LIN
- CAN/ CAN-FD/ CAN-XL and CAN-SIC
- FlexRay
- SENT

4. Quick reference data

Table 1. Quick reference data

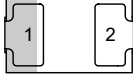
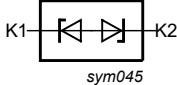
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ °C}$	-	-	75	V	
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ °C}$	0.3	0.35	0.4	pF	
V_{ESD}	electrostatic discharge voltage	ISO 10605; contact discharge; $C = 150\text{ pF}; R = 330\text{ }\Omega$	[1] [2]	18	-	-	kV
		IEC 61000-4-2; contact discharge	[1] [2]	18	-	-	kV
		1000 contact discharges (IEC 61000-4-2); OPEN Alliance specification	[2]	15	-	-	kV

[1] Device stressed with ten non-repetitive ESD pulses.

[2] Measured from pin 1 to pin 2.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	 <p>Transparent top view</p> <p>DFN1006BD-2 (SOD882BD)</p>	 <p>sym045</p>
2	K2	cathode (diode 2)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD75VX1BLS-Q	DFN1006BD-2	Leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.47 mm body	SOD882BD

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD75VX1BLS-Q	HHH

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC60134)

Symbol	Parameter	Conditions		Min	Max	Unit
I_{PPM}	rated peak pulse current	$t_p = 8/20 \mu s$	[1]	-	2.3	A
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-55	150	°C
T_{stg}	storage temperature			-65	150	°C
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[2] [3]	18	-	kV
		ISO 10605; contact discharge; C = 150 pF; R = 330 Ω	[2] [3]	18	-	kV
		1000 contact discharges (IEC 61000-4-2); OPEN Alliance specification	[3]	15	-	kV

[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Device stressed with ten non-repetitive ESD pulses.

[3] Measured from pin 1 to pin 2.

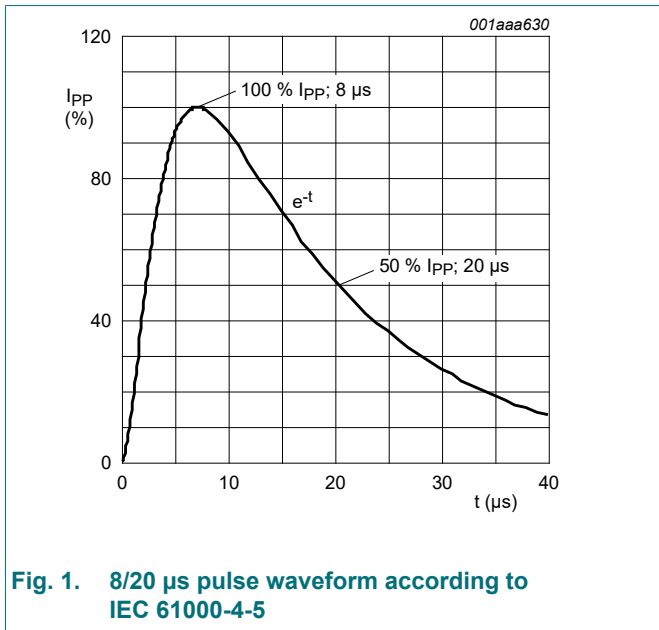


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

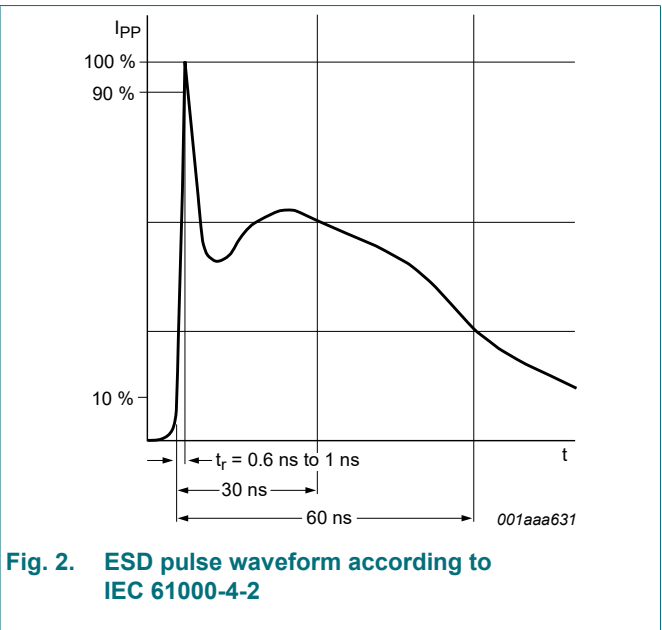


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25\text{ °C}$	-	-	75	V
V_{BR}	breakdown voltage	$I_R = 1\text{ mA}; T_{amb} = 25\text{ °C}$	120	125	130	V
I_{RM}	reverse leakage current	$V_{RWM} = 75\text{ V}; T_{amb} = 25\text{ °C}$	-	1	100	nA
C_d	diode capacitance	$f = 1\text{ MHz}; V_R = 0\text{ V}; T_{amb} = 25\text{ °C}$	0.3	0.35	0.4	pF
V_{CL}	clamping voltage	$I_{PPM} = 2.3\text{ A}; t_p = 8/20\text{ }\mu\text{s}; T_{amb} = 25\text{ °C}$ [1]	-	41	-	V
		$I_{PP} = 16\text{ A}; t_p = 100\text{ ns}; T_{amb} = 25\text{ °C}$ [2]	-	50	-	V
R_{dyn}	dynamic resistance	$I_R = 20\text{ A}; t_p = 100\text{ ns}; T_{amb} = 25\text{ °C}$ [2]	-	1	-	Ω

[1] Device stressed with 8/20 μs exponential decay waveform according to IEC 61000-4-5.

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008.

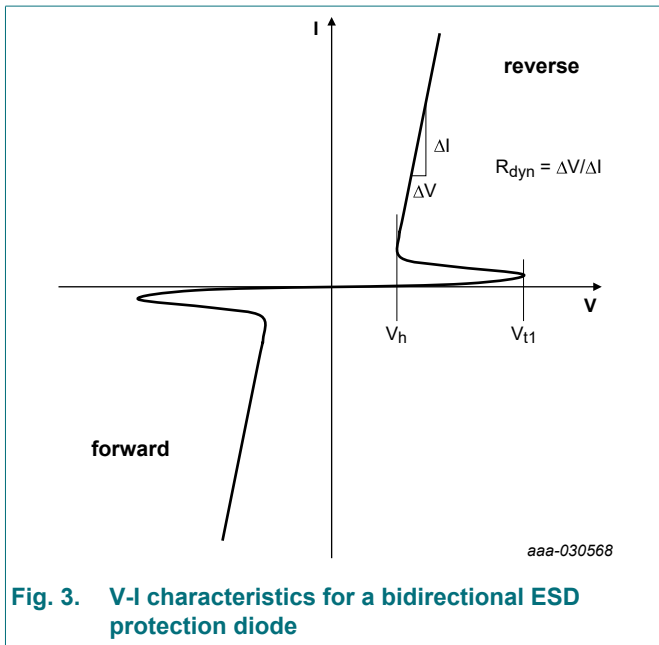


Fig. 3. V-I characteristics for a bidirectional ESD protection diode

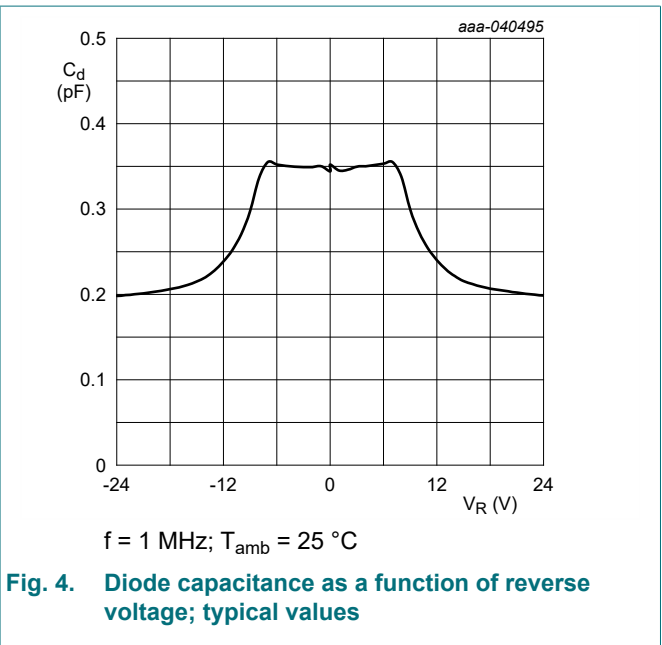
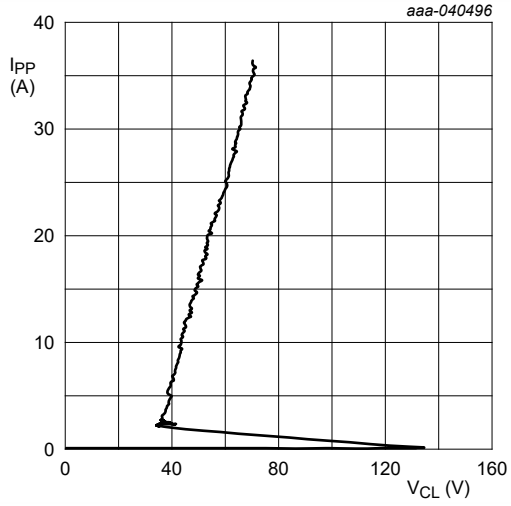
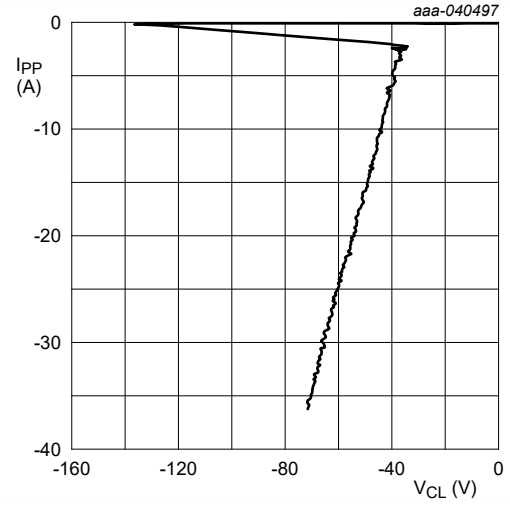


Fig. 4. Diode capacitance as a function of reverse voltage; typical values



Transmission Line Pulse (TLP);
 $t_p = 100 \text{ ns}$; $t_r = 1 \text{ ns}$

Fig. 5. Dynamic resistance with positive clamping; typical values



Transmission Line Pulse (TLP);
 $t_p = 100 \text{ ns}$; $t_r = 1 \text{ ns}$

Fig. 6. Dynamic resistance with negative clamping; typical values

10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

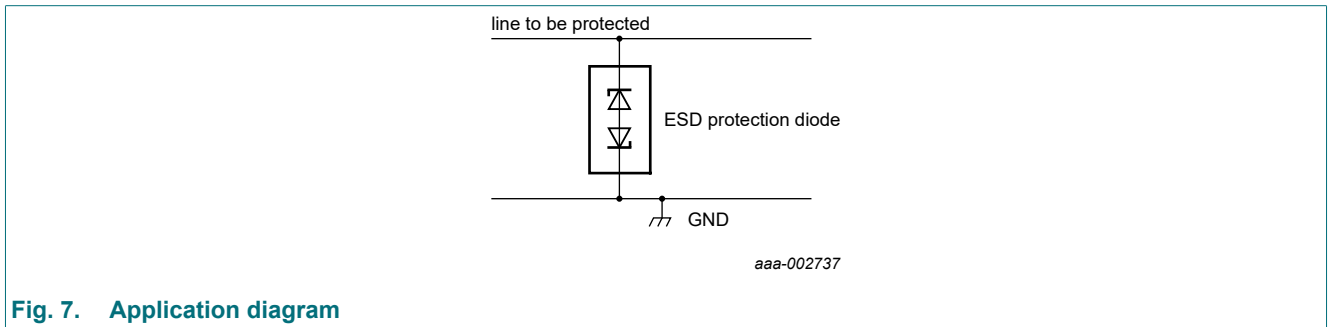


Fig. 7. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

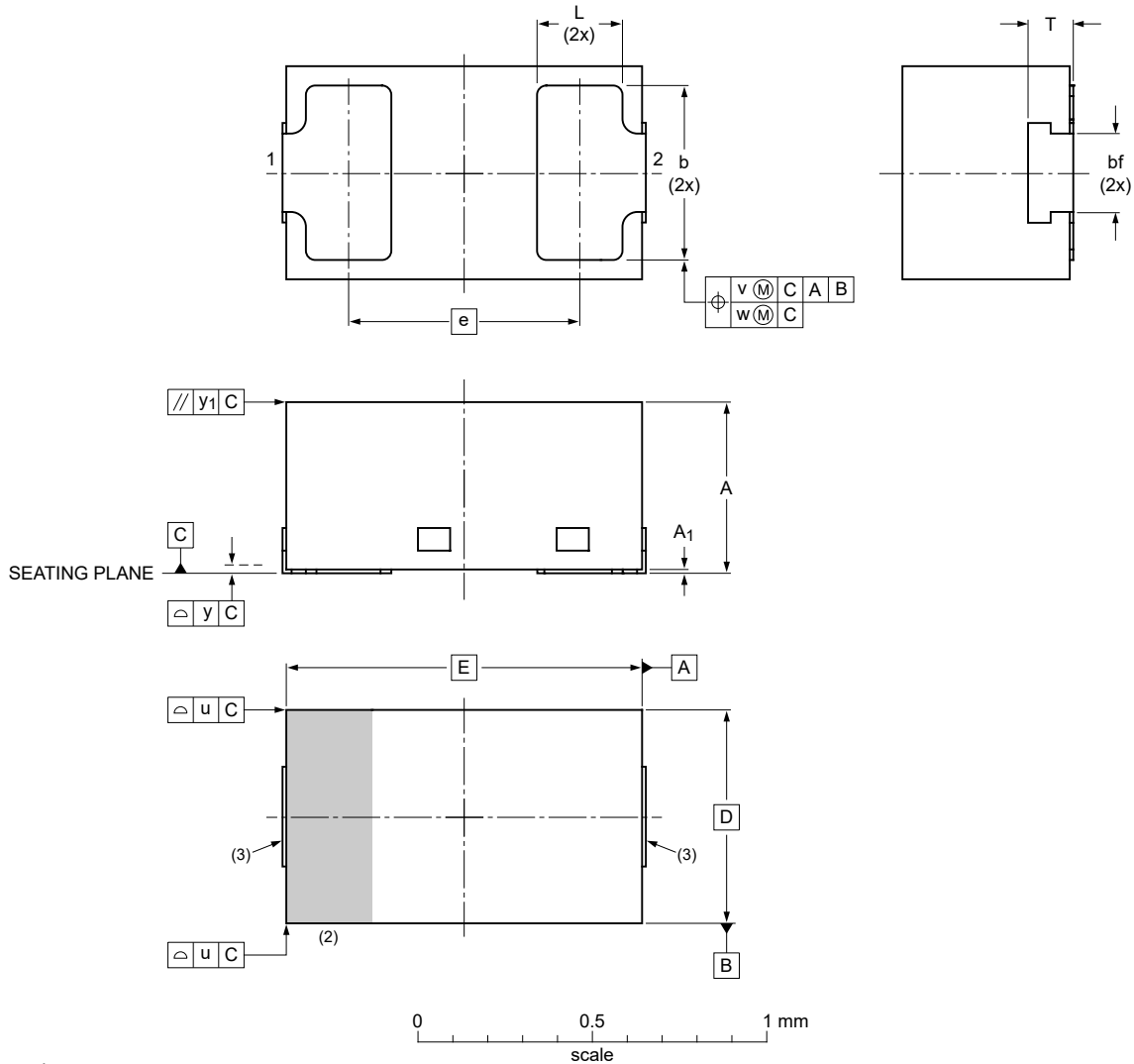
Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

DFN1006BD-2 Leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals;
0.65 mm pitch; 1 mm x 0.6 mm x 0.47 mm body

SOD882BD



Dimensions

Unit	A ⁽¹⁾	A ₁	bf ⁽¹⁾	b	D	E	e	L	T ⁽¹⁾	u	v	w	y	y ₁
mm	max 0.50	0.04		0.55	0.60	1.00	0.65	0.30	0.22	0.05	0.10	0.05	0.05	0.05
	nom 0.47			0.50	0.60	1.00	0.65	0.25	0.16	0.05	0.10	0.05	0.05	0.05
	min 0.44		0.20	0.45				0.22	0.10					

Note

1. Dimension including plating thickness.
2. The marking bar indicates the cathode.
3. Solderable lead end, protrusion max. 0.02 mm.

sod882bd_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOD882BD		MO-343AA			20-06-22 20-06-23

Fig. 8. Package outline DFN1006BD-2 (SOD882BD)

13. Soldering

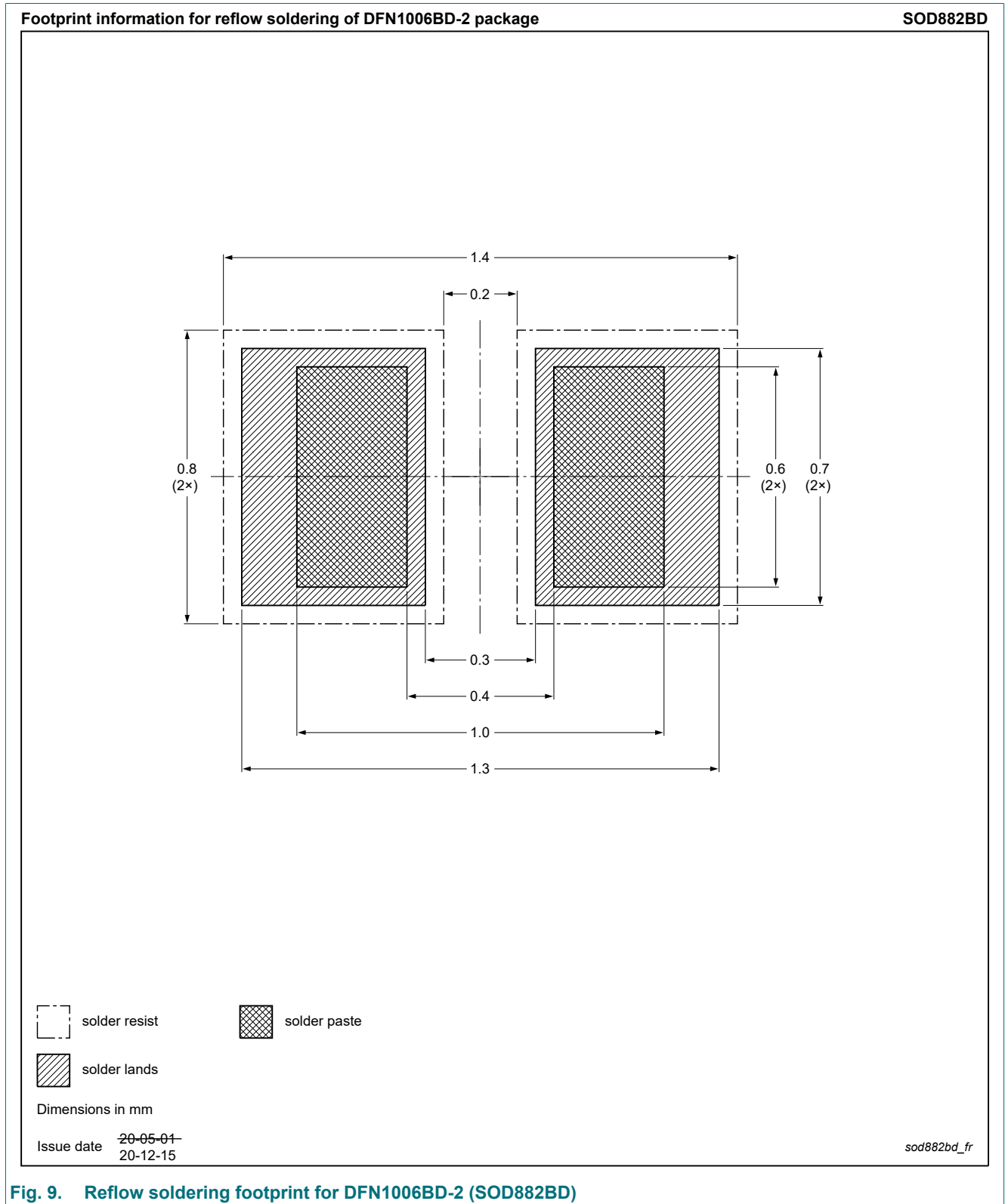


Fig. 9. Reflow soldering footprint for DFN1006BD-2 (SOD882BD)

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD75VX1BLS-Q v.1	20240814	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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