1. General description

Ultra low capacitance unidirectional ElectroStatic Discharge (ESD) protection diode designed to protect one signal line from the damage caused by ESD and other transients.

The device is housed in a SOD882D leadless ultra small Surface-Mounted Device (SMD) plastic package with visible and solderable side pads.

The combination of extremely low capacitance and ultra low clamping voltage makes the device ideal for high-speed data line protection applications.

2. Features and benefits

- ESD protection of one line
- Ultra low diode capacitance $C_d = 0.95 \text{ pF}$
- Ultra low clamping voltage: $V_{CL} = 8 \text{ V}$
- Ultra low leakage current: $I_{RM} = 1 \text{ nA}$
- ESD protection up to $8 \text{ kV}$
- IEC 61000-4-2; level 4 (ESD)
- Ultra small SMD plastic package
- Solderable tin-plated side pads
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- 10/100/1000 Mbit/s Ethernet
- Communication systems
- Portable electronics
- SIM card protection
- USB, High-Definition Multimedia Interface (HDMI), FireWire
- High-speed data lines

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{RWM}$</td>
<td>reverse standoff voltage</td>
<td>$T_{amb} = 25 \degree \text{C}$</td>
<td>-</td>
<td>-</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>$C_d$</td>
<td>diode capacitance</td>
<td>$f = 1 \text{MHz}; V_R = 0 \text{V}; T_{amb} = 25 \degree \text{C}$</td>
<td>-</td>
<td>0.95</td>
<td>1.1</td>
<td>pF</td>
</tr>
</tbody>
</table>
5. Pinning information

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>K</td>
<td>cathode[1]</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>A</td>
<td>anode</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>


6. Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PESD5V0X1ULD-Q</td>
<td>DFN1006D-2</td>
<td>leadless ultra small plastic package with side-wettable flanks (SWF); 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.4 mm body</td>
<td>SOD882D</td>
</tr>
</tbody>
</table>

7. Marking

Table 4. Marking codes

<table>
<thead>
<tr>
<th>Type number</th>
<th>Marking code</th>
</tr>
</thead>
<tbody>
<tr>
<td>PESD5V0X1ULD-Q</td>
<td>1111 0000</td>
</tr>
</tbody>
</table>

Fig. 1. SOD882D binary marking code description
8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{PPM}</td>
<td>rated peak pulse current</td>
<td>( t_p = 8/20 , \mu\text{s} )</td>
<td>-1.5</td>
<td>1.5</td>
<td>A</td>
</tr>
<tr>
<td>( T_j )</td>
<td>junction temperature</td>
<td></td>
<td>-</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{amb} )</td>
<td>ambient temperature</td>
<td></td>
<td>-55</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>( T_{stg} )</td>
<td>storage temperature</td>
<td></td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

**ESD maximum ratings**

<table>
<thead>
<tr>
<th>( V_{ESD} )</th>
<th>electrostatic discharge voltage</th>
<th>IEC 61000-4-2 (contact discharge); ( T_{amb} = 25 , ^\circ\text{C} )</th>
<th>[3]</th>
<th>8</th>
<th>kV</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>IEC 61000-4-2 (air discharge)</td>
<td>[2]</td>
<td>15</td>
<td>kV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>machine model; ( T_{amb} = 25 , ^\circ\text{C} )</td>
<td>[2]</td>
<td>400</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MIL-STD-883 (human body model); ( T_{amb} = 25 , ^\circ\text{C} )</td>
<td>[2]</td>
<td>10</td>
<td>kV</td>
</tr>
</tbody>
</table>

[1] Non-repetitive current pulse 8/20 \( \mu\text{s} \) exponentially decay waveform according to IEC 61000-4-5.


---

![Fig. 2. 8/20 \( \mu\text{s} \) pulse waveform according to IEC 61000-4-5](image1)

![Fig. 3. ESD pulse waveform according to IEC 61000-4-2](image2)
9. Characteristics

Table 6. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{RWM}</td>
<td>reverse standoff voltage</td>
<td>T_{amb} = 25 °C</td>
<td>-</td>
<td>-</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>V_{BR}</td>
<td>breakdown voltage</td>
<td>I_R = 10 mA; T_{amb} = 25 °C</td>
<td>5.8</td>
<td>7.5</td>
<td>10</td>
<td>V</td>
</tr>
<tr>
<td>I_{RM}</td>
<td>reverse leakage current</td>
<td>V_{RWM} = 5 V; T_{amb} = 25 °C</td>
<td>-</td>
<td>1</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>C_d</td>
<td>diode capacitance</td>
<td>f = 1 MHz; V_R = 0 V; T_{amb} = 25 °C</td>
<td>-</td>
<td>0.95</td>
<td>1.1</td>
<td>pF</td>
</tr>
<tr>
<td>V_{CL}</td>
<td>clamping voltage</td>
<td>I_{PPM} = 1.5 A; T_{amb} = 25 °C</td>
<td>[1] [2]</td>
<td>8</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>R_{dyn}</td>
<td>dynamic resistance</td>
<td>I_R = 10 A; T_{amb} = 25 °C</td>
<td>[3]</td>
<td>0.25</td>
<td>-</td>
<td>Ω</td>
</tr>
</tbody>
</table>

[1] Non-repetitive current pulse 8/20 µs exponentially decay waveform according to IEC 61000-4-5.
[3] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI / ESD STM5.5.1-2008.

Fig. 4. Diode capacitance as a function of reverse voltage; typical values

Fig. 5. V-I characteristics for a unidirectional ESD protection diode
Fig. 6. ESD clamping test setup and waveforms
10. Application information

The device is designed for protection of one unidirectional data or signal line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are either positive or negative with respect to ground.

![Application Diagram](aaa-002440)

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.
# 12. Package outline

DFN1006D-2: Leadless ultra small plastic package; 2 terminals; body 1 x 0.6 x 0.4 mm  

![DFN1006D-2 Package Diagram](image)

### Dimensions

<table>
<thead>
<tr>
<th>Unit</th>
<th>A(1)</th>
<th>A1</th>
<th>b</th>
<th>D</th>
<th>E</th>
<th>e</th>
<th>L1</th>
<th>w</th>
<th>y</th>
</tr>
</thead>
<tbody>
<tr>
<td>max</td>
<td>0.4</td>
<td>0.04</td>
<td>0.55</td>
<td>0.65</td>
<td>1.05</td>
<td>0.30</td>
<td>0.1</td>
<td>0.03</td>
<td></td>
</tr>
<tr>
<td>nom</td>
<td>0.50</td>
<td>0.60</td>
<td>1.00</td>
<td>0.65</td>
<td>0.25</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>min</td>
<td>0.45</td>
<td>0.55</td>
<td>0.95</td>
<td>0.22</td>
<td></td>
<td></td>
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**Note:**
1. Dimension including plating thickness.
2. The marking bar indicates the cathode (if applicable).

### References

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<tr>
<th>Outline version</th>
<th>IEC</th>
<th>JEDEC</th>
<th>JEITA</th>
<th>European projection</th>
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**Fig. 8.** Package outline DFN1006D-2 (SOD882D)
13. Soldering

Fig. 9. Reflow soldering footprint for DFN1006D-2 (SOD882D)
## 14. Revision history

Table 7. Revision history

<table>
<thead>
<tr>
<th>Data sheet ID</th>
<th>Release date</th>
<th>Data sheet status</th>
<th>Change notice</th>
<th>Supersedes</th>
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<tr>
<td>PESD5V0X1ULD-Q v.1</td>
<td>20220823</td>
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15. Legal information

Data sheet status

<table>
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<th>Document status</th>
<th>Product status</th>
<th>Definition</th>
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Date of release: 23 August 2022

Product data sheet 23 August 2022
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