1. General description

Ultra low capacitance bidirectional double ElectroStatic Discharge (ESD) protection array designed to protect up to two signal lines from the damage caused by ESD and other transients. The device is housed in a leadless ultra small SOT883B (DFN1006B-3) Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- ESD protection of up to two lines
- Ultra low diode capacitance: \( C_d = 2.9 \) pF
- Ultra low leakage current: \( I_{RM} = 5 \) nA
- AEC-Q101 qualified
- ESD protection up to 10 kV
- IEC 61000-4-2; level 4 (ESD)

3. Applications

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Communication systems
- Portable electronics
- SIM card protection
- High-speed data lines

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{RWM} )</td>
<td>reverse standoff voltage</td>
<td>( T_{amb} = 25 ) °C</td>
<td>-</td>
<td>-</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>( C_d )</td>
<td>diode capacitance</td>
<td>( f = 1 ) MHz; ( V_R = 0 ) V; ( T_{amb} = 25 ) °C</td>
<td>-</td>
<td>2.9</td>
<td>3.5</td>
<td>pF</td>
</tr>
</tbody>
</table>
5. Pinning information

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>K1</td>
<td>cathode (diode 1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>K2</td>
<td>cathode (diode 2)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>CC</td>
<td>common cathode</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

6. Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Name</th>
<th>Description</th>
<th>Version</th>
</tr>
</thead>
<tbody>
<tr>
<td>PESD5V0U2BMB</td>
<td>DFN1006B-3</td>
<td>plastic, leadless ultra small plastic package; 3 solder lands; 0.35 mm pitch; 1.0 mm x 0.6 mm x 0.37 mm body</td>
<td>SOT883B</td>
<td></td>
</tr>
</tbody>
</table>

7. Marking

Table 4. Marking codes

<table>
<thead>
<tr>
<th>Type number</th>
<th>Marking code</th>
</tr>
</thead>
<tbody>
<tr>
<td>PESD5V0U2BMB</td>
<td>0001 1010</td>
</tr>
</tbody>
</table>

Fig. 1. DFN1006B-3 (SOT883B) binary marking code description
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{PPM}</td>
<td>rated peak pulse current</td>
<td>( t_p = 8/20 , \mu s )</td>
<td>-</td>
<td>1.5</td>
<td>A</td>
</tr>
<tr>
<td>( T_j )</td>
<td>junction temperature</td>
<td>-</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>( T_{amb} )</td>
<td>ambient temperature</td>
<td>-55</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>( T_{stg} )</td>
<td>storage temperature</td>
<td>-65</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
</tbody>
</table>

**ESD maximum ratings**

- \( V_{ESD} \) electrostatic discharge voltage
  - IEC 61000-4-2 (contact discharge) [3] [2] - 10 kV
  - machine model [2] - 400 V

[1] Device stressed with ten non-repetitive current pulses (8/20 µs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321).
[2] Measured from pin 1 or 2 to pin 3.

Fig. 2. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

Fig. 3. ESD pulse waveform according to IEC 61000-4-2
9. Characteristics

Table 6. Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_{RWM}</td>
<td>reverse standoff voltage</td>
<td>T_{amb} = 25 °C</td>
<td>-</td>
<td>-</td>
<td>5</td>
<td>V</td>
</tr>
<tr>
<td>V_{BR}</td>
<td>breakdown voltage</td>
<td>I_{R} = 5 mA; T_{amb} = 25 °C</td>
<td>5.5</td>
<td>6.5</td>
<td>9.5</td>
<td>V</td>
</tr>
<tr>
<td>I_{RM}</td>
<td>reverse leakage current</td>
<td>V_{RWM} = 5 V; T_{amb} = 25 °C</td>
<td>-</td>
<td>5</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>C_{d}</td>
<td>diode capacitance</td>
<td>f = 1 MHz; V_{R} = 0 V; T_{amb} = 25 °C</td>
<td>-</td>
<td>2.9</td>
<td>3.5</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>f = 1 MHz; V_{R} = 5 V; T_{amb} = 25 °C</td>
<td>-</td>
<td>1.9</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>V_{CL}</td>
<td>clamping voltage</td>
<td>I_{PP} = 1 A; T_{amb} = 25 °C</td>
<td>[1]</td>
<td>[2]</td>
<td>-</td>
<td>10 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>I_{PPM} = 1.5 A; T_{amb} = 25 °C</td>
<td>[1]</td>
<td>[2]</td>
<td>-</td>
<td>12 V</td>
</tr>
<tr>
<td>R_{dyn}</td>
<td>dynamic resistance</td>
<td>I_{R} = 10 A; T_{amb} = 25 °C</td>
<td>[3]</td>
<td>-</td>
<td>0.6</td>
<td>Ω</td>
</tr>
</tbody>
</table>

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5 and IEC 61643-321.
[2] Measured from pin 1 or 2 to pin 3.
[3] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI / ESD STM5.5.1-2008.

Fig. 4. Diode capacitance as a function of reverse voltage; typical values

Fig. 5. V-I characteristics for a bidirectional ESD protection diode
Fig. 6. ESD clamping test setup and waveforms
10. Application information

The device is designed for protection of up to two bidirectional data or signal lines from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both, positive and negative, with respect to ground.

![Application diagram](image-url)

**Fig. 7. Application diagram**

**Circuit board layout and protection device placement**

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

**Quality information**

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.
12. Package outline

Fig. 8. Package outline DFN1006B-3 (SOT883B)

13. Soldering

Fig. 9. Reflow soldering footprint for DFN1006B-3 (SOT883B)
# 14. Revision history

<table>
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<th>Release date</th>
<th>Data sheet status</th>
<th>Change notice</th>
<th>Supersedes</th>
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<td>20181205</td>
<td>Product data sheet</td>
<td>-</td>
<td>PESD5V0U2BMB v.1</td>
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**Modifications:**
- Legal texts have been adapted to the new company name where appropriate.
- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.

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<th>Data sheet ID</th>
<th>Release date</th>
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<th>Change notice</th>
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<td>20120313</td>
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15. Legal information

Data sheet status

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<th>Document status</th>
<th>Product status</th>
<th>Definition</th>
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<td>[1][2]</td>
<td>Production</td>
<td>Product [short] data sheet</td>
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</tbody>
</table>

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term "short data sheet" is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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For sales office addresses, please send an email to: salesaddresses@nexperia.com
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