1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, part of the TrEOS protection family. The device is housed in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- Bidirectional ESD protection of one line
- Surge robustness $I_{PPM} = 20$ A according to IEC 61000-4-5
- Extremely low diode capacitance $C_d = 0.5$ pF
- Extremely low clamping to protect sensitive I/Os
- Extremely low-inductance protection path to ground
- ESD protection up to ± 30 kV according to IEC 61000-4-2
- Ultra small SMD package

3. Applications

- USB3.2 and HDMI2.0 data lines
- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals

4. Quick reference data

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_d$</td>
<td>diode capacitance</td>
<td>$f = 1$ MHz; $V_R = 1.5$ V</td>
<td>-</td>
<td>0.5</td>
<td>0.6</td>
<td>pF</td>
</tr>
<tr>
<td>$V_{RWM}$</td>
<td>reverse standoff voltage</td>
<td></td>
<td>-</td>
<td>-</td>
<td>3.3</td>
<td>V</td>
</tr>
</tbody>
</table>
5. Pinning information

Table 2. Pinning information

<table>
<thead>
<tr>
<th>Pin</th>
<th>Symbol</th>
<th>Description</th>
<th>Simplified outline</th>
<th>Graphic symbol</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>K1</td>
<td>cathode (diode 1)</td>
<td>Transparent top view</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>K2</td>
<td>cathode (diode 2)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

6. Ordering information

Table 3. Ordering information

<table>
<thead>
<tr>
<th>Type number</th>
<th>Package</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PESD3V3W1BCSF</td>
<td>DSN0603-2</td>
<td>silicon, leadless ultra small package; 2 terminals; 0.4 mm pitch; 0.6 mm x 0.3 mm x 0.3 mm body</td>
</tr>
</tbody>
</table>

7. Marking

Table 4. Marking codes

<table>
<thead>
<tr>
<th>Type number</th>
<th>Marking code</th>
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</thead>
<tbody>
<tr>
<td>PESD3V3W1BCSF</td>
<td>g</td>
</tr>
</tbody>
</table>
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{\text{RWM}}$</td>
<td>reverse standoff voltage</td>
<td></td>
<td>-</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>$I_{\text{PPM}}$</td>
<td>rated peak pulse current $t_p = 8/20 \mu s$</td>
<td>[1] [2]</td>
<td>-</td>
<td>20</td>
<td>A</td>
</tr>
<tr>
<td>$T_{\text{amb}}$</td>
<td>ambient temperature</td>
<td></td>
<td>-40</td>
<td>125</td>
<td>°C</td>
</tr>
<tr>
<td>$T_{\text{stg}}$</td>
<td>storage temperature</td>
<td></td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
</tbody>
</table>

ESD maximum ratings

| $V_{\text{ESD}}$ | electrostatic discharge voltage | IEC 61000-4-2; contact discharge | [3] | -30 | 30  | kV  |
| $V_{\text{ESD}}$ | electrostatic discharge voltage | IEC 61000-4-2; air discharge    | [3] | -30 | 30  | kV  |

[1] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5.
[2] In positive and negative direction.

---

Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5 and IEC 61643-321

Fig. 2. ESD pulse waveform according to IEC 61000-4-2
9. Characteristics

Table 6. Characteristics

\( t_{\text{amb}} = 25^\circ \text{C unless otherwise specified.} \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{BR} )</td>
<td>breakdown voltage</td>
<td>( I_R = 1 \text{ mA} )</td>
<td>-</td>
<td>6.8</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>( I_{RM} )</td>
<td>reverse leakage current</td>
<td>( V_{RWM} = 3.3 \text{ V; } t_{\text{amb}} = 25^\circ \text{C} )</td>
<td>-</td>
<td>1</td>
<td>50</td>
<td>nA</td>
</tr>
<tr>
<td>( C_d )</td>
<td>diode capacitance</td>
<td>( f = 1 \text{ MHz; } V_R = 0 \text{ V} )</td>
<td>-</td>
<td>0.55</td>
<td>0.65</td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( f = 1 \text{ MHz; } V_R = 1.5 \text{ V} )</td>
<td>-</td>
<td>0.5</td>
<td>0.6</td>
<td>pF</td>
</tr>
<tr>
<td>( V_{CL} )</td>
<td>clamping voltage</td>
<td>( I_{PPM} = 20 \text{ A} )</td>
<td>[1]</td>
<td>5.1</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>( R_{dy} )</td>
<td>dynamic resistance</td>
<td>( I_R = 10 \text{ A} )</td>
<td>[2]</td>
<td>0.1</td>
<td>-</td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( I_R = -10 \text{ A} )</td>
<td>[2]</td>
<td>0.1</td>
<td>-</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( f_{3dB} )</td>
<td>-3 dB cut-off frequency</td>
<td>normalized to attenuation at 1 MHz</td>
<td>-</td>
<td>11.6</td>
<td>-</td>
<td>GHz</td>
</tr>
</tbody>
</table>

[1] Device stressed with 8/20 \( \mu \text{s} \) exponential decay waveform according to IEC 61000-4-5.


![Graph](aaa-028662)

Fig. 3. Insertion loss; typical values

![Graph](aaa-028663)

\[ a = \frac{C_d}{C_d(V_{RWM} = 0 \text{ V})} \]

Fig. 4. Relative capacitance as a function of reverse standoff voltage; typical values
Fig. 5. Differential Time Domain Reflectometer (TDR) plot; typical values

Data rate: 10 Gbit/s

Fig. 6. USB 3.2 eye diagram, PCB with device; typical values

Data rate: 10 Gbit/s

Fig. 7. USB 3.2 eye diagram, PCB without device; typical values
Extremely low capacitance bidirectional ESD protection diode

Data rate: 5 Gbit/s

Fig. 8. USB 3.2 eye diagram, PCB with device; typical values

Data rate: 5 Gbit/s

Fig. 9. USB 3.2 eye diagram, PCB without device; typical values
1080p
Data rate: 6 Gbit/s

Fig. 10.  HDMI2.0 TP1 eye diagram, PCB with device; typical values

1080p
Data rate: 6 Gbit/s

Fig. 11.  HDMI2.0 TP1 eye diagram, PCB without device; typical values
Extremely low capacitance bidirectional ESD protection diode

Fig. 12. HDMI2.0 TP2 eye diagram, PCB with device; typical values

Fig. 13. HDMI2.0 TP2 eye diagram, PCB without device; typical values
Extremely low capacitance bidirectional ESD protection diode

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Typical Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fig. 14</td>
<td>Dynamic resistance with positive clamping</td>
<td>$t_r = 1$ ns, $t_p = 100$ ns; Transmission Line Pulse (TLP)</td>
</tr>
<tr>
<td>Fig. 15</td>
<td>Dynamic resistance with negative clamping</td>
<td>$t_r = 1$ ns, $t_p = 100$ ns; Transmission Line Pulse (TLP)</td>
</tr>
<tr>
<td>Fig. 16</td>
<td>Dynamic resistance with positive clamping</td>
<td>$t_r = 600$ ps, $t_p = 5$ ns; Very-Fast Transmission Line Pulse (VF-TLP)</td>
</tr>
<tr>
<td>Fig. 17</td>
<td>Dynamic resistance with negative clamping</td>
<td>$t_r = 600$ ps, $t_p = 5$ ns; Very-Fast Transmission Line Pulse (VF-TLP)</td>
</tr>
</tbody>
</table>
Fig. 18. Dynamic resistance with positive clamping; typical values

Fig. 19. Dynamic resistance with negative clamping; typical values

Fig. 20. TLP voltage and current over time, typical values
10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

![Application diagram](image)

**Fig. 21. Application diagram**

**Circuit board layout and protection device placement**

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.
11. Package outline

Leadless ultra small package; 2 terminals; body 0.6 x 0.3 x 0.3 mm

Fig. 22. Package outline DSN0603-2 (SOD962-2)
12. Soldering

Footprint information for reflow soldering of leadless ultra small package; 2 terminals

Fig. 23. Reflow soldering footprint for DSN0603-2 (SOD962-2)
### 13. Revision history

<table>
<thead>
<tr>
<th>Data sheet ID</th>
<th>Release date</th>
<th>Data sheet status</th>
<th>Change notice</th>
<th>Supersedes</th>
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<tr>
<td>PESD3V3W1BCSF v.2</td>
<td>20190329</td>
<td>Product data sheet</td>
<td>-</td>
<td>PESD3V3W1BCSF v.1</td>
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<td></td>
<td></td>
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<td></td>
<td>Updated Package</td>
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<tr>
<td>PESD3V3W1BCSF v.1</td>
<td>20180627</td>
<td>Product data sheet</td>
<td>-</td>
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## Data sheet status

<table>
<thead>
<tr>
<th>Document status</th>
<th>Product status</th>
<th>Definition</th>
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<tbody>
<tr>
<td>Development</td>
<td>Development</td>
<td>This document contains data from the objective specification for product development.</td>
</tr>
<tr>
<td>Qualification</td>
<td>Qualification</td>
<td>This document contains data from the preliminary specification.</td>
</tr>
<tr>
<td>Production</td>
<td>Production</td>
<td>This document contains the product specification.</td>
</tr>
</tbody>
</table>

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2. The term "short data sheet" is explained in section "Definitions".
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