

PESD3V3L1UB

Low capacitance unidirectional ESD protection diode

6 April 2021

Product data sheet

1. General description

Low capacitance unidirectional ElectroStatic Discharge (ESD) protection diode in an ultra small and flat lead SOD523 (SC-79) Surface-Mounted Device (SMD) plastic packages designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- · Unidirectional ESD protection of one line
- Low diode capacitance: C_d = 34 pF
- Low clamping voltage: V_{CL} = 11 V
- Very low leakage current: I_{RM} = 100 nA
- ESD protection up to 30 kV
- IEC 61000-4-2; level 4 (ESD)
- AEC-Q101 qualified

3. Application information

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- Communication systems
- SIM card protection
- Portable electronics
- High-speed data lines

4. Quick reference data

Table 1. Quick reference data							
Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	3.3	V
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	34	40	pF

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5. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode[1]		
2	A	anode	1	006aaa152
			SC-79 (SOD523)	

[1] The marking bar indicates the cathode.

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PESD3V3L1UB		plastic, surface-mounted package; 2 leads; 1.2 mm x 0.8 mm x 0.6 mm body	SOD523			

7. Marking

Table 4. Marking codes	
Type number	Marking code
PESD3V3L1UB	27

8. Limiting values

Table 5. Limiting values

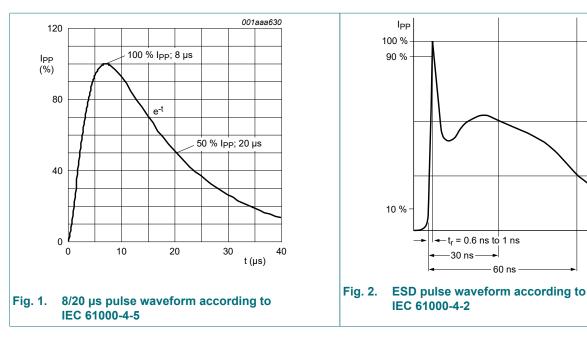
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P _{PPM}	rated peak pulse power	t _p = 8/20 μs	[1] [2]	-	45	W
I _{PPM}	rated peak pulse current		[1] [2]	-	4.5	А
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximu	ım ratings					
V _{ESD}	electrostatic discharge	IEC 61000-4-2 (contact discharge)	[3]	-	30	kV
	voltage	machine model		-	400	V
		MIL-STD-883 (human body model)		-	10	kV

[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC61000-4-5.

Measured from pin 1 to pin 2. [2]

Device stressed with ten non-repetitive ESD pulses. [3]



t

001aaa631

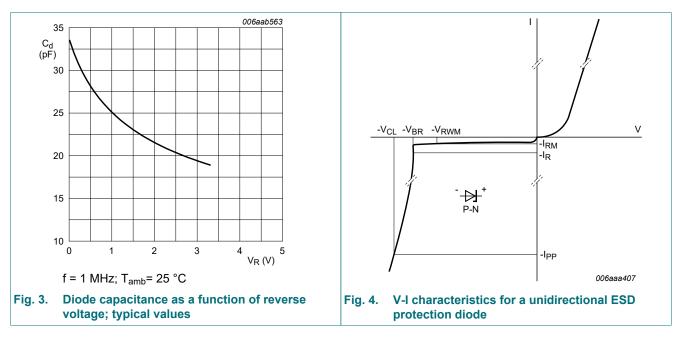
60 ns

9. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Мах	Unit
V _F	forward voltage	I _F = 200 mA; T _{amb} = 25 °C		-	-	1.2	V
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	3.3	V
V _{BR}	breakdown voltage	I _R = 5 mA; T _{amb} = 25 °C		5.3	5.6	6	V
I _{RM}	reverse leakage current	V _{RWM} = 3.3 V; T _{amb} = 25 °C		-	100	300	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	34	40	pF
V _{CL}	clamping voltage	I _{PPM} = 1 A; T _{amb} = 25 °C	[1] [2]	-	-	8	V
		I _{PPM} = 4.5 A; T _{amb} = 25 °C	[1] [2]	-	-	11	V
r _{dif}	differential resistance	I _R = 5 mA; T _{amb} = 25 °C		-	-	30	Ω

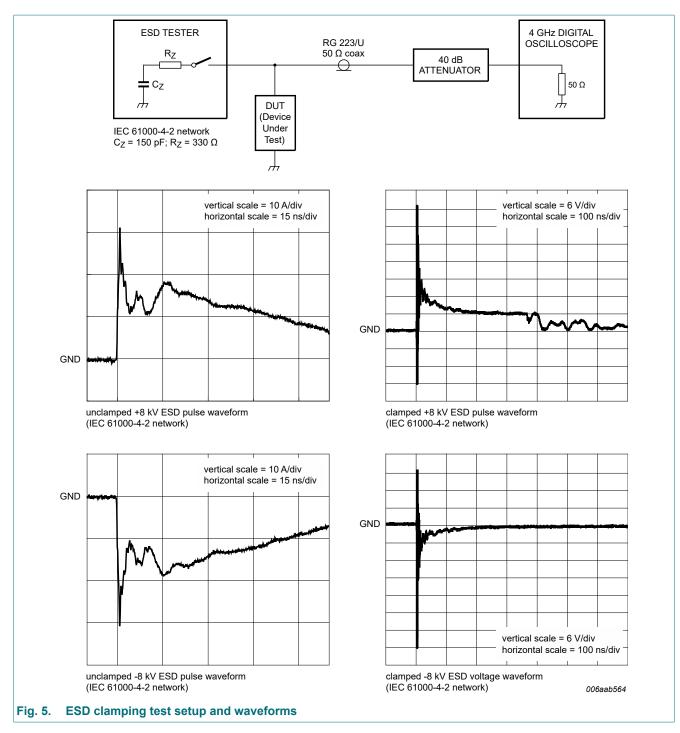
[1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.

[2] Measured from pin 1 to pin 2.



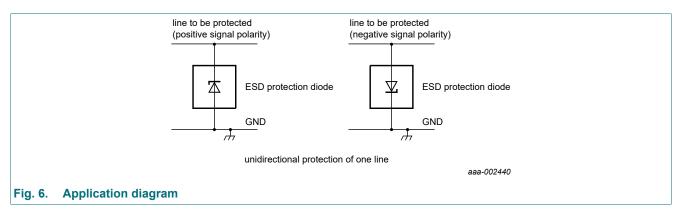
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10. Application information

The device is designed for the protection of one unidirectional data or signal line from the damage caused by ESD and surge pulses. The device may be used on lines where the signal polarities are either positive or negative with respect to ground. The device provides a surge capability up to 45 W per line for an 8/20 µs waveform.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- **1.** Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

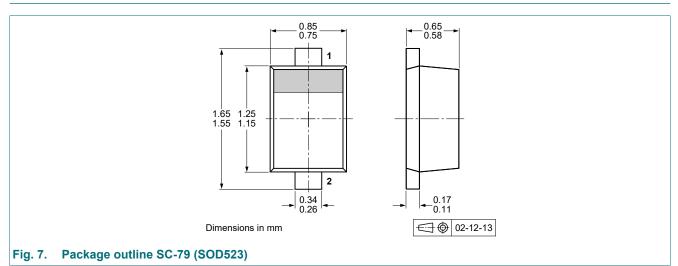
11. Test information

Quality information

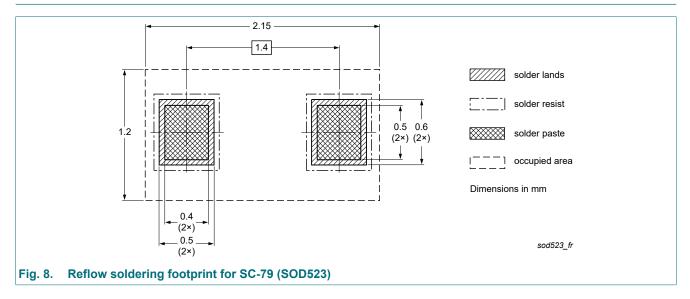
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

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12. Package outline



13. Soldering



14. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes	
PESD3V3L1UB v.2	20210406	Product data sheet	-	PESD3V3L1UA_UB_UL v.1	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Family data sheet reduced to single type data sheet. Figure "Reflow soldering footprint for SOD523" updated. 				
PESD3V3L1UA_UB_UL v.1	20090617	Product data sheet	-	-	

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <u>https://www.nexperia.com</u>.

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